TD34TS04
Temperature Sensor with 4-Kbit SPD EEPROM

GENERAL DESCRIPTION

The TD34TS04 is a temperature sensor product with embedded 4-Kbit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I^2C/SMBus interface and compliant to the JEDEC TSE2004av specification. The EEPROM memory is organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks. This product is designed for memory module applications in most PC and server platforms, as well as other related applications. All the information concerning the DRAM Dual Inline Memory Modules (DIMMs) configuration content (such as its access speed, its size, and its organization) can be kept write protected in one or more of the blocks of memory.

The TD34TS04 operates in a supply voltage range of 1.7V to 3.6V and is offered in 8-pin ultra-thin UTDFN package, 2mm × 3mm × 0.6mm (MAX), which is lead/halogen free, RoHS compliant, providing space as well as cost saving for DIMM manufactures.

The embedded 4-Kbit SPD EEPROM is protocol compatible with previous generation 2-Kbit device. The page selection method allows commands used with legacy device to applied to the lower or upper pages of the EEPROM/Temperature Sensor. In this way, the TD34TS04 may be used in legacy applications without software changes. Individually locking a 128-byte block of the EEPROM may be accomplished using a Software Write Protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific I^2C Bus sequence, each block may be protected from writes until write protection is electrically reversed using a separate I^2C Bus sequence which also requires V_{HV} on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared. The operating ambient temperature range of the EEPROM is from -40℃ to +125℃.

The temperature sensor monitors the ambient temperature range from -40℃ to 125℃. The temperature sensor includes a high precision band gap type temperature sensor, a sigma-delta analog-to-digital converter (ADC) and a serial interface compatible to industrial standard I^2C/SMBus. The ADC default resolution is set at 10-bit (0.25℃/LSB). The accuracy over various temperature ranges is:

- ±0.5℃ (TYP) for an active range from +75℃ to +95℃
- ±1℃ (TYP) for a monitor range from +40℃ to +125℃
- ±2℃ (TYP) for a temperature range from -40℃ to 125℃

The temperature sensor can be set in power-saving shutdown mode with a low current of 2μA (TYP) with SPD EEPROM in Standby mode.

The temperature sensor component has user-programmable registers that are used to configure both the temperature sensor performance and response to over-temperature conditions. The device contains programmable high, low and critical temperature limits. The $\overline{\text{EVENT}}$ pin can be configured as active-high or active-low and can be configured to operate as an interrupt or as a comparator output.

The TD34TS04 is available in a Green UTDFN-2×3-8AL package.

FEATURES

- Temperature Sensor with Integrated 4-Kbit SPD EEPROM
- Fully Compliant with JEDEC TSE2004av Specification
- Supply Voltage: 1.7V to 3.6V
- 2-Wire Serial Interface I^2C/SMBus Compatible
  - Up to 1MHz Transfer Rate (I^2C Fast Mode+) Supported
  - Bus Timeout Supported
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Operating Temperature Range: -40℃ to +125℃
- Available in a Green UTDFN-2×3-8AL Package

TEMPERATURE SENSOR

- Temperature Sensor Accuracy:
  - ±0.5℃ (TYP) from +75℃ to +95℃
  - ±1℃ (TYP) from +40℃ to +125℃
  - ±2℃ (TYP) from -40℃ to +125℃
- Temperature Sensor Resolution:
  - 10-Bit Analog-to-Digital Converter with 0.25℃/LSB Resolution (Default)
  - Programmable 9-12 Bits
- ADC Conversion Time: 125ms (MAX)
- Programmable Temperature Hysteresis Threshold: 0, 1.5, 3 and 6.0℃
- Low Operating Current
  - Temperature Sensor Active (EEPROM Standby): 0.2mA (MAX)
  - Temperature Sensor Shutdown (EEPROM Standby): 5μA (MAX)

SPD EEPROM

- Functionality Identical to TD34C04 SPD EEPROM
- Software Data Protection on All Four 128-byte Blocks
- Byte and Page Write Mode
  - Page Size up to 16 Bytes
- Self-timed Write Cycle: 3ms (MAX)
- Operating Temperature Range: -40℃ to +125℃
- High Reliability
  - Endurance: 1,000,000 Write Cycles at T_A = +25℃
  - Data Retention: 100 Years at T_A = +25℃
- Low Operating Current
  - SPD EEPROM Write Current: 0.5mA (MAX)
  - SPD EEPROM Read Current: 0.5mA (MAX)

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
TD34TS04	UTDFN-2×3-8AL	-40℃ to +125℃	TD34TS04-ULPTR	TDT34ULP YYWW	Tape and Reel, 3000

MARKING INFORMATION



TD: SGMICRO Logo

T34ULP: TD34TS04-ULP

YYWW: Date Code, YY = Year, WW = Week
Example: 2140 = Year 2021, Week 40

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to 4.3V
Voltage on Pin SA0, V_{SA0} ..... -0.5V to 10V
Voltage on input Pins, V_{IN} ..... -0.5V to 4.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

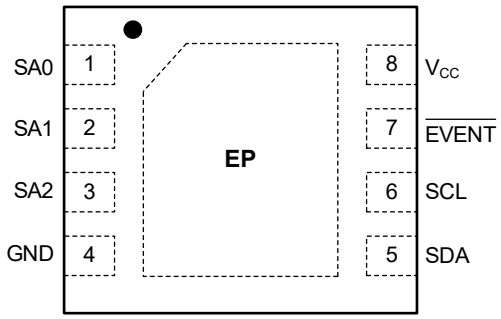
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTDFN-2×3-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	SA0	I	Device Address Inputs. The SA0, SA1 and SA2 pins are used to select the device address and correspond to the 3 least significant bits of the I^2C/SMBus 7-bit slave address. These pins can be directly connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus. The SA0 pin is also used to detect the V_{HV} voltage, when decoding a SWPn or CWP instruction. See Table 24 for decode details.
2	SA1		
3	SA2		
4	GND	P	Ground. The ground reference for the power supply. GND should be connected to the system ground.
5	SDA	I/O	Serial Data. The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
6	SCL	I	Serial Clock. The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
7	$\overline{\text{EVENT}}$	O	$\overline{\text{EVENT}}$ Pin. The $\overline{\text{EVENT}}$ pin is an open-drain output pin and is active-low. A pull-up resistor must be connected to this pin. It has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt mode, Comparator mode and TCRIT Only mode. See **Event Output Pin Functionality** for details.
8	V_{CC}	P	Device Power Supply. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

NOTE: I = input, O = output, I/O = input/output, P = power.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Operating conditions: T_A = -40℃ to +125℃, V_{CC} = 1.7V to 3.6V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Voltage	V_{CC}		1.7	3.6	V
Supply Current, Read Operation	I_{CC1}	V_{CC} = 3.6V, f_C = 1MHz		0.5	mA
Supply Current, Write Operation (1)	I_{CC2}	V_{CC} = 3.6V, f_C = 1MHz		0.5	mA
Standby Supply Current	I_{SB}	TS active, EEPROM standby		200	μA
Shutdown Mode Supply Current	I_{SD}	TS shutdown, EEPROM standby		5	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND		±5	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or GND or V_{CC}, SDA in Hi-Z		±5	μA
Input Low Voltage (SDA, SCL)	V_{IL}		-0.5	0.3 × V_{CC}	V
Input High Voltage (SDA, SCL)	V_{IH}		0.7 × V_{CC}	V_{CC} + 0.5	V
SA0 Pin High Voltage	V_{HV}	V_{HV} - V_{CC} ≥ 4.8V	7	10	V
Output Low Voltage (2) Open-Drain or Open-Collector	V_{OL1}	V_{CC} > 2V, I_{OL} = 3mA		0.4	V
	V_{OL2}	V_{CC} ≤ 2V, I_{OL} = 2mA		0.2 × V_{CC}	V
Low-Level Output Current (3)	I_{OL}	V_{OL} = 0.4V	3.0	20	mA
		V_{OL} = 0.6V	6.0		mA
Input Hysteresis	V_{HYST}	V_{CC} < 2V	0.10 × V_{CC}		V
		V_{CC} ≥ 2V	0.05 × V_{CC}		V

NOTES:

1. This parameter is ensured by design and characterization only.

2. The same resistor value to drive 3mA at 3.0V V_{CC} provides the same RC time constant when using < 2V V_{CC} with a smaller current draw.

3. In order to drive full bus load at 400kHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts not meeting this specification can still function, but not at 400kHz and 400pF.

ELECTRICAL CHARACTERISTICS (continued)

AC Characteristics

(Operating conditions: Input rise and fall time ≤ 50ns; input pulse voltages: 0.2 × V_{CC} to 0.8 × V_{CC}; input and output timing reference voltages: 0.3 × V_{CC} to 0.7 × V_{CC}; unless otherwise noted.)

PARAMETER	SYMBOL	V_{CC} < 2.2V		V_{CC} ≥ 2.2V				UNITS
		100kHz		400kHz		1000kHz		
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Frequency, SCL	f_{SCL}	10	100	10	400	10	1000	kHz
Clock Pulse Width High	t_{HIGH}	4000		600		260		ns
Clock Pulse Width Low	t_{LOW} (1)	4700		1300		500		ns
Detect Clock Low Timeout	$t_{TIMEOUT}$ (2)	25	35	25	35	25	35	ms
SDA Rise Time	t_R (3)		1000	20	300		120	ns
SDA Fall Time	t_F (3)		300	20	300		120	ns
Data In Set-up Time	$t_{SU.DAT}$	250		100		50		ns
Data In Hold Time	$t_{HD.DI}$	0		0		0		ns
Data Out Hold Time	$t_{HD.DAT}$	200	3450	200	900	0	350	ns
Start Condition Setup Time	$t_{SU.STA}$ (4)	4700		600		260		ns
Start Condition Hold Time	$t_{HD.STA}$	4000		600		260		ns
Stop Condition Setup Time	$t_{SU.STO}$	4000		600		260		ns
Time between Stop Condition and Next Start Condition	t_{BUF}	4700		1300		500		ns
Write Cycle Time	t_{WR}		3	-	3		3	ms

NOTES:

1. The TD34TS04 shall not initiate clock stretching, which is an optional I^2C Bus feature.
2. I^2C bus Masters can terminate a transaction in process and reset device communication on the bus by asserting SCL low for $t_{TIMEOUT,MAX}$ or longer. The TD34TS04 detects this condition must reset their communication and be able to receive a new Start condition no later than $t_{TIMEOUT,MAX}$; the device will not reset if SCL stretching is less than $t_{TIMEOUT,MIN}$.
3. Guaranteed by design and characterization, not necessarily tested.
4. For a re-Start condition, or following a write cycle.

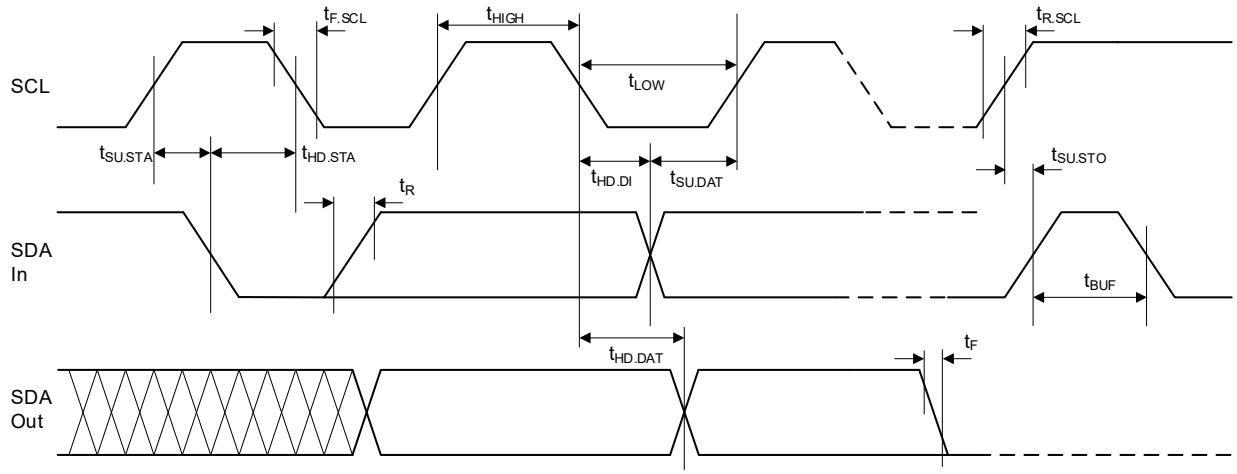


Figure 1. Bus Timing

ELECTRICAL CHARACTERISTICS (continued)

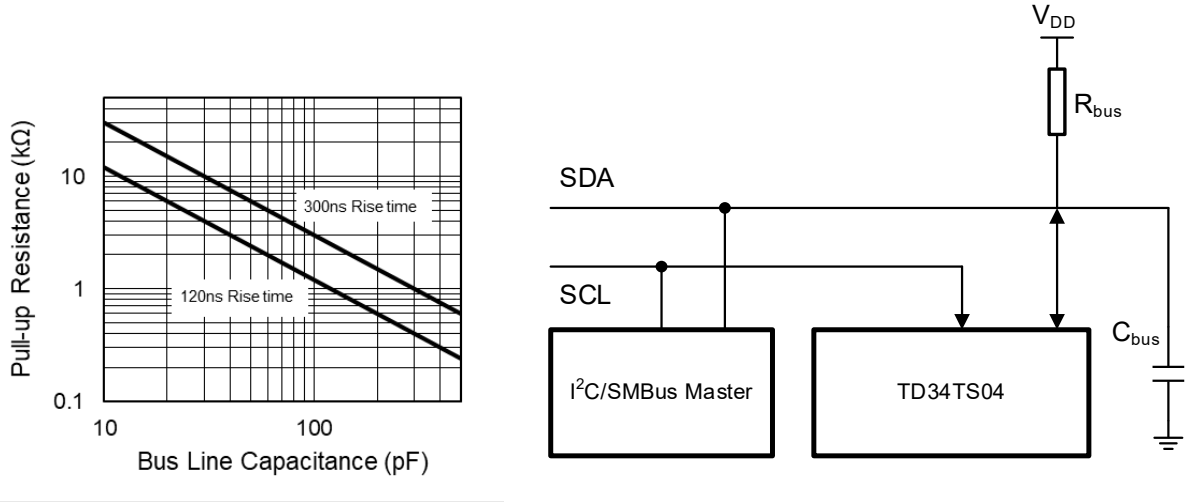


Figure 2. Maximum Pull-up Resistance vs. Bus Parasitic Capacitance

Capacitance

(Operating range for pin capacitance: T_A = +25℃, f_C = 400kHz, V_{CC} = 1.7V to 3.6V, unless otherwise noted.)

PARAMETER (1)	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input/output Capacitance (SDA)	$C_{I/O}$			8	pF
Input Capacitance (SA0, SA1, SA2, SCL)	C_{IN}			6	pF
SA0, SA1, SA2 input impedance	Z_{AIL}	V_{IN} < 0.3 × V_{CC}	30		kΩ
SA0, SA1, SA2 input impedance	Z_{AIH}	V_{IN} > 0.7 × V_{CC}	800		kΩ
Pulse width of spikes that must be suppressed by the input filter on SCL and SDA	t_{SP}	Single glitch, f_C ≤ 100kHz			ns
		Single glitch, f_C > 100kHz	0	50	

NOTE: 1. These parameters are ensured by design and characterization only.

Temperature to Digital Conversion Performance

(Typical numbers taken at V_{CC} = 3.3V, T_A = 25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TYP	MAX	UNITS
Temperature Sensor Accuracy (B-Grade)	T_{ACC}	+75℃ < T_A < +95℃	±0.5	±1	℃
		+40℃ < T_A < +125℃	±1	±2	℃
		-20℃ < T_A < +125℃	±2	±3	℃
Temperature Sensor Resolution	R_{TS}		0.25	0.0625	℃/LSB
ADC Resolution	R_{ADC}		10	12	bit
Conversion Time	t_{CONV}		70	125	ms

SPD EEPROM Reliability

PARAMETER	SYMBOL	CONDITIONS	MIN	UNITS
Write Cycle Endurance	N_W	T_A = +25℃, Page mode	1×10^6	cycle
		T_A = +125℃, Page mode	1×10^5	
Data Retention	D_R	T_A = +25℃	100	year

FUNCTIONAL BLOCK DIAGRAM

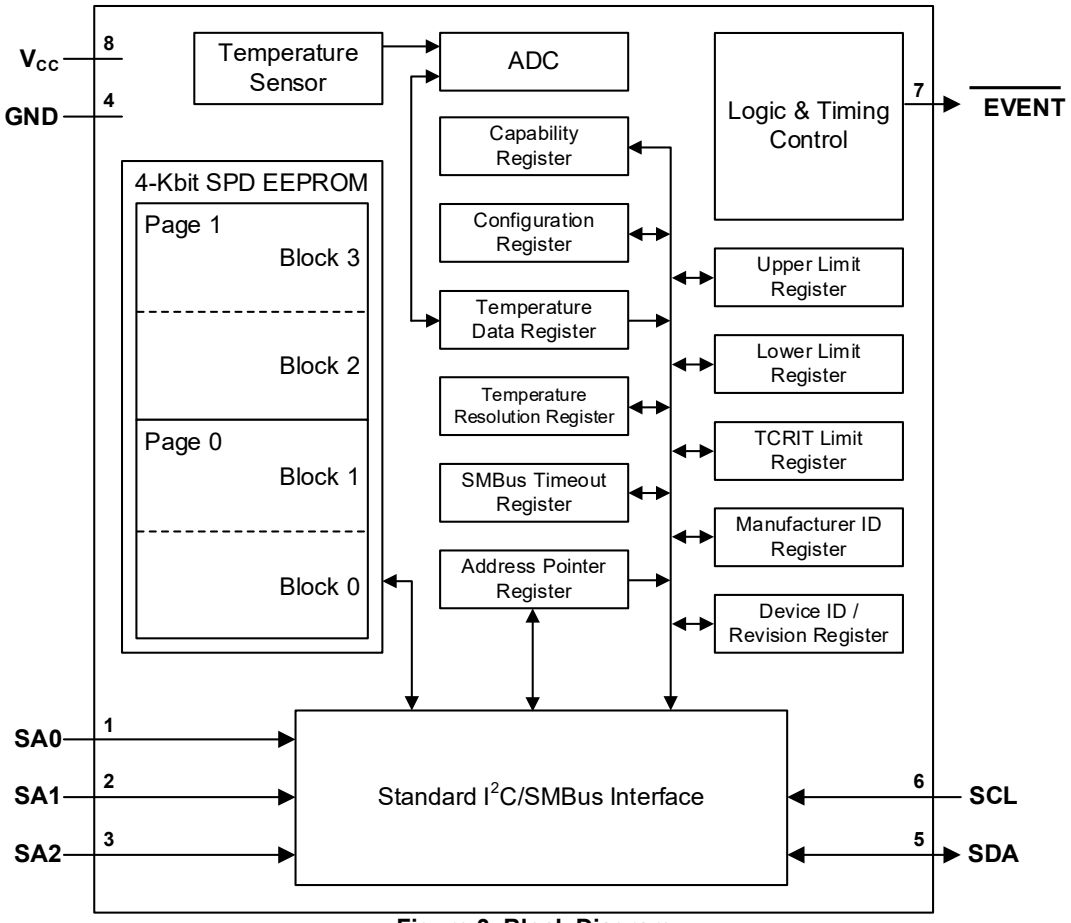


Figure 3. Block Diagram

DEVICE COMMUNICATION

The TD34TS04 operates as a slave device and utilizes a 2-wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the TD34TS04 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after 8 bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a 9th clock cycle generated by the Master. Therefore, 9 clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see Figure 4). The TD34TS04 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

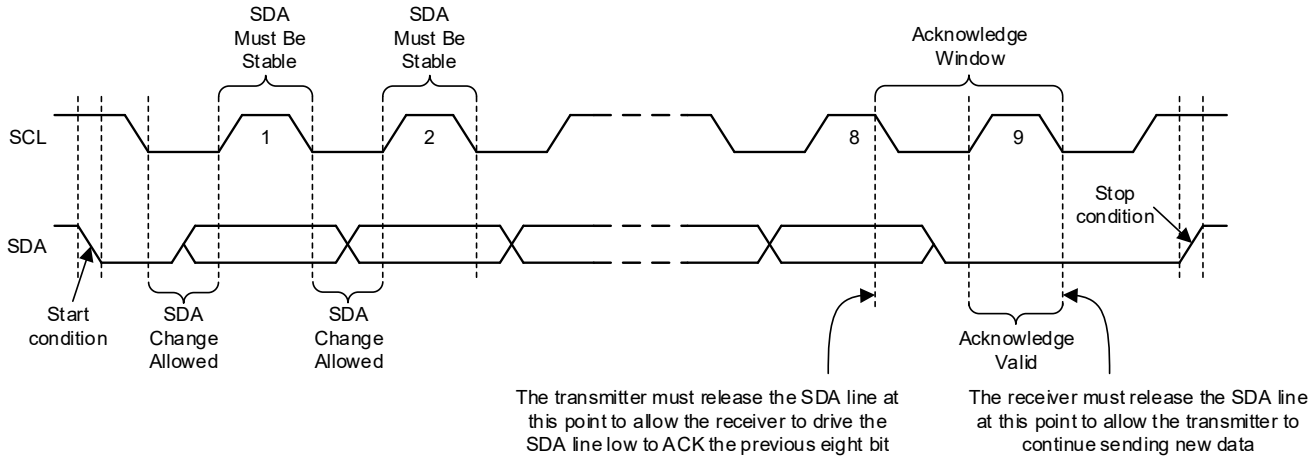


Figure 4. Start, Stop, and ACK

Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see Figure 4). A Stop condition terminates communication between the TD34TS04 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the TD34TS04 subsequently returns to Standby mode after receiving a Stop condition.

Acknowledge (ACK)

After each byte of data is received, the TD34TS04 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a 9th clock cycle for every byte). During the ACK/NACK clock cycle, the TD34TS04 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see Figure 4).

DEVICE COMMUNICATION (continued)

When the TD34TS04 is transmitting data to the Master, the Master can indicate that it is done receiving data and end the operation by sending an NACK response to the TD34TS04 instead of an ACK response. This is accomplished by the Master outputting Logic 1 during the ACK/NACK clock cycle, at which point the TD34TS04 should release the SDA line so that the Master can then generate a Stop condition.

In addition, the TD34TS04 can use an NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to Write to a Read-Only register.

Device Reset and Initialization

The TD34TS04 incorporates an internal Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC} (MIN) without any ring back to ensure a proper power-up (see Figure 5). Once the supply voltage passes V_{POR}, the device is reset. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.

At power-down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{CC} must remain below V_{POFF} for t_{POFF}, and must meet cold power-on reset timing when restoring power.

Parameters related to power-up conditions are listed in Table 1.

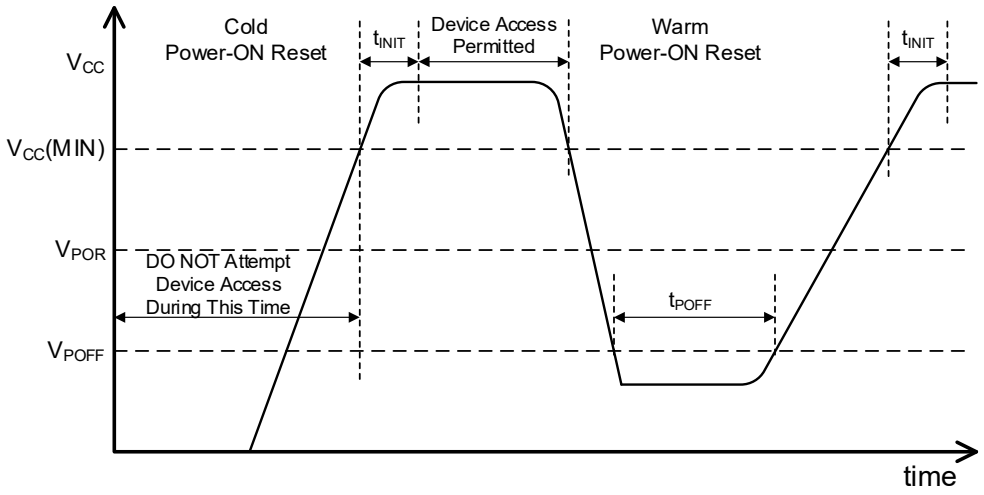


Figure 5. Power-up Timing

Table 1. Power-up Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{POR}	Power-On Reset Threshold Voltage	1.6		V
V_{POFF}	Power-Off Threshold for Warm Power-On Cycle		0.9	V
t_{INIT}	Time from Power-On to First Command	10.0		ms
t_{POFF}	Warm Power Cycle Off Time	1.0		ms

DEVICE COMMUNICATION (Continued)

Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock 9 cycles.
3. Create another Start condition followed by Stop condition (see Figure 6).

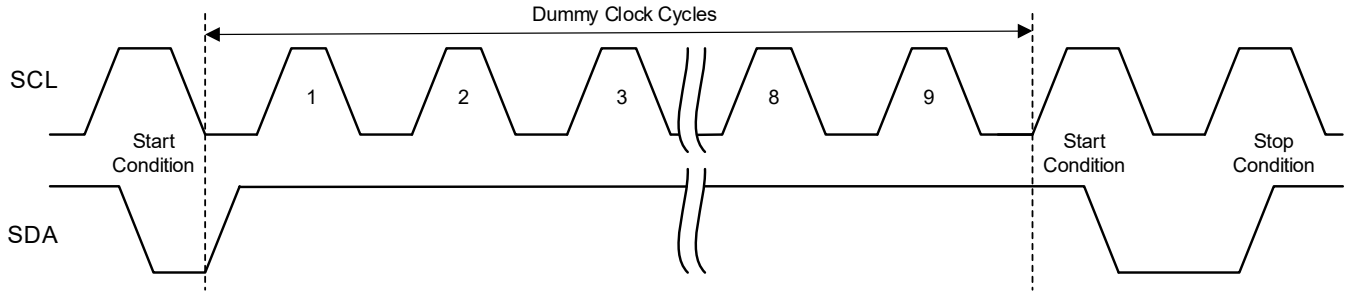


Figure 6. 2-Wire Software Reset

Timeout Function

The TD34TS04 supports the industry standard bus timeout feature to prevent potential system bus lock-ups. The device resets the serial interface and returns to Standby mode if the SCL pin is held low for more than the maximum timeout t_{OUT} (MAX) specification. If the SCL pin is held low for less than the minimum timeout t_{OUT} (MIN) specification, the device will not reset the serial interface (see Figure 7). This feature requires a minimum SCL clock speed of 10kHz to avoid any timeout issues.

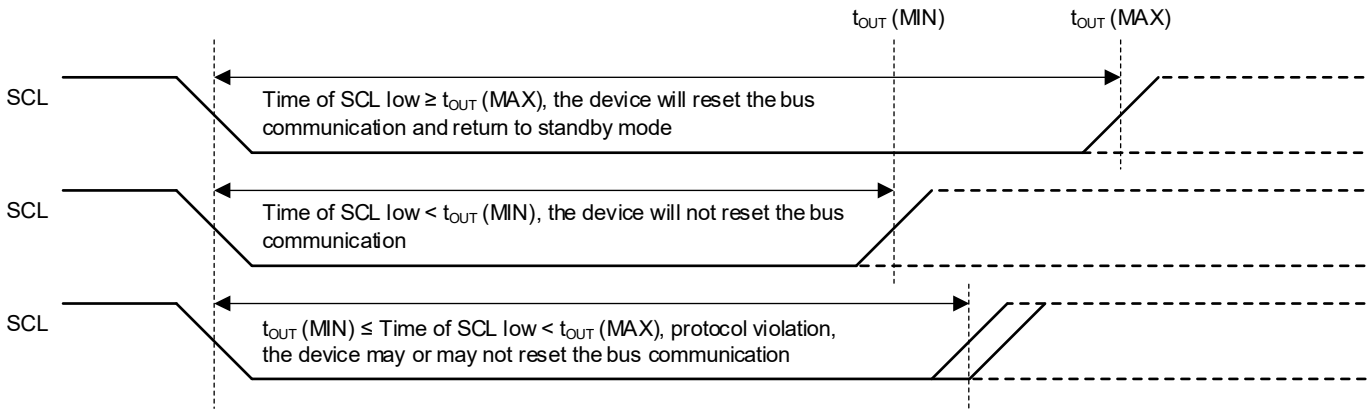


Figure 7. Bus Timeout

DEVICE ADDRESSING

The TD34TS04 is designed to allow the temperature sensor and the SPD EEPROM to operate in parallel while executing valid command protocol. For example, when the temperature sensor is busy during a temperature conversion cycle, it is possible to perform any SPD EEPROM operation during this time.

The device requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with either the temperature sensor or the SPD EEPROM. The device address byte is comprised of a 4-bit Device Type Identifier (DTI) followed by three device address bits (A2, A1 and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the most significant bit first (see Table 2).

The TD34TS04 will respond to three unique device type identifiers. The device type identifier of '1010' is necessary to select the SPD EEPROM for Read or Write operation. The device type identifier of '0110' is used to access the page address function which determines what the internal address counter is set to. The device type identifier of '0110' is also used to access the Software Write Protection feature of the device. The device type identifier of '0011' is used to access the temperature sensor registers for Read or Write operation. The software device address bits (A2, A1 and A0) must match their corresponding hard-wired device address inputs ($\overline{SA2}$, $\overline{SA1}$ and $\overline{SA0}$) (see Table 3), allowing up to 8 devices on the bus at the same time. The 8th bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the TD34TS04 will output an ACK or an NACK during the 9th clock cycle if the compare is true or not true. The device will return to the low-power Standby mode after an NACK.

Table 2. TD34TS04 Device Address Byte

FUNCTION	DEVICE TYPE IDENTIFIER				DEVICE ADDRESS			TYPE
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SPD EEPROM for Read or Write Operation	1	0	1	0	A2	A1	A0	R/W
SPD EEPROM Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/W
Temperature Sensor Registers	0	0	1	1	A2	A1	A0	R/W

Table 3. Device Address Combinations

SOFTWARE DEVICE ADDRESS BITS			HARD-WIRED DEVICE ADDRESS INPUTS		
A2	A1	A0	SA2	SA1	SA0
0	0	0	GND	GND	GND
0	0	1	GND	GND	V_{CC}
0	1	0	GND	V_{CC}	GND
0	1	1	GND	V_{CC}	V_{CC}
1	0	0	V_{CC}	GND	GND
1	0	1	V_{CC}	GND	V_{CC}
1	1	0	V_{CC}	V_{CC}	GND
1	1	1	V_{CC}	V_{CC}	V_{CC}

TEMPERATURE SENSOR

The temperature sensor component consists of a sigma-delta analog-to-digital converter (ADC) with a bandgap type temperature sensor and continuously monitors the ambient temperature and updates the Temperature Data Register. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Temperature Sensor Write Operation

Writing to the TD34TS04 temperature register set is accomplished through a modified block Write operation for two data bytes. To maintain I^2C Bus compatibility, the 16-bit register is accessed through a Pointer Register, requiring the write sequence to include an Address Pointer Register in addition to the slave address, which indicates the storage location for the next two bytes received. Figure 8 shows an entire write transaction on the bus.

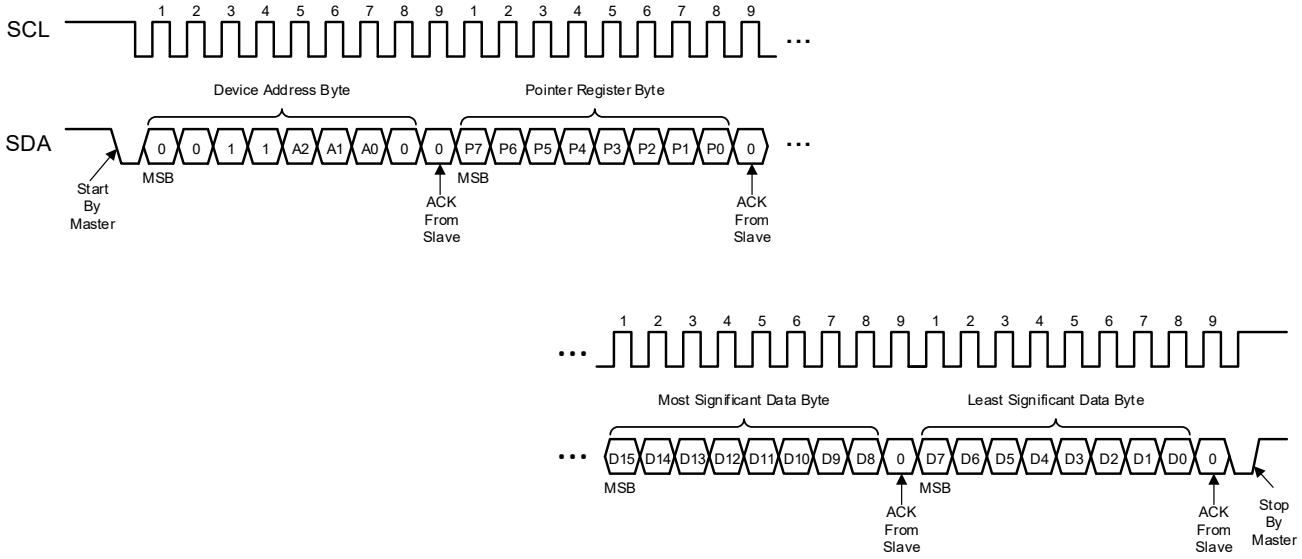


Figure 8. Temperature Sensor Write Operation

TEMPERATURE SENSOR (continued)

Temperature Sensor Read Operation

Reading data from the temperature sensor may be accomplished in one of two ways:

1. If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a slave address from the bus Master followed by two bytes of data from the device; or

2. The Pointer Register is loaded with the correct register address, and the data is read. The preset pointer read is shown in Figure 9. If it is desired to read random address each cycle, the complete pointer write, word read sequence is shown in Figure 10.

The data byte has the MSB first. At the end of a read, this device can accept either ACK or NACK from the Master (NACK is typically used as a signal for the slave that the Master has read its last byte).

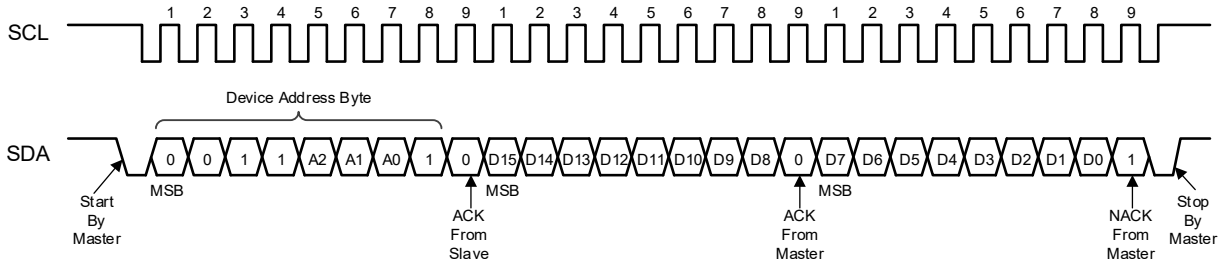


Figure 9. I²C Bus Preset Pointer Register Word Read

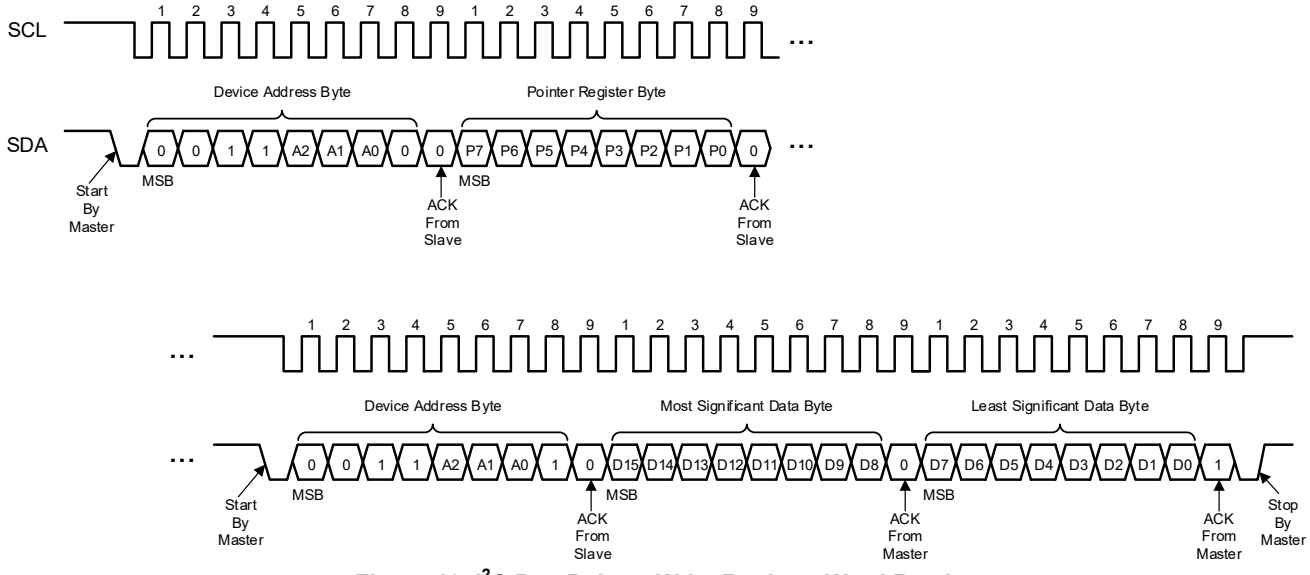


Figure 10. I²C Bus Pointer Write Register Word Read

TEMPERATURE SENSOR (continued)

Temperature Sensor Register Overview

The TD34TS04 contains several registers that are user accessible and/or programmable and utilized for latching the temperature readings, storing high, low and critical temperature limits, configuring the temperature sensor performance, and reporting temperature sensor status.

These registers include a Capability Register, Configuration Register, High Limit Register, Low Limit Register, TCRIT Limit Register, Temperature Data Register, Manufacturer ID Register, Device ID/Revision Register, Temperature Resolution Register and SMBus Timeout Register, as shown in Table 4.

The TD34TS04 utilizes an Address Pointer Register to access the 16-bit registers. This Pointer Register is an 8-bit Write-Only register (see Table 5). Bit 7 through bit 4 must always be written to '0'. The power-on default value is 00h which is the address location for the Capability Register.

Table 4. Temperature Sensor Registers Summary

ADDRESS	TYPE	REGISTER NAME	FUNCTION	DEFAULT
N/A	W	Address Pointer	Address storage for subsequent operations	Undefined
00h	R	Capability	Functions and Capability of the temperature sensor	00EFh
01h	R/W	Configuration	Operation control of the temperature monitor	0000h
02h	R/W	High Limit	Temperature High Limit	0000h
03h	R/W	Low Limit	Temperature Low Limit	0000h
04h	R/W	TCRIT Limit	Critical temperature	0000h
05h	R	Temperature Data	Current Ambient temperature	N/A
06h	R	Manufacturer ID	Manufacturer ID	104Ah
07h	R	Device ID/Revision	Device ID and Revision number	2201h
08h	R/W	Temperature Resolution	Selected Temperature Resolution	0001h
09h	R/W	SMBus Timeout	SMBus Timeout status	0080h
0A - 0Fh	R/W	Vendor-defined	Vendor specific information	N/A

NOTE: Registers beyond the specified (00 - 09h) are reserved and must not be accessed by the user in system application, or it may cause undesirable results.

Table 5. Address Pointer Register Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	P4	P3	P2	P1

TEMPERATURE SENSOR (continued)

REG0x00: Capability Register

The temperature sensor Capability Register indicates the supported features of the temperature sensor portion of the TD34TS04. This register is Read-Only and writing to the register will have no effect. Table 6 shows the Capability Register bit definition.

Table 6. Capability Register Bit Definition

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[15:8]	Reserved	R	00h	Reserved
D[7]	EVSD	R	1	$\overline{\text{EVENT}}$ Output with Shutdown Action: 1 = The $\overline{\text{EVENT}}$ pin output is de-asserted (not driven) when entering shutdown mode and will remain de-asserted upon exit from shutdown mode until the next temperature measurement sample is taken. In Interrupt mode, the $\overline{\text{EVENT}}$ pin maybe asserted when existing Shutdown if a pending interrupt has not been cleared.
D[6]	TMOUT	R	1	Bus Timeout Period during Normal Operation: 1 = Bus Timeout supported within the range 25ms to 35ms (default) 0 = Bus Timeout is disabled
D[5]	VHV	R	1	SA0 Pin High Voltage: 1 = The SA0 pin supports a maximum voltage up to 10V
D[4:3]	TRES[1:0]	R	01	Temperature Resolution: 00 = 9-bit, 0.5℃/LSB 01 = 10-bit, 0.25℃/LSB (default) 10 = 11-bit, 0.125℃/LSB 11 = 12-bit, 0.0625℃/LSB
D[2]	RANGE	R	1	Supported Temperature Range: 1 = Temperatures below 0 ℃ can be read and the Sign bit will be set accordingly
D[1]	ACC	R	1	Supported Temperature Accuracy: 1 = Supports a B-grade accuracy of ±1℃ over the active range (+75℃ to +95℃) and ±2℃ over the monitor range (+40℃ to +125℃).
D[0]	EVENT	R	1	Interrupt Capability: 1 = The device supports Interrupt Capability

REG0x01: Configuration Register

The temperature sensor Configuration Register holds the control and status bits of the $\overline{\text{EVENT}}$ output pin as well as general hysteresis on all limits. To avoid glitches on the $\overline{\text{EVENT}}$ output pin, users should disable EVENT or TCRIT functions prior to programming or changing other device configuration settings. Table 7 shows the Configuration Register bit definition.

Table 7. Configuration Register Bit Definition

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[15:11]	Reserved	R/W	0	Reserved
D[10:9]	HYST[1:0]	R/W	00	Applied Hysteresis (see Table 8 and Figure 11) : 00 = Hysteresis is disabled (default) 01 = Hysteresis is enabled at 1.5℃ 10 = Hysteresis is enabled at 3℃ 11 = Hysteresis is enabled at 6℃ This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. The hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set (bit 7 and bit 6), these bits cannot be altered.
D[8]	SHDN	R/W	0	Shutdown Mode: 0 = The thermal sensor is active and converting (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set (bit 7 and bit 6), this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the device still responds to commands normally, however bus timeout may or may not be supported in this mode.

TEMPERATURE SENSOR (continued)

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[7]	TCRIT_LOCK	R/W	0	Locks the TCRIT Limit Register: 0 = The TCRIT Limit Register can be updated normally (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data
D[6]	EVENT_LOCK	R/W	0	Locks the High and Low Limit Registers: 0 = The High and Low Limit Registers can be updated normally (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data
D[5]	CLEAR	R/W	0	Clears the $\overline{\text{EVENT}}$ pin asserted: 1 = The $\overline{\text{EVENT}}$ pin is released and will not be asserted until a new interrupt condition occurs This bit is ignored if the device is operating in Comparator mode. This bit is self-clearing and write only and will always read '0'.
D[4]	EVENT_STS	R/W	0	$\overline{\text{EVENT}}$ pin asserted status: 0 = The $\overline{\text{EVENT}}$ pin is not being asserted by the device (default) 1 = The $\overline{\text{EVENT}}$ pin is being asserted by the device
D[3]	EVENT_CTRL	R/W	0	Masks the $\overline{\text{EVENT}}$ pin from generating an interrupt: 0 = The $\overline{\text{EVENT}}$ pin is disabled and will not generate interrupts (default) 1 = The $\overline{\text{EVENT}}$ pin is enabled If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.
D[2]	TCRIT_ONLY	R/W	0	$\overline{\text{EVENT}}$ pin asserted from a high / low out-of-limit condition: 0 = The $\overline{\text{EVENT}}$ pin will be asserted if the measured temperature is above the High Limit or below the Low Limit Register in addition to if the temperature is above the TCRIT Limit Register. (default) 1 = The $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature is above the TCRIT Limit Register. When the EVENT_LOCK bit is set, this bit cannot be altered.
D[1]	EVENT_POL	R/W	0	"Active" state of $\overline{\text{EVENT}}$ pin asserted: 0 = The $\overline{\text{EVENT}}$ pin is active low; the active state of the pin will be Logic 0 (default) 1 = The $\overline{\text{EVENT}}$ pin is active high; the active state of the pin will be Logic 1 If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.
D[0]	EVENT_MODE	R/W	0	$\overline{\text{EVENT}}$ pin function mode: 0 = The $\overline{\text{EVENT}}$ pin will function in comparator mode (default) 1 = The $\overline{\text{EVENT}}$ pin will function in Interrupt mode If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.

Table 8. Hysteresis as Applied to Temperature Movement

	BELOW ALARM WINDOW BIT		ABOVE ALARM WINDOW BIT	
	TEMPERATURE SLOPE	TEMPERATURE THRESHOLD	TEMPERATURE SLOPE	TEMPERATURE THRESHOLD
Sets	Falling	T_L-HYS (1)	Rising	T_H (2)
Clears	Rising	T_L	Falling	T_H-HYS (3)

NOTES:

1. T_L = Value Stored in the Low Limit Register.
2. T_H = Value Stored in the High Limit Register.
3. HSY = Absolute Value of Selected Hysteresis.

TEMPERATURE SENSOR (continued)

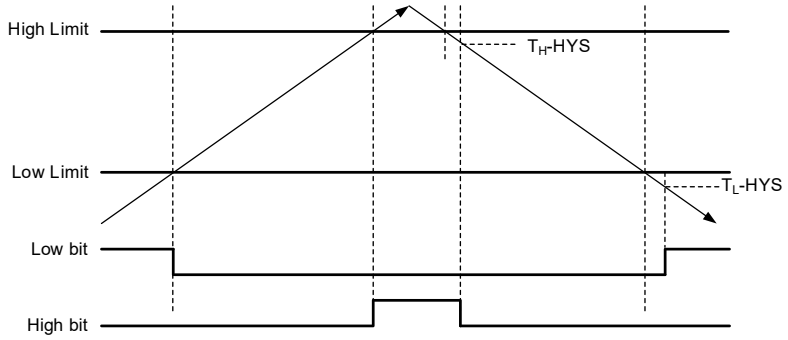


Figure 11. Hysteresis

Event Output Pin Functionality

In Interrupt mode, the $\overline{\text{EVENT}}$ pin will remain asserted until it is released by writing a '1' to the CLEAR bit in the Configuration Register. The value to write is independent of the EVENT_POL bit.

In Comparator mode, the $\overline{\text{EVENT}}$ pin will clear itself when the error condition that caused the pin to be asserted is removed.

In TCRIT Only mode, the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature rises above or equal to the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus TCRIT hysteresis. Figure 12 illustrates the operation of the different modes over time and temperature. Hysteresis will be used to sense temperature movement around trigger points when the HYST1 and HYST0 bits are enabled.

If the device enters the shutdown mode with the $\overline{\text{EVENT}}$ pin asserted, the output will be de-asserted. Once the SHDN bit is cleared, the $\overline{\text{EVENT}}$ pin will remain de-asserted until the first temperature conversion (t_{CONV}) is completed. Then, if in Comparator mode and T_A satisfies the High or Low Limit conditions, the $\overline{\text{EVENT}}$ pin will be asserted; If in Interrupt mode and the CLEAR bit is never set, the $\overline{\text{EVENT}}$ pin will be re-asserted.

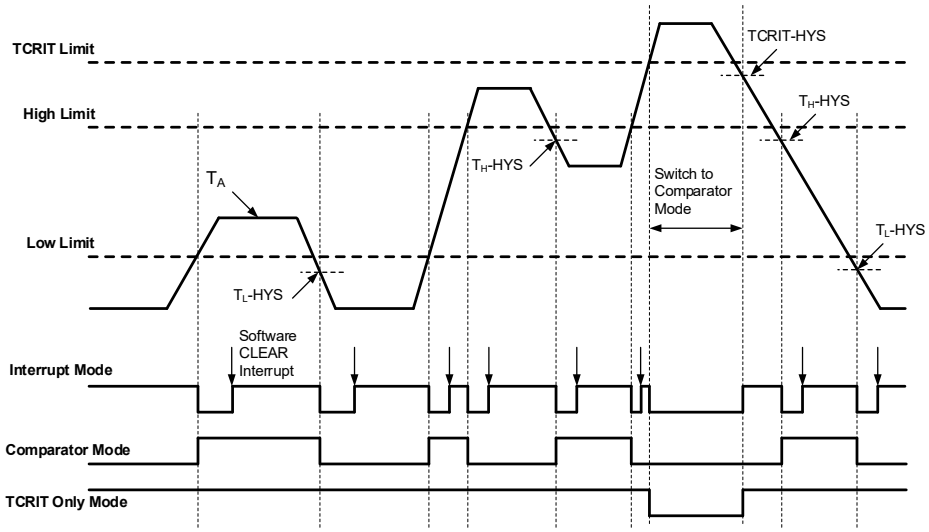


Figure 12. $\overline{\text{EVENT}}$ Output Pin Mode Functionality (EVENT_POL = 0, Active Low)

Systems that use the active high mode for $\overline{\text{EVENT}}$ pin must be wired point-to-point between the TD34TS04 and the sensing controller. Wire-OR configuration should not be used with active high $\overline{\text{EVENT}}$ pin since any device pulling the $\overline{\text{EVENT}}$ signal low will mask the other devices on the bus. Also note that the normal state of $\overline{\text{EVENT}}$ in active high mode is a '0', which will constantly draw power through the pull-up resistor.

TEMPERATURE SENSOR (continued)

Temperature Register Value Definition

Temperatures in the High Limit Register, Low Limit Register, TCRIT Limit Register and Temperature Data Register are expressed in two's complement format. Bit 12 through bit 2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capability Register; hence, a 0.25℃ minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits are shown in Table 9.

Table 9. Temperature Register Coding Examples

BIT 15 ~ BIT 0	VALUE	UNITS
xxx0 0000 0010 11xx	+2.75	℃
xxx0 0000 001 00xx	+1.00	℃
xxx0 0000 0000 01xx	+0.25	℃
xxx0 0000 0000 00xx	0	℃
xxx1 1111 1111 11xx	-0.25	℃
xxx1 1111 1111 00xx	-1.00	℃
xxx1 1111 1101 01xx	-2.75	℃

The TRES[1:0] field of the Capability Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects both the Temperature Data Register and temperature limit registers. When higher resolution devices generate status or $\overline{\text{EVENT}}$ changes, only bit 12 through bit 2 are used in the comparison; however, all 11 bits (TRES[1:0] = 10) or all 12 bits (TRES[1:0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capability Register (TRES[1:0] = 00), the finest resolution supported is 0.5℃. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

REG0x02: High Limit Register

The temperature limit registers (High, Low and TCRIT) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits must be programmed as '0'.

The High Limit Register holds the high limit for the nominal operating window. When the temperature rises above the high limit or drops below or equal to the high limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, then this register becomes Read-Only. Table 10 shows the High Limit Register format.

Table 10. High Limit Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
02h	R/W	-	-	-	Sign	128	64	32	16
		BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		8	4	2	1	0.5	0.25	-	-

REG0x03: Low Limit Register

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the low limit or rises up to meet or exceed the low limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, then this register becomes Read-Only. Table 11 shows the Low Limit Register format.

Table 11. Low Limit Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
03h	R/W	-	-	-	Sign	128	64	32	16
		BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		8	4	2	1	0.5	0.25	-	-

TEMPERATURE SENSOR (continued)

REG0x04: TCRIT Limit Register

The TCRIT Limit Register holds the TCRIT limit. If the temperature rises above or equal to the limit, the $\overline{\text{EVENT}}$ pin will be asserted. It will remain asserted until the temperature drops below the limit minus a hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register, then this register becomes Read-Only. Table 12 shows the TCRIT Limit Register format.

Table 12. TCRIT Limit Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
04h	R/W	-	-	-	Sign	128	64	32	16
		BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		8	4	2	1	0.5	0.25	-	-

REG0x05: Temperature Data Register

The 16-bit Read-Only Temperature Data Register stores the temperature measured by the internal bandgap type temperature sensor, as shown in Table 13. When reading this register, the MSBs (bit 15 to bit 8) are read first, and then the LSBs (bit 7 to bit 0) are read. The result is the current-sensed temperature. The data format is twos complement with one LSB = 0.25℃ for the default resolution.

The upper three bits (bit 15, bit 14 and bit 13) of the Temperature Data Register indicates the trip status of the current temperature, as shown in Table 14, and are not affected by the status of the event or configuration bits. If neither of the above or below values is set, then the temperature is exactly within the user-defined alarm window boundaries.

Table 13. Temperature Data Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
05h	R	TCRIT	HIGH	LOW	Sign	128	64	32	16
		BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		8	4	2	1	0.5	0.25 (1)	0.125 (1)	0.0625 (1)

NOTE: 1. Resolution defined based on the value of TRES[1:0] in the Capability Register. Unused/unsupported bits will read as '0'.

Table 14. Temperature Data Register Bit Definition

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[15]	TCRIT	R	N/A	0 = The temperature is below the TCRIT Limit Register setting. 1 = The temperature is above or equal to the TCRIT Limit Register setting. This bit will remain set so long as the temperature is above or equal to the TCRIT Limit and will automatically clear once the temperature has dropped below the limit minus the hysteresis.
D[14]	HIGH	R	N/A	0 = The temperature is below or equal to the High Limit Register setting. 1 = The temperature is above the High Limit Register setting This bit will remain set so long as the temperature is above the HIGH Limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.
D[13]	LOW	R	N/A	0 = The temperature is above or equal to the Low Limit Register setting 1 = The temperature is below the Low Limit Register setting This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.
D[12]	Sign	R	N/A	Sign bit: 0 = The temperature is greater than or equal to 0℃. 1 = The temperature is less than 0℃.
D[11:0]	TEMP[11:0]	R	N/A	Temperature bits: The encoding of bit 11 through bit 0 is the same as for the temperature limit registers.

TEMPERATURE SENSOR (continued)

REG0x06: Manufacturer ID Register

The Manufacturer ID Register holds the number 104Ah as shown in Table 15.

Table 15. Manufacturer ID Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
06h	R	0	0	0	1	0	0	0	0
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		0	1	0	0	1	0	1	0

REG0x07: Device ID/Revision Register

The upper byte of the Device ID/Revision Register is the Device ID and must be 0x22 for the TD34TS04. The lower byte holds the revision value which is 0x01 for the current device. Table 16 shows the Device ID/Revision Register format.

Table 16. Device ID/Revision Register Format

ADDRESS	TYPE	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
07h	R	0	0	1	0	0	0	1	0
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		0	0	0	0	0	0	0	1

REG0x08: Temperature Resolution Register

With the Temperature Resolution Register, a user can program the temperature sensor resolution from 9-12 bits. The power-on default is always 10-bit (0.25℃/LSB). The selected resolution RES[1:0] is also reflected in bit 4 and bit 3 (TRES[1:0]) of the Capability Register. Table 17 shows the Temperature Resolution Register format and bit definition.

Table 17. Temperature Resolution Register Bit Definition

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[15:2]	Reserved	R/W	000h	Reserved
D[1:0]	RES[1:0]	R/W	01	Temperature Resolution: 00 = 9-bit, 0.5℃/LSB 01 = 10-bit, 0.25℃/LSB (default) 10 = 11-bit, 0.125℃/LSB 11 = 12-bit, 0.0625℃/LSB

REG0x09: SMBus Timeout Register

The SMBus Timeout Register allows the user to enable or disable the SMBus timeout feature. Bit。7, SMBOUT as shown in Table 18, configures the SMBus Timeout function. When the SMBOUT is set to '1', the SMBus Timeout function is active. If the SMBOUT is set to '0', the SMBus Timeout is disabled. Other bits of this register are reserved for future use and will always read as '0'. The power-on default value of SMBOUT is '1'. The SMBOUT is also reflected in bit 6 (TMOUT) of the Capability Register.

Table 18. SMBus Timeout Register Bit Definition

BITS	BIT NAME	TYPE	DEFAULT	DESCRIPTION
D[15:8]	Reserved	R/W	00h	Reserved
D[7]	SMBOUT	R/W	1	SMBus Timeout status: 0 = the SMBus Timeout is disabled 1 = The SMBus Timeout function is active (default)
D[6:0]	Reserved	R/W	00h	Reserved

SPD EEPROM

Memory Organization

To provide great flexibility and backwards compatibility with the previous generations of SPD devices, the TD34TS04 memory is organized into two independent 2-Kbit memory arrays (Page 0 and Page 1). Each 2-Kbit (256-byte) array is internally organized as two independent blocks of 128 bytes with each block comprised of eight pages of 16 bytes. Including both memory Pages, there are four 128-byte blocks totaling 512 bytes (see Table 20).

The TD34TS04 utilizes a Set Page Address (SPA) command and Read Page Address (RPA) command to select and verify the desired half of the memory for Write and Read operations. If SPA = 0, the lower 256 bytes (Page 0) of the EEPROM is selected allowing access to Block 0 and Block 1. Alternately, if SPA = 1, the upper 256 bytes (Page 1) of the EEPROM is selected allowing access to Block 2 and Block 3.

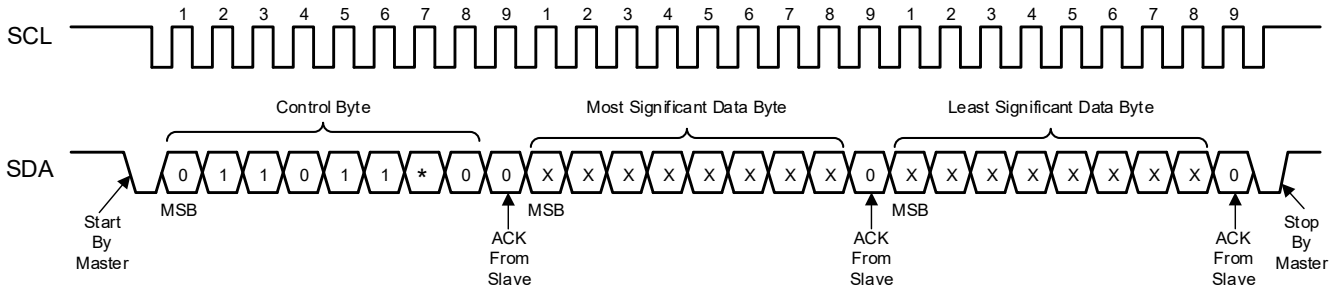
Table 19. SPA Setting and Memory Organization

BLOCKS	SET PAGE ADDRESS (SPA)	MEMORY ADDRESS LOCATIONS
Block 0	0	00h to 7Fh (decimal 0 to 127)
Block 1	0	80h to FFh (decimal 128 to 255)
Block 2	1	00h to 7Fh (decimal 0 to 127)
Block 3	1	80h to FFh (decimal 128 to 255)

Set Page Address Command

Setting the SPA value selects the desired half of the SPD EEPROM for Write or Read operation. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of ‘01101100’ or ‘01101110’. ‘0’ in the bit 7 position indicates setting the page address to the lower half of the memory while ‘1’ in this position indicates setting the page address to the upper half of the memory. After receiving the control byte, the TD34TS04 should return an ACK and the Master follows by sending two data bytes of Don’t Care values. The TD34TS04 responds with an ACK to each of the two data bytes although the JEDEC TSE2004av specification allows for either an ACK or an NACK response (see Figure 13). The protocol is completed by the Master sending a Stop condition.

After power-up, the SPA is set to zero, indicating internal address counter is located in the lower half of the memory. Performing software reset will not change the SPA setting.



X = Do not care value

Bit * = 0: Indicates the page address is located in the lower half of the memory.

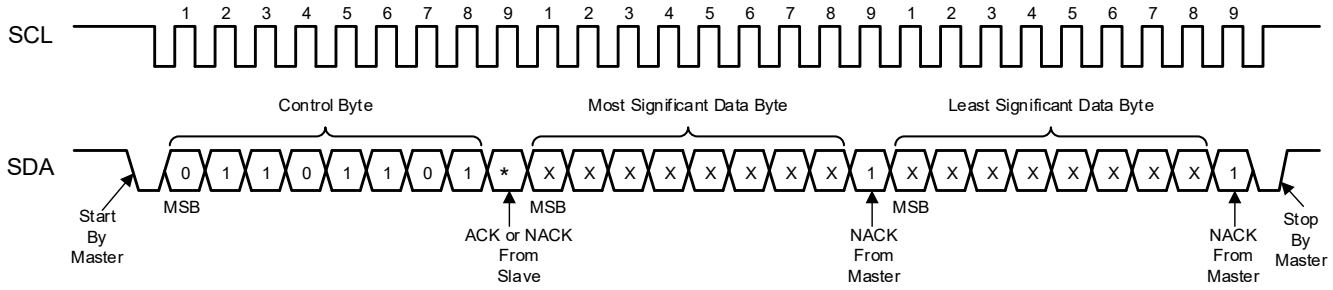
Bit * = 1: Indicates the page address is located in the upper half of the memory.

Figure 13. Set Page Address (SPA)

SPD EEPROM (continued)

Read Page Address Command

Reading the state of the SPA can be accomplished by the RPA command. The RPA command sequence requires the Master to transmit a Start condition followed by a control byte of '01101101'. The Master determines if the internal address counter is located in the lower half or upper half of the memory based on the device's ACK or NACK response. If the device's current address counter is located in the lower half of the memory, the TD34TS04 will respond with an ACK. Alternatively, an NACK response indicates the address counter is located in the upper half of the memory (see Figure 14). Following the ACK or NACK response, the TD34TS04 transmits two data bytes of Don't Care values. The Master should respond with an NACK on each of the two data bytes followed by sending a Stop condition to end the operation.



X = Do not care value

Bit * = 0: ACK indicates the device's internal address counter is located in the lower half of the memory.

Bit * = 1: NACK indicates the device's internal address counter is located in the upper half of the memory.

Figure 14. Read Page Address (RPA)

Write Operations

The TD34TS04 supports single Byte Write and Page Write up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

If a Byte Write or Page Write operation is attempted to a Write Protected or not protected block, the TD34TS04 will respond with ACK or NACK to the write operation according to Table 21.

Table 20. Acknowledge Status When Writing Data or Defining Write Protection

BLOCK STATUS	INSTRUCTION	ACK	WORD ADDRESS	ACK	DATA WORD	ACK	WRITE CYCLE
Write Protected	SWPn	NACK	Don't Care	NACK	Don't Care	NACK	No
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	NACK	No
Not Protected	SWPn	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

SPD EEPROM (continued)

Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The TD34TS04 responds with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the SPD EEPROM. After receiving an ACK from the TD34TS04, the Master transmits the data word to be programmed followed by an ACK from the TD34TS04. The Master ends the Write sequence with a Stop condition during the 10th clock cycle (see Figure 15) to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle.

Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the t_{WR} specification. During the time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is complete (see Figure 17). The SPD EEPROM will increment its internal address counter each time a byte is written.

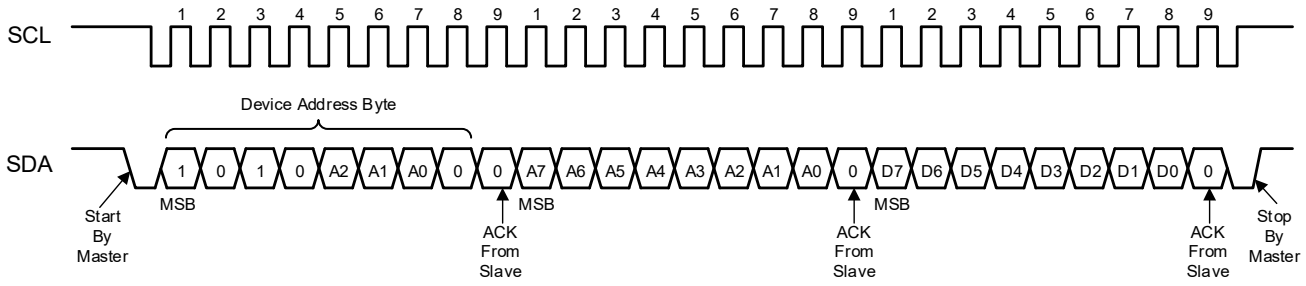


Figure 15. Byte Write

Page Write

The 4-Kbit SPD EEPROM is capable of writing up to 16 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to fifteen more data words. The device will respond with an ACK after each data word is received (see Figure 16). After the device acknowledges to the last data word, the Master should terminate the Page Write sequence with a Stop condition to start the internal write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the t_{WR} specification (see Figure 17). During this time, the Master should wait a fixed time by the specified t_{WR} parameter, or for time sensitive applications, an ACK polling routine can be implemented.

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than sixteen data words are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

SPD EEPROM (continued)

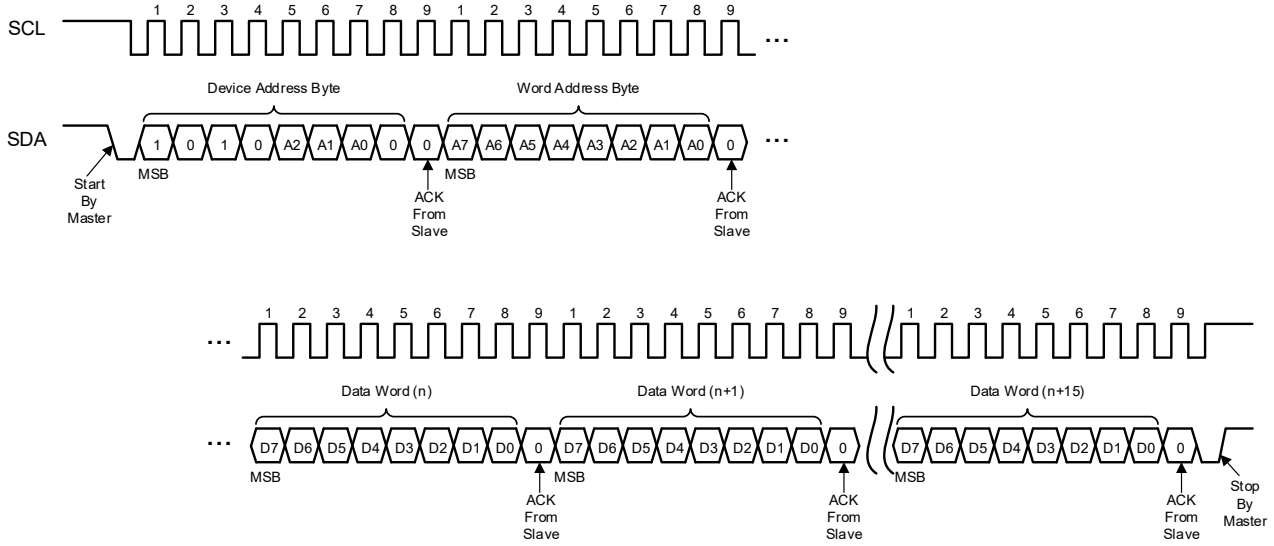


Figure 16. Page Write

Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the TD34TS04 that it subsequently responds with an ACK (see Figure 17).

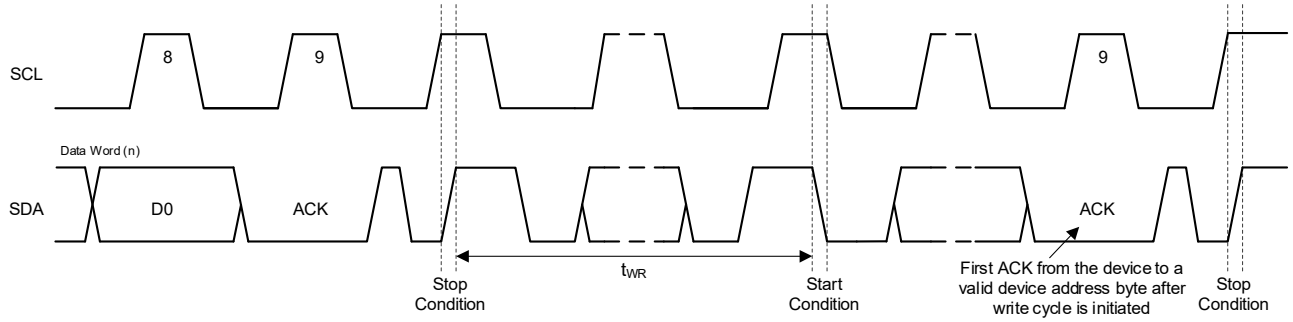


Figure 17. Write Cycle Timing

SPD EEPROM (continued)

Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the SPD EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see Figure 18).

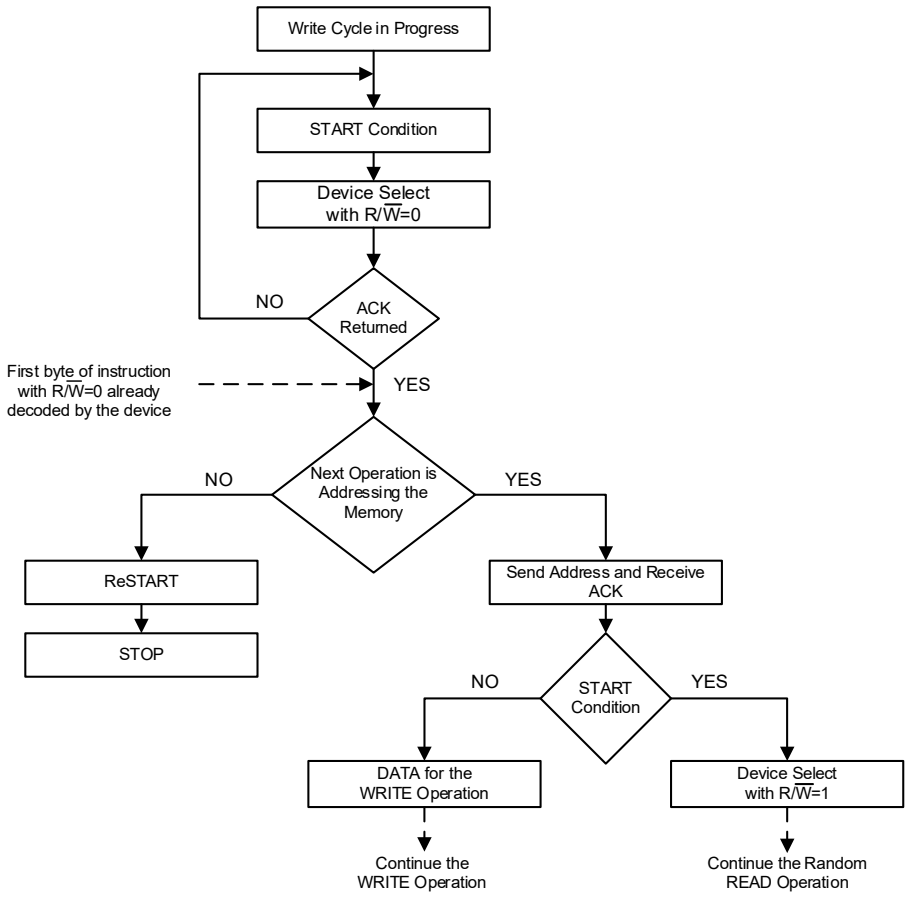


Figure 18. Acknowledge Polling Flow Chart

SPD EEPROM (continued)

Read Operations

All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of '1010', three software address bits (A2, A1, A0) corresponding to the hard-wired address pins (SA2, SA1, SA0) and the R/$\overline{W}$ select bit with Logic 1 state. In the following clock cycle, the TD34TS04 should return an ACK. The subsequent sequence depends on the Read operation type. There are three Read operations: Current Address Read, Random Address Read, and Sequential Read.

Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/$\overline{W}$ bit set to Logic 1 (see Figure 19). The TD34TS04 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last memory page to the first byte of the first page. To end the command, the Master responds with an NACK and a Stop condition.

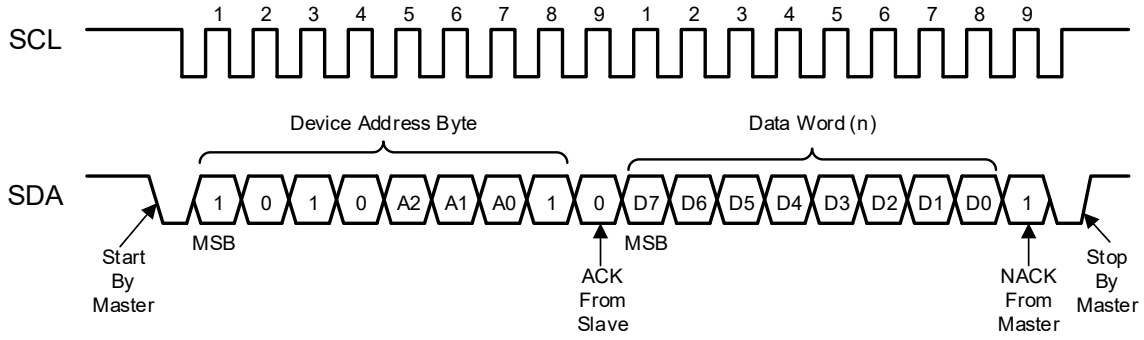


Figure 19. Current Address Read

Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to the TD34TS04 as part of the dummy write sequence (see Figure 20). Once the device address byte and data word address are clocked in and acknowledged by the TD34TS04, the Master generates another Start condition and then initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The TD34TS04 responds with an ACK to the device address byte and serially clocks out the first data word and increments its internal address counter by one. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with an NACK followed by a Stop condition.

SPD EEPROM (continued)

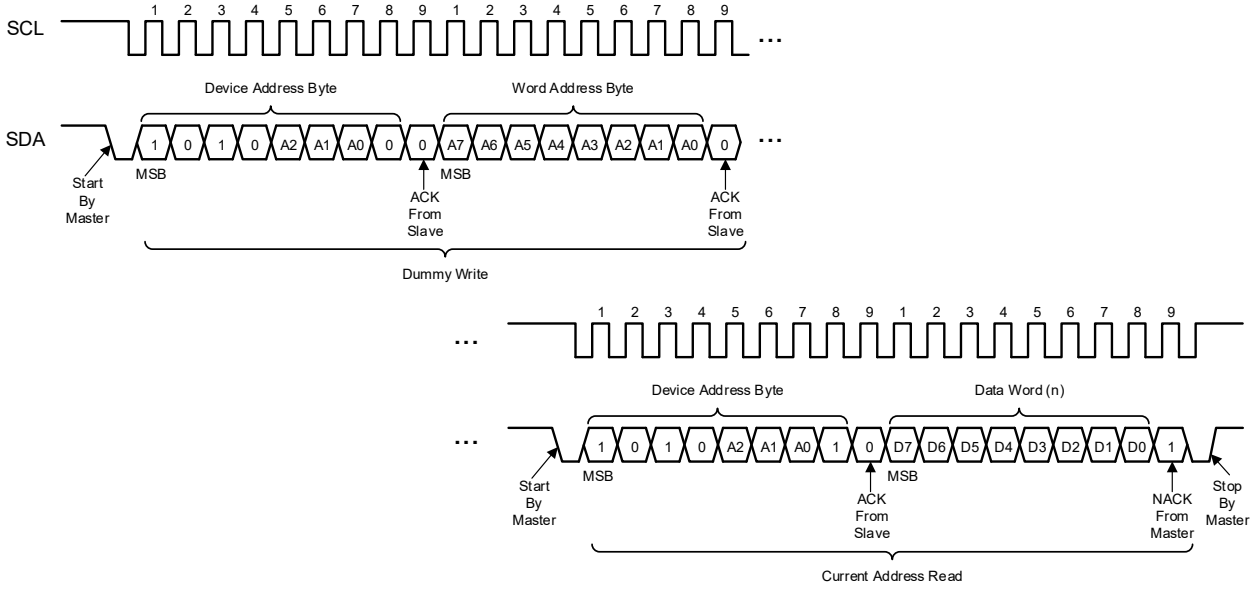


Figure 20. Random Read

Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after transmitted the first data word by the TD34TS04, the Master responds with an ACK instead of an NACK. As long as the TD34TS04 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see Figure 21). When the internal address counter is at the last byte of the last page, the data word address will roll-over to the first byte of the first page and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with an NACK followed by a Stop condition.

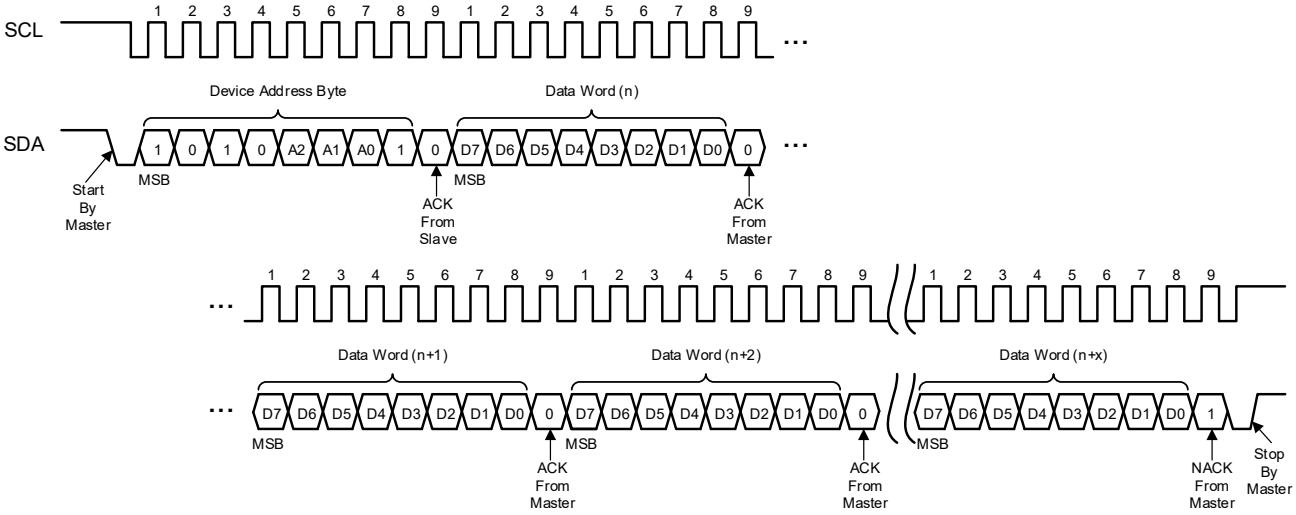


Figure 21. Sequential Read

SPD EEPROM (continued)

Write Protection

The TD34TS04 has three software commands for setting, clearing, or checking the write protection:

1. SWPn: Set Write Protection for Block n.

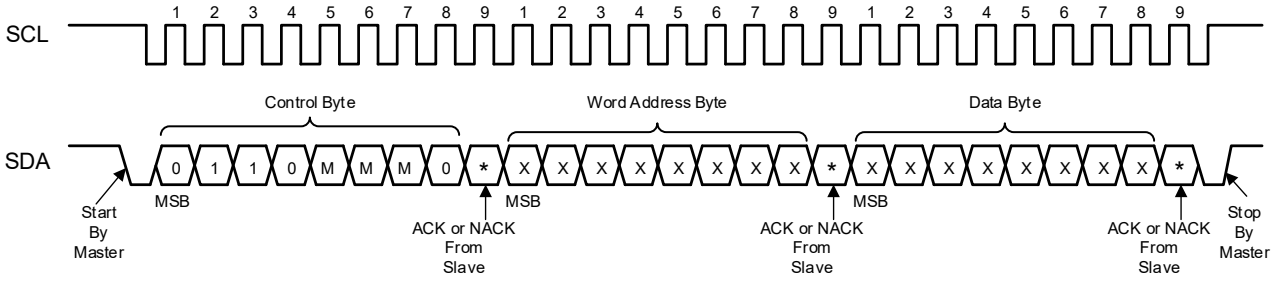
2. CWP: Clear Write Protection for all blocks to an unprotected state.

3. RPSn: Read the Protection Status of Block n.

The Software Write Protection feature allows the ability of selective write protection data stored in each of the four independent 128-byte blocks.

Set Write Protection

Setting the Write Protection is enabled by sending the Set Write Protection (SWPn) command to the target Block n. The SWPn sequence requires the Master to send a control byte of ‘0110MMM0’ (where ‘M’ represents the memory address identifier for the block to be write-protected, see Table 24) with the R/$\overline{W}$ bit set to Logic 0. If the target block has not been write-protected, the TD34TS04 responds with an ACK to the control byte. If Software Write Protection has been already set to the target block, the TD34TS04 responds with an NACK (see Table 23). Then the Master transmits a word address byte and a data byte with Don’t Care values followed by the TD34TS04 responds to each of the word address byte and the data byte with an ACK or an NACK corresponding to the response on the control byte. To end the SWPn sequence, the Master sends a Stop condition (see Figure 22). In conjunction with sending the protocol, the SA0 pin must be connected to V_{HV} for the duration of the SWPn sequence. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the TD34TS04.



M = Memory Address Identifier

X = Do not care value

Bit * = 0: ACK indicates Software Write Protection has not been set to target block.

Bit * = 1: NACK indicates Software Write Protection has been set to target block.

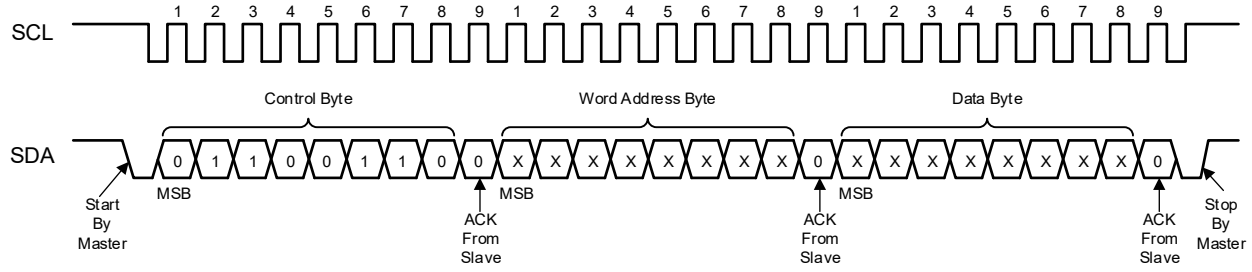
Figure 22. Set Write Protection

SPD EEPROM (continued)

Clear Write Protection

The Write Protection status on all blocks can be reversed by transmitting the Clear Write Protection (CWP) command. The CWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110' with the R/$\overline{W}$ select bit set to Logic 0. The TD34TS04 should respond with an ACK. Then the Master transmits a word address byte and a data byte with Don't Care values followed by the TD34TS04 responds with an ACK to each of the word address byte and the data byte. To end the CWP sequence, the Master sends a Stop condition (see Figure 23). In conjunction with sending the protocol, the SA0 pin must be connected to V_{HV} for the duration of CWP command. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the TD34TS04.

The SWPn acts on a single block only as specified in the SWPn command and can only be reversed by issuing the CWP command and will unprotect all blocks in one operation (see Table 24). For example, if both Block 0 and Block 3 are needed to be write-protected, two separate SWP0 and SWP3 commands should be required; however, only one CWP command is needed to clear the write protection status of both blocks.



X = Do not care value

Figure 23. Clear Write Protection

Table 21. SWPn, CWP and RPSn

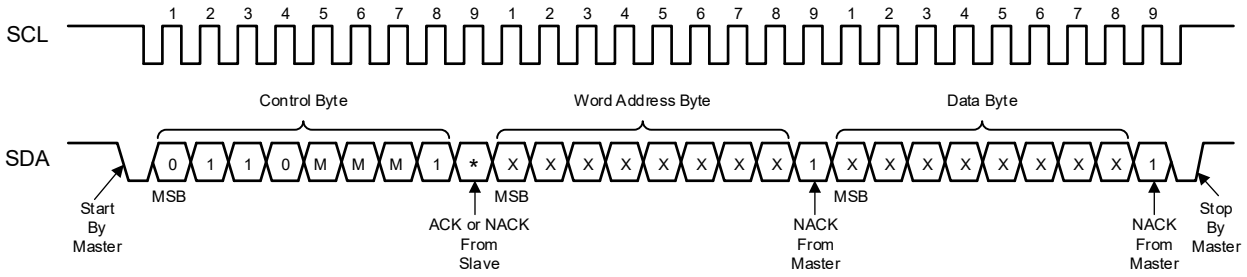
FUNCTION	PIN			CONTROL BYTE							
				DEVICE TYPE IDENTIFIER				MEMORY ADDRESS IDENTIFIER			R/W
	SA2	SA1	SA0	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Set Write Protection, Block 0	X (1)	X	V_{HV} (2)	0	1	1	0	0	0	1	0
Set Write Protection, Block 1	X	X						1	0	0	0
Set Write Protection, Block 2	X	X						1	0	1	0
Set Write Protection, Block 3	X	X						0	0	0	0
Clear All Write Protection	X	X						0	1	1	0
Read Protection Status, Block 0	X	X	0, 1 or V_{HV}	0	1	1	0	0	0	1	1
Read Protection Status, Block 1	X	X						1	0	0	1
Read Protection Status, Block 2	X	X						1	0	1	1
Read Protection Status, Block 3	X	X						0	0	0	1

NOTES:
1. X = Don't care but recommended to be hard-wired to V_{CC} or GND.
2. See **DC Characteristics** for V_{HV} value.

SPD EEPROM (continued)

Read Protection Status

The Read Protection Status (RPSn) command allows the ability to check a block's write protection status. To find out if the Software Write Protection has been set to a specific Block n, the same procedure used to set the block's write protection can be utilized except that the R/$\overline{W}$ select bit is set to Logic 1, and the SA0 pin is not required to be connected to V_{HV}. The RPSn sequence requires the master to send a control byte of '0110MMM1' (where 'M' represents the memory address identifier for the block to be read) with the R/$\overline{W}$ bit set to Logic 1 (see Table 24). If Software Write Protection has not been set to the target block, the TD34TS04 responds to the control byte with an ACK. Alternately, If Software Write Protection has been set, the TD34TS04 responds with an NACK. In either case, neither the word address byte nor the data byte with Don't Care values will be acknowledged (see Figure 24). The operation is completed by the Master creating a Stop condition.



M = Memory Address Identifier

X = Do not care value

Bit * = 0: ACK indicates Software Write Protection has not been set.

Bit * = 1: NACK indicates Software Write Protection has been set.

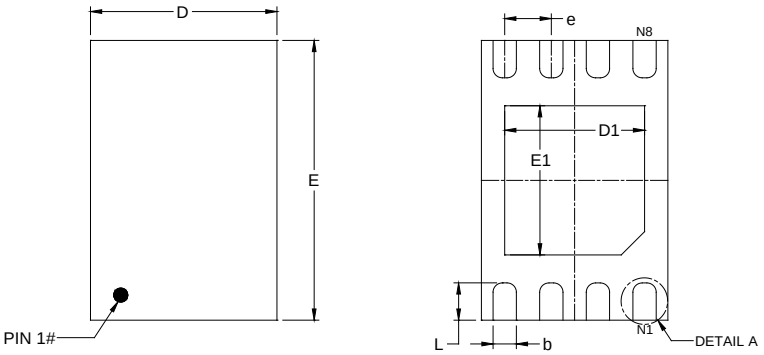
Figure 24. Read Protection Status

REVISION HISTORY

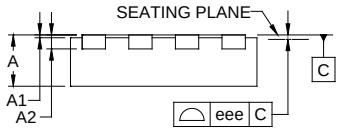
REVISION	DATE	COMMENTS
REV.A	Jan. 2022	Initial version release
REV.A.1	Oct. 2026	Updated: — Package Outline Dimensions Added: — N_W at T_A = +125℃, Page mode — Tape and Reel Information

PACKAGE OUTLINE DIMENSIONS

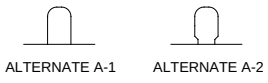
UTDFN-2×3-8AL



TOP VIEW **BOTTOM VIEW**

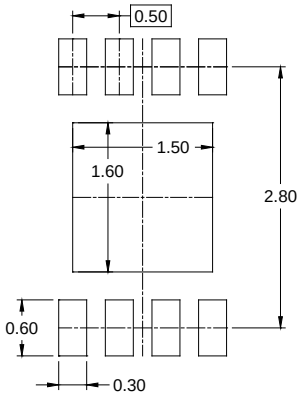


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



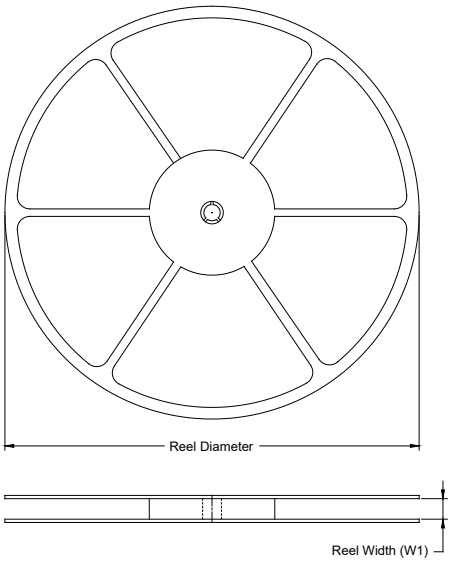
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.150 REF		
b	0.180	-	0.300
D	1.900	-	2.100
D1	1.400	-	1.600
E	2.900	-	3.100
E1	1.500	-	1.700
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

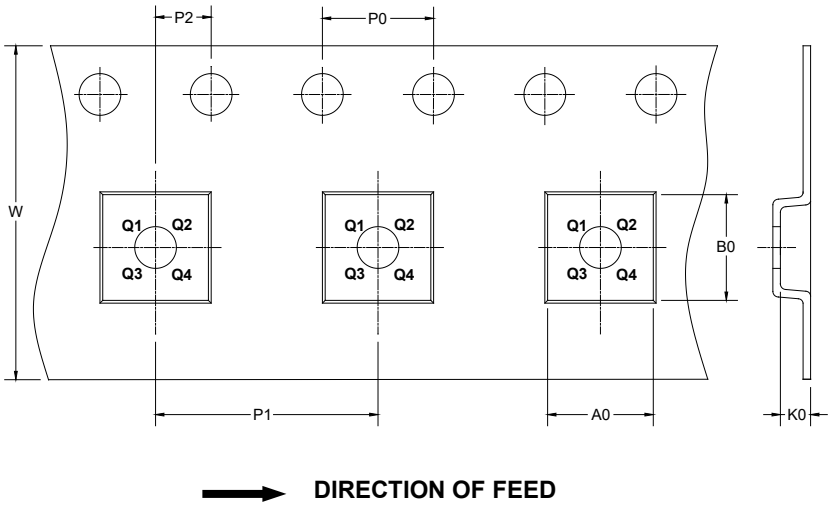
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



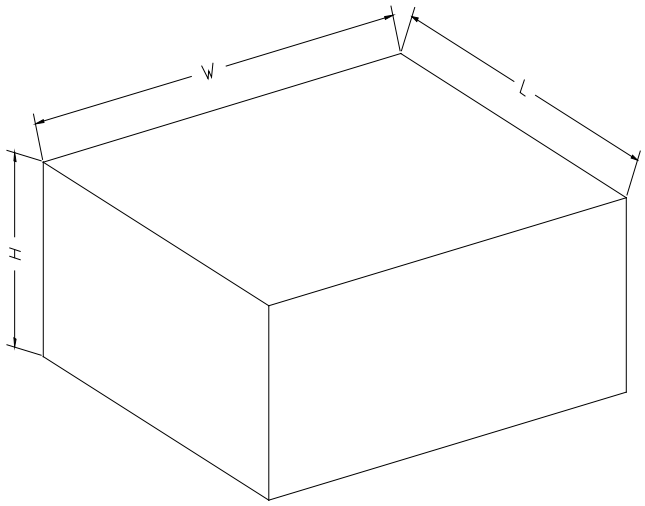
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-2×3-8AL	7"	9.5	2.30	3.30	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002