SGM25703

60V, 800mA with Integrated Reverse Input and Output Polarity Protection Industrial eFuse

GENERAL DESCRIPTION

The SGM25703 device is a compact and feature-rich high-voltage eFuse family, which offers comprehensive protection features. With a broad supply input range of 4.5V to 60V, it is suitable for controlling a variety of common DC bus voltages. The device can handle and protect loads from ±60V negative and positive supply voltages. The device supports reverse polarity protection on both the input and output. Reverse current blocking is allowed by the integrated back-to-back MOSFETs, so if the systems require output voltage hold-up during power failures and brownout conditions, the device is an ideal choice. It offers source, device, and load protection with numerous adjustable features, including over-current protection, output slew rate control, and over-voltage and under-voltage thresholds. The SGM25703 incorporates strong internal protection control blocks and a high-voltage rating, making it easier to design systems with effective surge protection.

The SGM25703A/SGM25703C feature latch-off and SGM25703B/SGM25703D feature auto-retry functionality, which are the over-temperature and over-current fault events.

The SGM25703 is available in a Green TDFN-3×3-10AL package.

TYPICAL APPLICATION

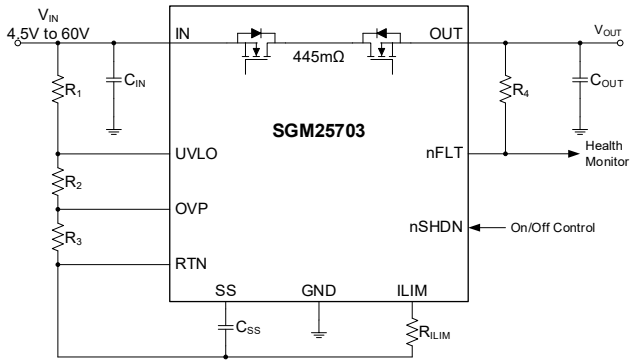


Figure 1. Typical Application Circuit

FEATURES

- **4.5V to 60V Operating Voltage, 62V Absolute Maximum**
- **Up to -60V Integrated Reverse Input Polarity Protection**
- **Up to -(60V - V_{IN}) Integrated Reverse Output Polarity Protection**
- **Integrated Back-to-Back MOSFETs Total On-Resistance (R_{ON}): 445mΩ**
- **Adjustable Current Limit: 25mA to 880mA (±4.2% Accuracy at 880mA)**
- **Load Protection during Surge (IEC 61000-4-5) with Minimum External Components**
- **Electrical Fast Transients Immunity (IEC 61000-4-4)**
- **Fast Reverse Current Blocking Response**
- **Adjustable UVLO, OVP, Output Slew Rate Control for Inrush Current Control**
- **Fixed 38V Over-Voltage Clamp (SGM25703C and SGM25703D Only)**
- **Low Quiescent Current, 197μA in Operating, 16.5μA in Shutdown**
- **Available in a Green TDFN-3×3-10AL Package**

APPLICATIONS

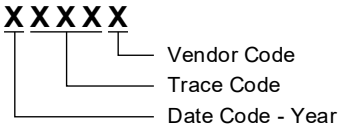
PLC I/O Modules
AC and Servo Drives
Sensor and Controls
Thermostat
PoE High-side Protection

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25703A	TDFN-3×3-10AL	-40℃ to +125℃	SGM25703AXTGZ10G/TR	SGM 2N6GZ XXXXX	Tape and Reel, 4000
SGM25703B	TDFN-3×3-10AL	-40℃ to +125℃	SGM25703BXTGZ10G/TR	SGM 2VHGZ XXXXX	Tape and Reel, 4000
SGM25703C	TDFN-3×3-10AL	-40℃ to +125℃	SGM25703CXTGZ10G/TR	SGM 2VIGZ XXXXX	Tape and Reel, 4000
SGM25703D	TDFN-3×3-10AL	-40℃ to +125℃	SGM25703DXTGZ10G/TR	SGM 28SGZ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE COMPARISON TABLE

Part Number	Over-Voltage Protection	Overload and Thermal Fault Response
SGM25703A	Over-Voltage Cut-Off, Adjustable	Latch-Off
SGM25703B	Over-Voltage Cut-Off, Adjustable	Auto-Retry
SGM25703C	Over-Voltage Clamp, Fixed (38V)	Latch-Off
SGM25703D	Over-Voltage Clamp, Fixed (38V)	Auto-Retry

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- IN, IN - OUT ..... -60V to 62V
- OUT ..... -(60 - V_{IN})V to 62V
- IN, IN - OUT (10ms Transient), T_A = +25℃ ..... -70V to 70V
- IN, OUT, nFLT, nSHDN to RTN ..... -0.3V to 62V
- UVLO, OVP, SS, ILIM to RTN ..... -0.3V to 5V
- RTN ..... -60V to 0.3V

Sink Current, I_{nFLT}, I_{SS} 10mA

Source Current, I_{SS}, I_{ILIM}, I_{nSHDN} ..... Internally Limited

Package Thermal Resistance
- TDFN-3×3-10AL, θ_{JA} ..... 37.3℃/W
- TDFN-3×3-10AL, θ_{JB} ..... 12.2℃/W
- TDFN-3×3-10AL, $\theta_{JC\ (TOP)}$ ..... 36.4℃/W
- TDFN-3×3-10AL, $\theta_{JC\ (BOT)}$ ..... 1.8℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±4000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range
- IN ..... 4.5V to 60V
- OUT, nFLT ..... 0V to 60V
- UVLO, OVP, SS, ILIM ..... 0V to 4V
- nSHDN ..... 0V to 6V

Resistance, ILIM ..... 7.5kΩ to 267kΩ

External Capacitance
- IN, OUT ..... 0.01μF (MIN)
- SS ..... 6.8nF (MIN)

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

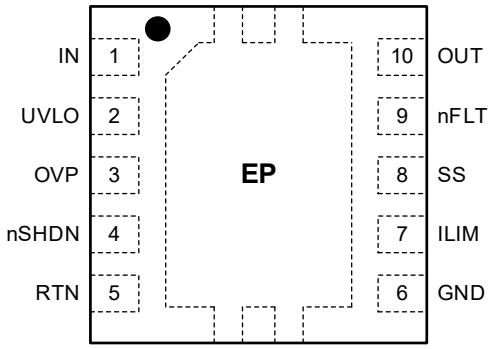
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM25703 (TOP VIEW)



TDFN-3×3-10AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	IN	P	Power Input and Supply Voltage.
2	UVLO	I	Under-Voltage Lockout. This input provides a resistor-programmable under-voltage lockout threshold. When an under-voltage condition occurs, the internal FET is turned off.
3	OVP	I	Over-Voltage Protection. This input provides a resistor-programmable over-voltage protection threshold. When an over-voltage event occurs, it turns off the internal FET. To disable this protection on the SGM25703A and SGM25703B, connect the OVP pin to RTN. For over-voltage clamp response (SGM25703C and SGM25703D only), also connect the OVP pin to the RTN pin externally.
4	nSHDN	I	Shutdown Pin. Pulling the nSHDN pin low switches the device into low power shutdown mode. Cycle this pin will reset the device after it has latched off as a result of a fault (SGM25703A and SGM25703C only).
5	RTN	—	Device Internal Control Circuits Reference.
6	GND	—	Connect to System Ground.
7	ILIM	I/O	Programming Current Limit Pin. This pin sets the overload and short-circuit current limit by connecting a resistor to RTN.
8	SS	I/O	Soft-Start Pin. Place a capacitor from this pin to RTN to set the output voltage slew rate.
9	nFLT	O	Fault Event Indicator. This pin is an open-drain output and should be left floating when not in use.
10	OUT	P	Power Output of the Device.
Exposed Pad	EP	—	Connect it to RTN for Heat Sinking. This pin cannot be used as the sole electrical connection to RTN.

NOTE: I = input, O = output, I/O = input/output, P = power.

ELECTRICAL CHARACTERISTICS

(-40℃ ≤ T_J ≤ +125℃, V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 267kΩ, nFLT = open, C_{OUT} = 1μF, and C_{SS} = open. All voltages referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Operating Input Voltage	V_{IN}		4.5		60	V
Internal POR Threshold, Rising	V_{PORR}		3.62	3.79	3.96	V
Internal POR Hysteresis	V_{PORHYS}			88		mV
Supply Current	I_{Q_ON}	Enabled: V_{nSHDN} = 2V		197	325	μA
	I_{Q_OFF}	V_{nSHDN} = 0V		16.5	35	μA
Reverse Input Supply Current	I_{VINR}	V_{IN} = -24V, V_{OUT} = 0V		15	26	μA
Over-Voltage Clamp	V_{OVC}	V_{IN} > 40V, I_{LOAD} = 10mA, SGM25703C, SGM25703D only	36	37.5	39	V
Under-Voltage Lockout (UVLO) Input						
UVLO Threshold, Rising	V_{UVLOR}		1.161	1.196	1.231	V
UVLO Threshold, Falling	V_{UVLOF}		1.06	1.095	1.13	V
UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to 4V	-150	10	150	nA
Over-Voltage Protection (OVP) Input						
Over-Voltage Threshold, Rising	V_{OVPR}		1.161	1.196	1.231	V
Over-Voltage Threshold, Falling	V_{OVPF}		1.06	1.095	1.13	V
OVP Input Leakage Current	I_{OVP}	V_{OVP} = 0V to 4V	-120	10	120	nA
Low I_Q Shutdown (nSHDN) Input						
Output Voltage	V_{nSHDN}	I_{nSHDN} = 0.1μA	3	3.55	4.1	V
nSHDN Threshold Voltage for Low I_Q Shutdown, Falling	V_{SHUTF}				0.7	V
nSHDN Threshold, Rising	V_{SHUTR}		1.5			V
Leakage Current	I_{nSHDN}	V_{nSHDN} = 0V	-5.8	-2.3		μA
Output Ramp Control (SS)						
SS Charging Current	I_{SS}	V_{SS} = 0V	1.32	1.96	2.6	μA
SS Discharging Resistance	R_{SS}	V_{nSHDN} = 0V, with I_{SS} = 10mA sinking		14	22	Ω
SS Maximum Capacitor Voltage	V_{SS_MAX}		4.27	4.5	4.73	V
SS to OUT Gain	$GAIN_{SS}$	V_{OUT}/V_{SS}	23.88	24.65	25.42	V/V
Current Limit Programming (ILIM)						
ILIM Bias Voltage	V_{ILIM}			1		V
Overload Current Limit	I_{OL}	R_{ILIM} = 267kΩ, V_{IN} - V_{OUT} = 1V	0.02	0.025	0.032	A
		R_{ILIM} = 44.2kΩ, V_{IN} - V_{OUT} = 1V	0.144	0.152	0.16	
		R_{ILIM} = 26.7kΩ, V_{IN} - V_{OUT} = 1V	0.238	0.25	0.262	
		R_{ILIM} = 13.3kΩ, V_{IN} - V_{OUT} = 1V	0.475	0.5	0.519	
		R_{ILIM} = 8.25kΩ, V_{IN} - V_{OUT} = 1V	0.766	0.8	0.834	
		R_{ILIM} = 7.5kΩ, V_{IN} - V_{OUT} = 1V	0.843	0.88	0.917	
	$I_{OL\_R\text{-}OPEN}$	R_{ILIM} = open, open resistor current limit	9	20.5	32	mA
	$I_{OL\_R\text{-}SHORT}$	R_{ILIM} = short, shorted resistor current limit	27	45	63	mA
Short-Circuit Current Limit	I_{SCL}	R_{ILIM} = 7.5kΩ, V_{IN} - V_{OUT} = 24V		0.88		A
Fast-Trip Comparator Threshold	$I_{FAST\text{-}TRIP}$			1.6		A

ELECTRICAL CHARACTERISTICS (continued)

(-40℃ ≤ T_J ≤ +125℃, V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 267kΩ, nFLT = open, C_{OUT} = 1μF, and C_{SS} = open. All voltages referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pass FET Output (OUT)						
On-Resistance	R_{ON}	I_{OUT} = 0.025A to 0.8A, T_J = +25℃	378	445	510	mΩ
		I_{OUT} = 0.025A to 0.8A, -40℃ ≤ T_J ≤ +85℃			685	
		I_{OUT} = 0.025A to 0.8A, -40℃ ≤ T_J ≤ +125℃	210	445	800	
OUT Leakage Current in Off-State	I_{LKG_OUT}	V_{IN} = 60V, V_{nSHDN} = 0V, V_{OUT} = 0V, sourcing		0.05	0.9	μA
		V_{IN} = 0V, V_{nSHDN} = 0V, V_{OUT} = 24V, sinking		13	25	
		V_{IN} = -60V, V_{nSHDN} = 0V, V_{OUT} = 0V, sinking		21	37	
OUT Leakage Current under Output Reverse Polarity Condition		V_{IN} = 24V, V_{nSHDN} = 2V, V_{OUT} = -24V, sourcing		90		
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Falling	V_{REVTH}		-71	-55	-39	mV
V_{IN} - V_{OUT} Threshold for Reverse Protection Comparator, Rising	V_{FWDTH}		1	17	36	mV
FAULT FLAG (nFLT): Active-Low						
nFLT Pull-Down Resistance	R_{nFLT}	V_{UVLO} = 0.5V, I_{nFLT} = 10mA sinking	43	83	133	Ω
nFLT Input Leakage Current	I_{nFLT}	V_{nFLT} = 0V to 60V	-350	40	350	nA
Thermal Shutdown (TSD)						
TSD Threshold, Rising	T_{SD}			160		℃
TSD Hysteresis	T_{HYS}			10		℃
MODE						
Thermal Fault		SGM25703A, SGM25703C		Latch		
		SGM25703B, SGM25703D		Auto-Retry		

TIMING REQUIREMENTS

(-40℃ ≤ T_J ≤ +125℃, V_{IN} = 24V, V_{nSHDN} = 2V, R_{ILIM} = 267kΩ, nFLT = open, C_{OUT} = 1μF, and C_{SS} = open. All voltages referenced to GND, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN and UVLO Input						
UVLO Turn-On Delay	$t_{UVLO\_ON\_DLY}$	UVLO↑ (100mV above V_{UVLOR}) to V_{OUT} = 100mV, C_{SS} = open		51		μs
		UVLO↑ (100mV above V_{UVLOR}) to V_{OUT} = 100mV, C_{SS} > 4.7nF, C_{SS} in nF		51 + 39 × C_{SS}		μs
UVLO Turn-Off Delay	$t_{UVLO\_OFF\_DLY}$	UVLO↓ (100mV below V_{UVLOF}) to nFLT↓		5.5		μs
Shutdown Control Input (nSHDN)						
Shutdown Exit Delay	$t_{SD\_ON\_DLY}$	nSHDN↑ to V_{OUT} = 100mV, C_{SS} = open		156		μs
		nSHDN↑ to V_{OUT} = 100mV, C_{SS} > 4.7nF, C_{SS} in nF		156 + 39 × C_{SS}		μs
Shutdown Entry Delay	$t_{SD\_OFF\_DLY}$	nSHDN↓ (below SHUTF) to nFLT↓		1.35		μs
Over-Voltage Protection Input (OVP)						
OVP Exit Delay	$t_{OVP\_ON\_DLY}$	OVP↓ (20mV below V_{OVPF}) to V_{OUT} = 100mV, SGM25703A/B only		55		μs
OVP Disable Delay	$t_{OVP\_OFF\_DLY}$	OVP↑ (20mV above V_{OVPR}) to nFLT↓, SGM25703A/B only		3.9		μs
Current Limit						
Maximum Duration in Current Limit	t_{CL_DLY}	I_{ILIM} < I_{OUT} < $I_{FAST-TRIP}$		512		ms
Fast-Trip Comparator Delay	$t_{FAST-TRIP\_DLY}$ (1)	I_{OUT} > $I_{FAST-TRIP}$		200		ns
Reverse Protection Comparator						
Reverse Protection Comparator Delay	t_{REV_DLY} (1)	(V_{IN} - V_{OUT})↓ (10mV overdrive below V_{REVTH}) to internal FET turn off		1.2		μs
		(V_{IN} - V_{OUT})↓ (1V overdrive below V_{REVTH}) to internal FET turn off		0.34		
		(V_{IN} - V_{OUT})↓ (150mV overdrive below V_{REVTH}) to nFLT↓		45		
	t_{FWD_DLY}	(V_{IN} - V_{OUT})↑ (100mV overdrive above V_{FWDTH}) to nFLT↑		63		
Thermal Shutdown						
Retry Delay in TSD				512		ms
Output Ramp Control (SS)						
Output Ramp Time	t_{SS}	nSHDN↑ to V_{OUT} = 23.9V, with C_{SS} = 22nF		11.7		ms
		nSHDN↑ to V_{OUT} = 23.9V, with C_{SS} = open		0.643		
FAULT FLAG (nFLT)						
PGOOD Delay	t_{PGOODF}	Falling edge, internal FET turn off to nFLT↓		875		μs
	t_{PGOODR}	Rising edge, internal FET turn on to nFLT↑		1500		

NOTE:

1. Guaranteed by design, not tested in production.

PARAMETER MEASUREMENT INFORMATION

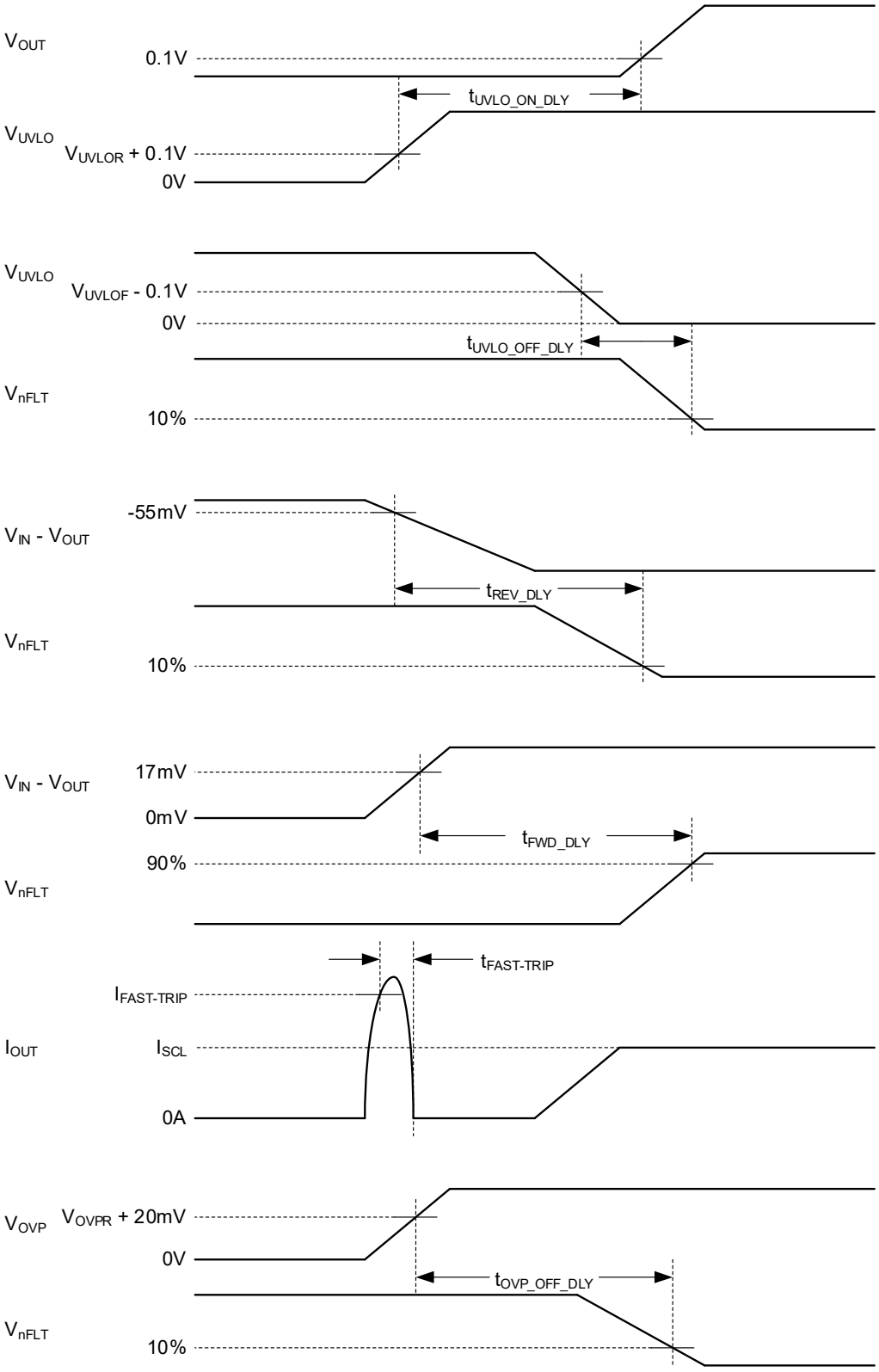


Figure 2. Timing Waveforms

FUNCTIONAL BLOCK DIAGRAM

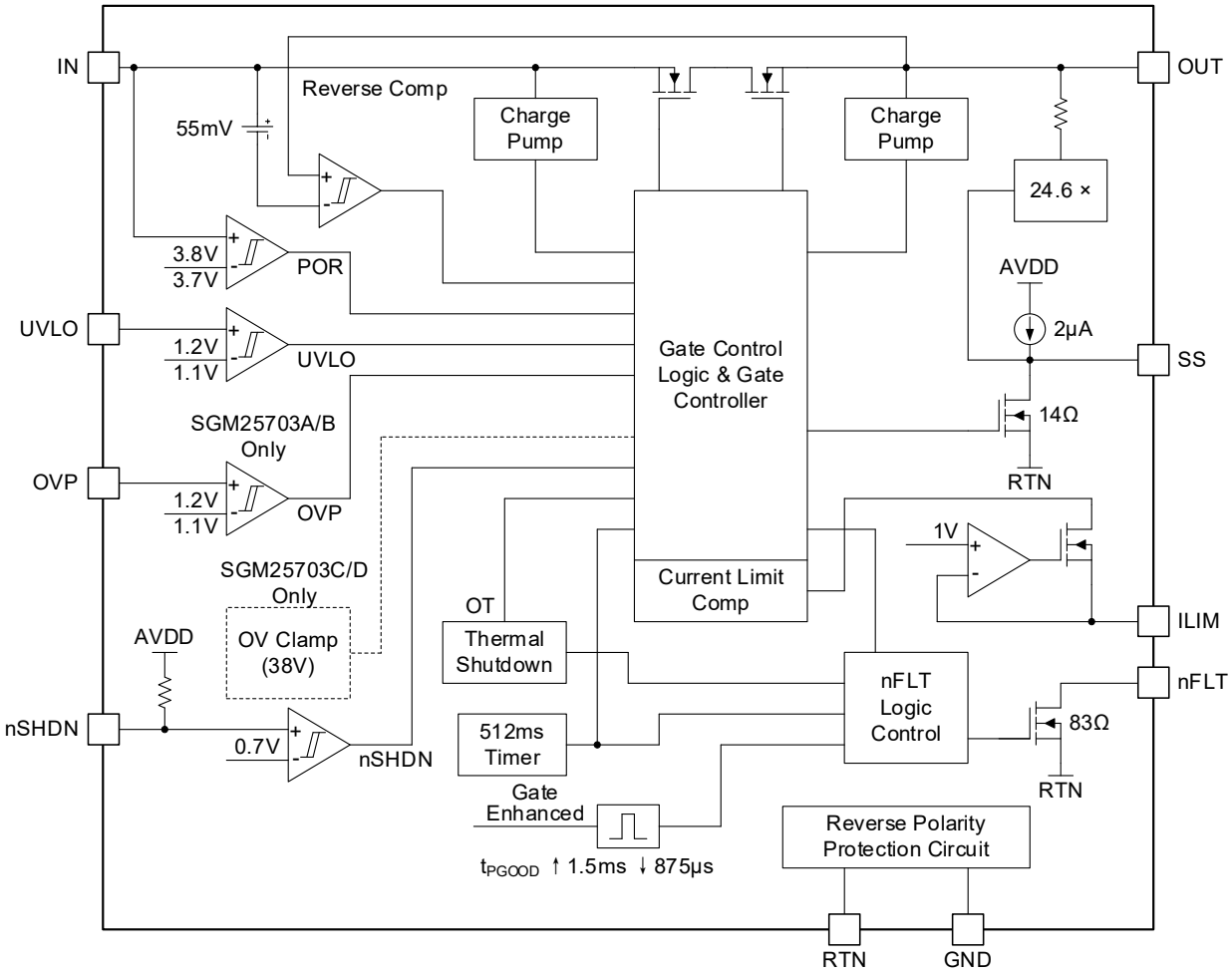
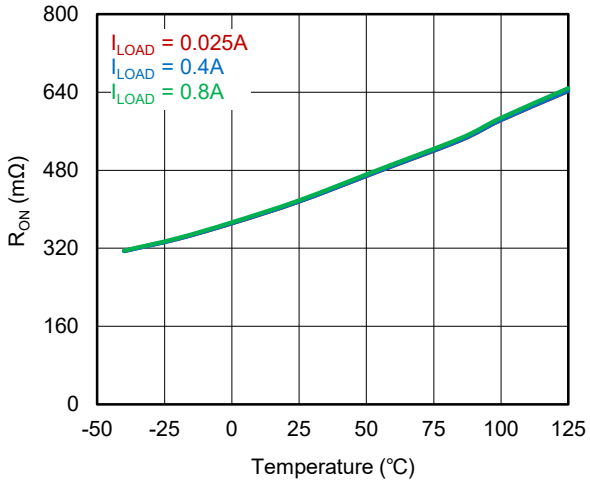


Figure 3. Block Diagram

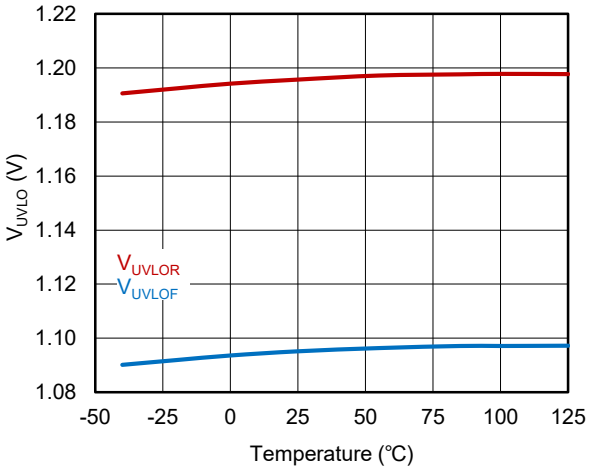
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = -40℃ to +125℃, unless otherwise noted.

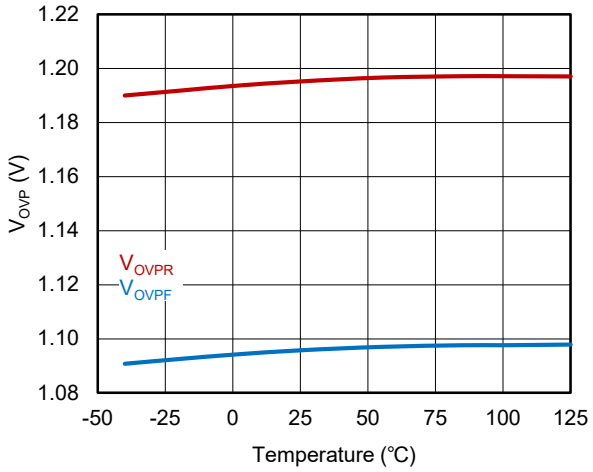
R_{ON} vs. Temperature (Across Load Current)



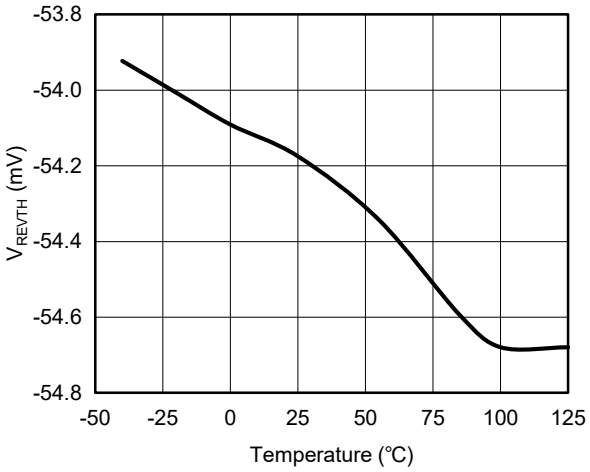
V_{UVLO} vs. Temperature



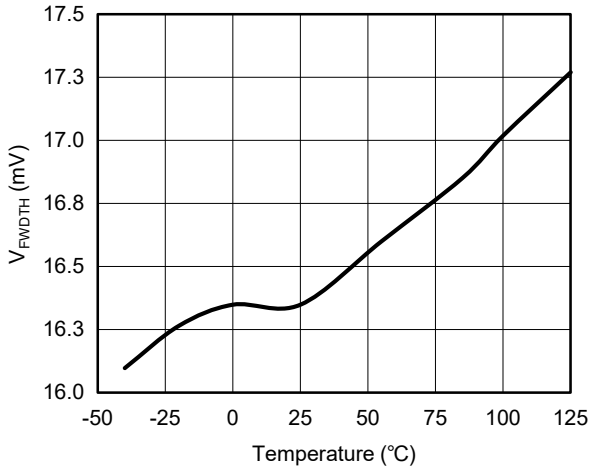
V_{OVP} vs. Temperature



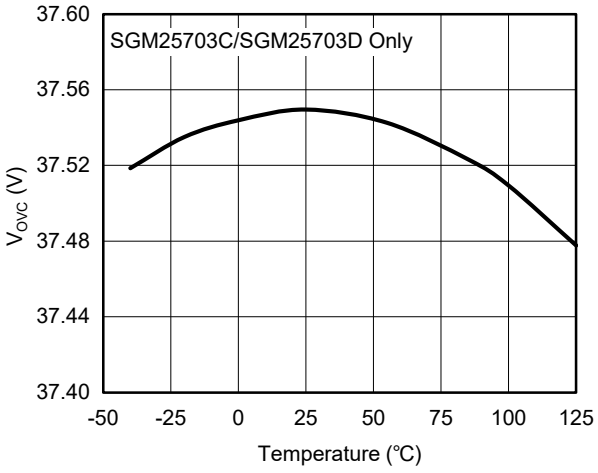
V_{REVTH} vs. Temperature



V_{FWDTH} vs. Temperature



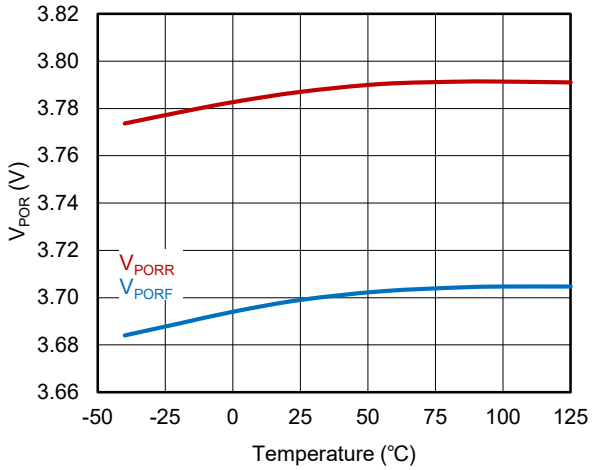
V_{OVC} vs. Temperature



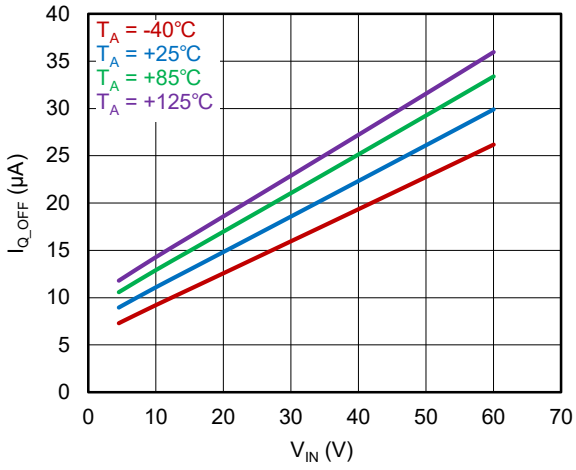
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

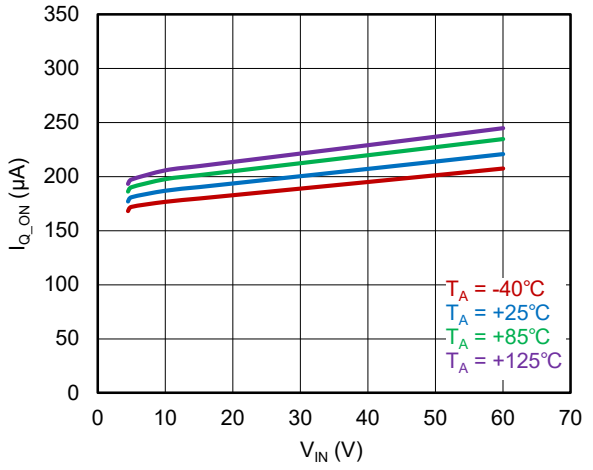
V_{POR} vs. Temperature



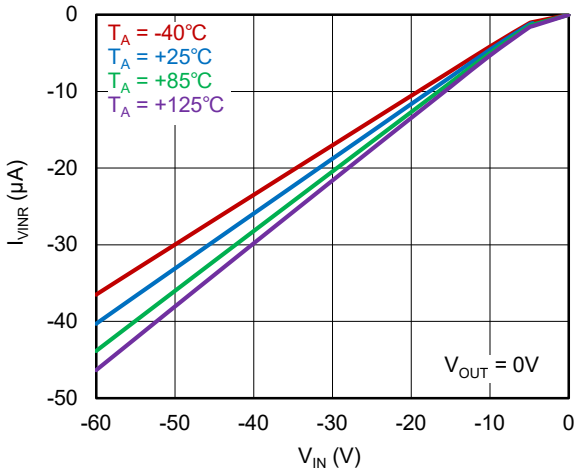
I_{Q_OFF} vs. V_{IN} (Shutdown)



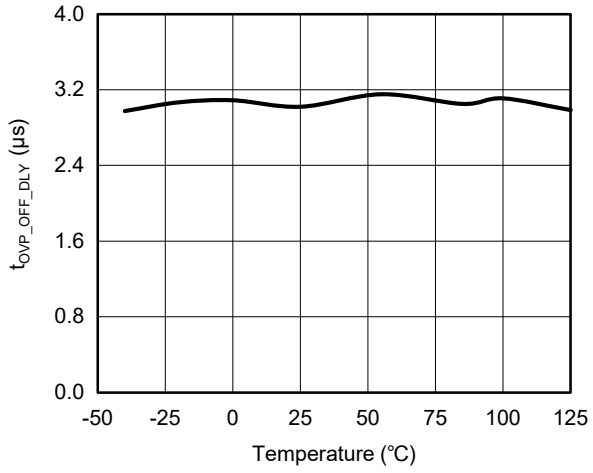
I_{Q_ON} vs. V_{IN} (Normal Operation)



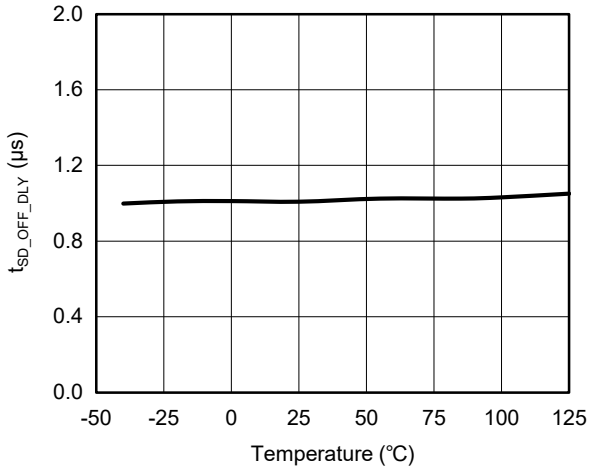
I_{VINR} vs. V_{IN} (Reverse Voltage)



$t_{OVP\_OFF\_DLY}$ vs. Temperature



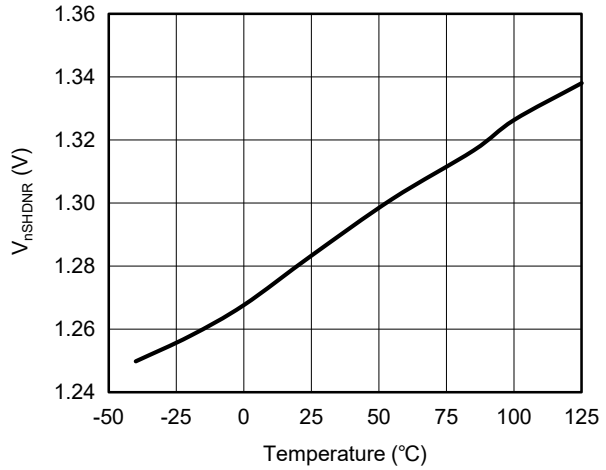
$t_{SD\_OFF\_DLY}$ vs. Temperature



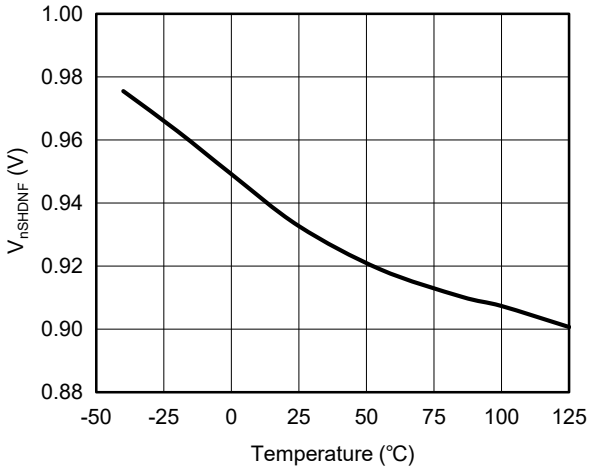
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

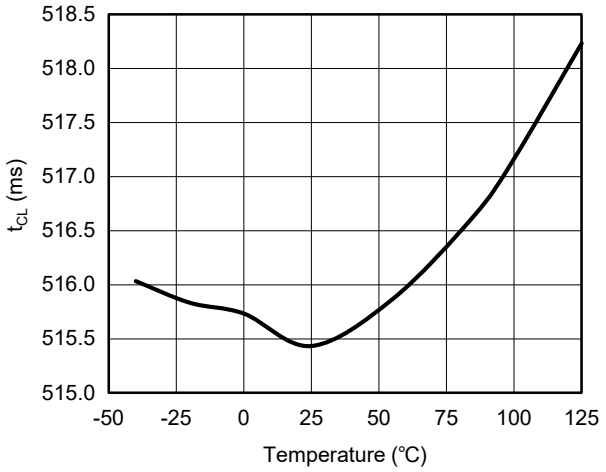
V_{nSHDNR} vs. Temperature



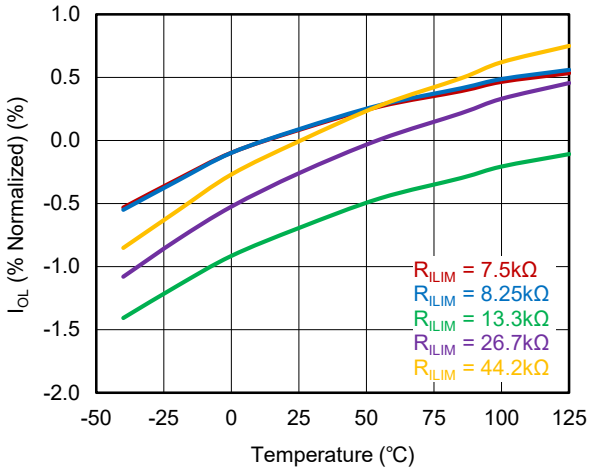
V_{nSHDNF} vs. Temperature



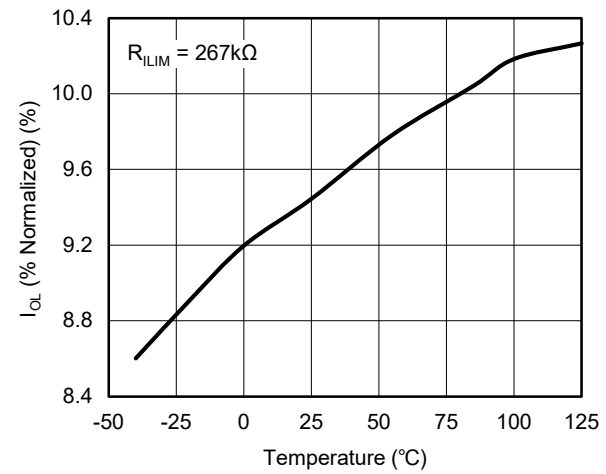
t_{CL} vs. Temperature



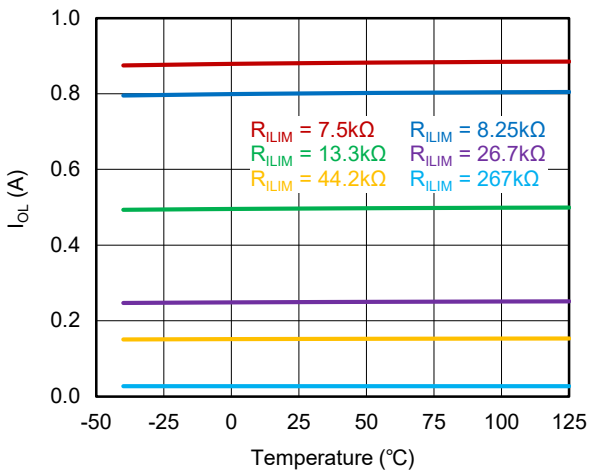
I_{OL} (% Normalized) vs. Temperature



I_{OL} (% Normalized) vs. Temperature



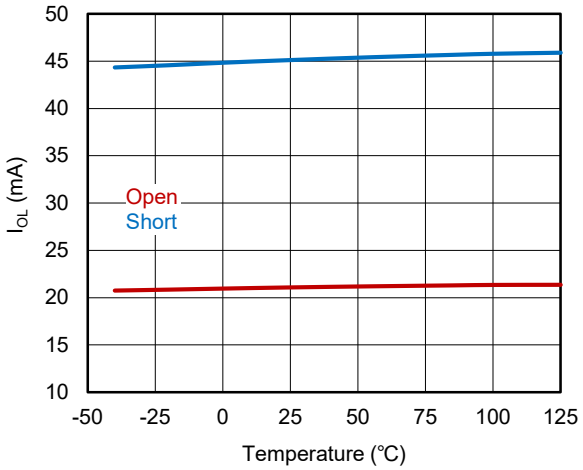
I_{OL} vs. Temperature



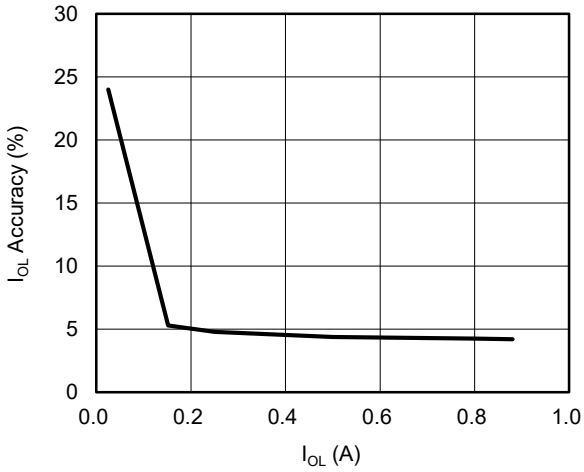
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

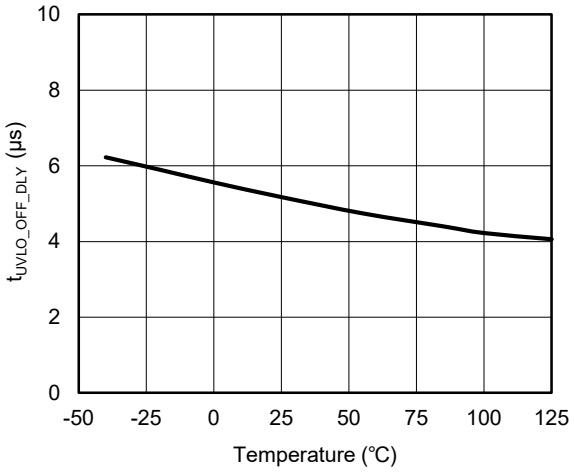
I_{OL} vs. Temperature (R_{ILIM} = Open and Short)



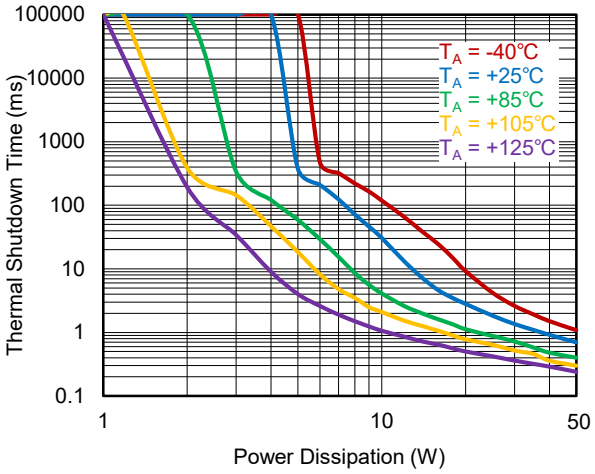
I_{OL} Accuracy vs. I_{OL}



$t_{UVLO\_OFF\_DLY}$ vs. Temperature



Thermal Shutdown Time vs. Power Dissipation (1)



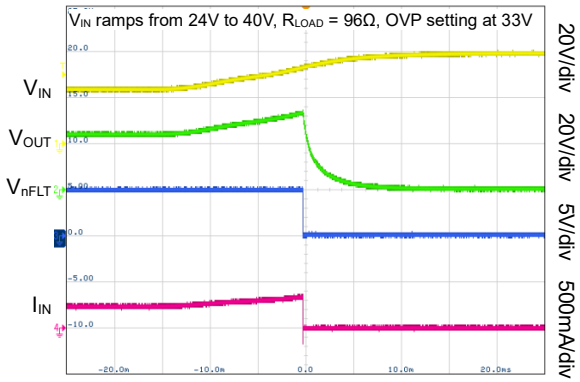
NOTE:

1. Taken on 2-layer board, 2 oz. (0.08mm thick) with RTN plane area: 1cm^2 (Top) and 4.6cm^2 (Bottom).

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

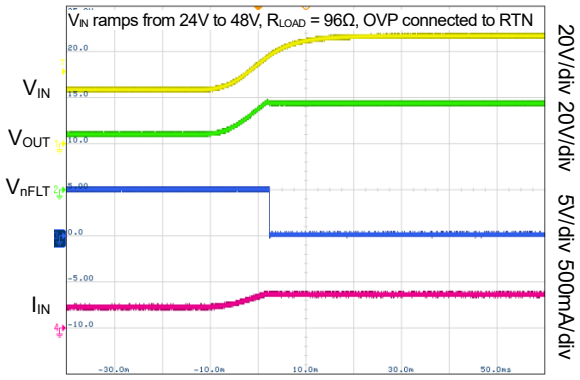
T_A = +25℃, V_{IN} = 24V, R_{ILIM} = 7.5kΩ, C_{IN} = C_{OUT} = 1.1μF, C_{SS} = open, and nFLT is pulled up to 5V external source (V_{CC}) separately, unless otherwise noted.

Over-Voltage Lockout



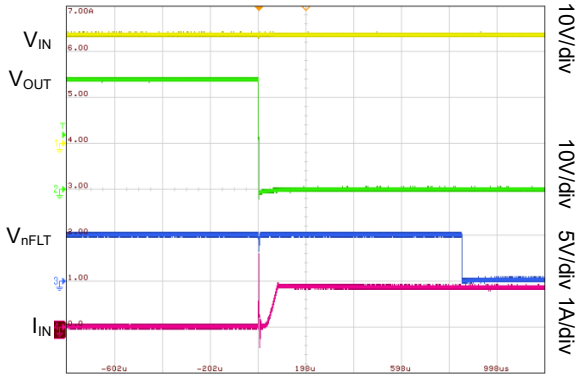
Time (5ms/div)

Over-Voltage Clamp (SGM25703C, SGM25703D)



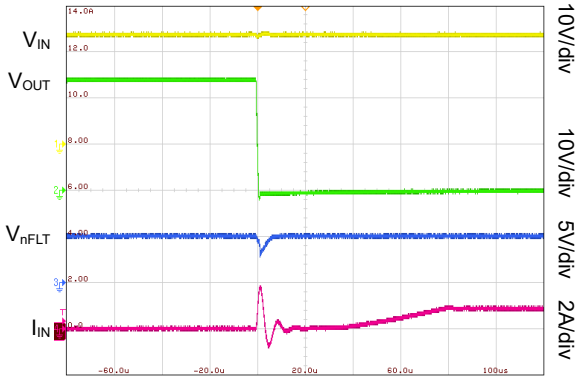
Time (10ms/div)

Output Hot-Short Functionality at 24V Input



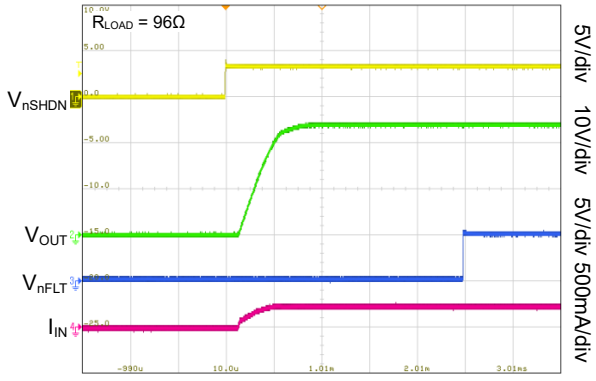
Time (200μs/div)

Hot-Short Fast-Trip Response (Zoomed)



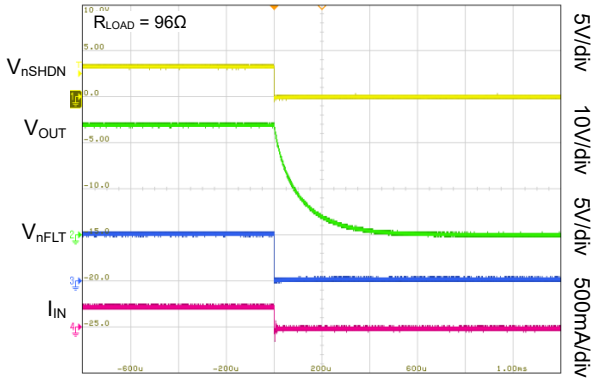
Time (20μs/div)

Turn-On by nSHDN



Time (500μs/div)

Turn-Off by nSHDN

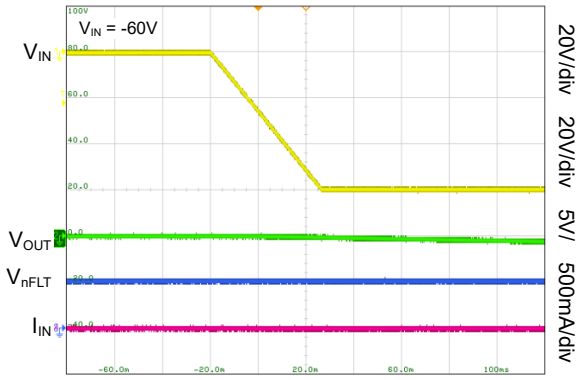


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

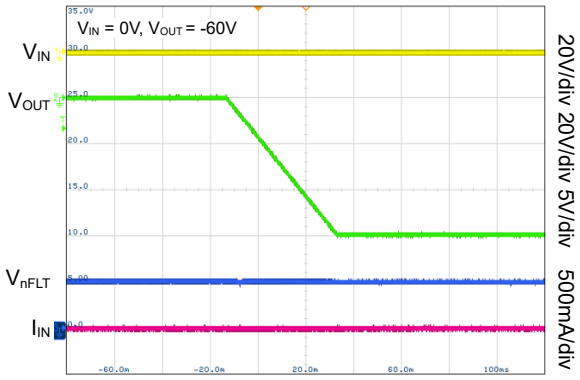
T_A = +25℃, V_{IN} = 24V, R_{ILIM} = 7.5kΩ, C_{IN} = C_{OUT} = 1.1μF, C_{SS} = open, and nFLT is pulled up to 5V external source (V_{CC}) separately, unless otherwise noted.

Input Polarity Reverse Protection



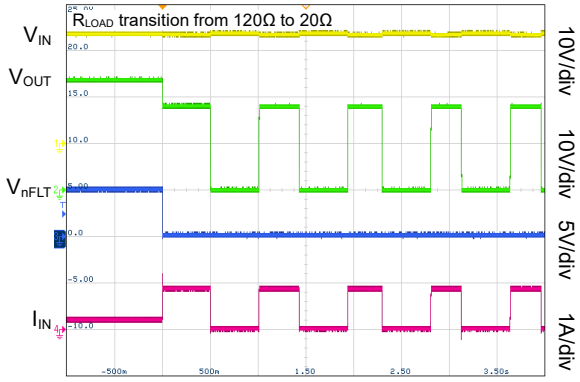
Time (20ms/div)

Output Polarity Reverse Protection



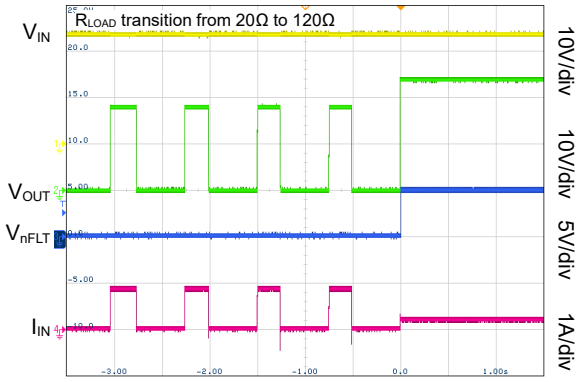
Time (20ms/div)

Auto-Retry Fault Behavior



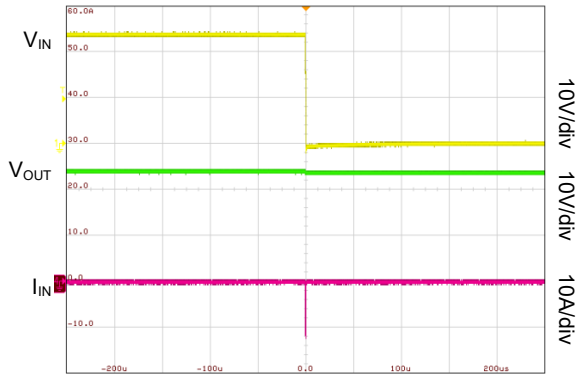
Time (500ms/div)

Response during Coming out of Overload Fault



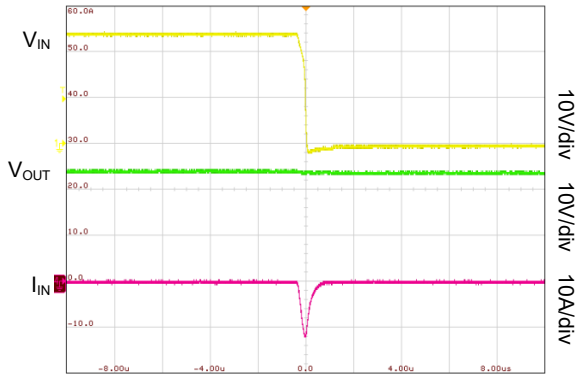
Time (500ms/div)

Input Hot-Short Functionality at 24V Supply



Time (50μs/div)

Hot-Short Response (Zoomed)

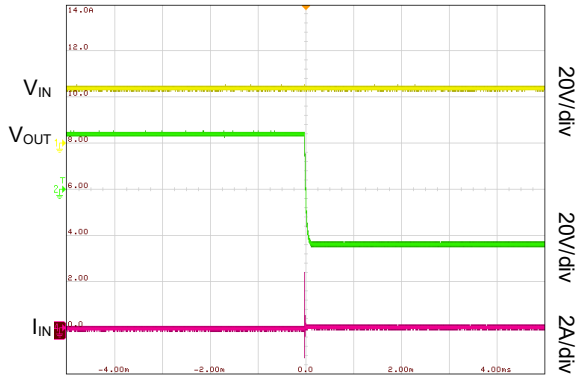


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

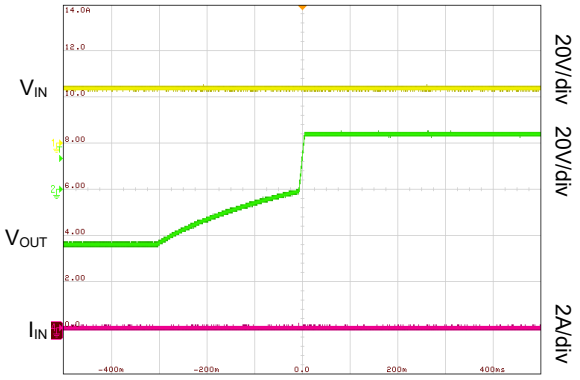
T_A = +25℃, V_{IN} = 24V, R_{ILIM} = 7.5kΩ, C_{IN} = C_{OUT} = 1.1μF, C_{SS} = open, and nFLT is pulled up to 5V external source (V_{CC}) separately, unless otherwise noted.

Reverse Output Polarity Protection with -24V at OUT and 24V at IN



Time (1ms/div)

Response during Coming out of Output Reverse Polarity Fault Condition



Time (100ms/div)

DETAILED DESCRIPTION

The SGM25703 is a high-voltage industrial efuse featuring integrated back-to-back FETs design and comprehensive protection functions. This device features a broad supply input range of 4.5V to 60V. This device supports inrush current control and programmable output voltage slew rate control. With an ability to withstand up to ±60V at the input without damage, it is well-suited for hot-swap power applications. Additionally, it integrates multiple protection features such as under-voltage, over-voltage, and over-current protection to ensure robust safeguarding of peripheral equipment. The accurate over-current limit threshold (±4.2% at 880mA) reduces the system over-design. Under output short-circuit conditions, the fast-trip short-circuit protection responds within 200ns (TYP) to shut down the device and disconnect the fault current.

Under-Voltage Lockout (UVLO)

The SGM25703 provides programmable under-voltage lockout (UVLO) protection. When the voltage of UVLO drops below the falling threshold V_{UVLOF}, the internal MOSFET is turned off and nFLT pin is asserted. The UVLO hysteresis is 101mV (TYP). The UVLO threshold can be set through connecting a resistor network from IN to UVLO pin and to RTN.

Over-Voltage Protection (OVP)

The SGM25703 series of device provides robust input over-voltage protection. The SGM25703A and SGM25703B offer programmable over-voltage cut-off protection. When the voltage on OVP pin exceeds the rising threshold V_{OVPR}, the internal MOSFET is turned off. The OVP threshold can be set by connecting a resistor network from IN to OVP pin and to RTN. If the over-voltage feature is not used, connect the OVP pin directly to RTN.

The SGM25703C and SGM25703D provide 38V over-voltage clamp protection. When the input voltage exceeds 38V, the device clamps the output to the V_{OVC} threshold. Under this condition, the power dissipation of the chip is $P_D = (V_{IN} - V_{OVC}) \times I_{OUT}$. If the device continues to operate in the over-voltage clamp state, it may trigger thermal protection due to excessive heat. If the device temperature is below T_{SD}, the device shuts off the internal FET following the t_{CL_DLY} delay. Following this shutdown, the SGM25703C latches off, while the SGM25703D auto-retries.

Hot Plug-In and Inrush Current Control

The SGM25703 is designed to provide hot plug-in power management by controlling the inrush current as well as the output slew rate. This design helps eliminate the voltage drop and avoid undesired power reset. The output ramp rate at power-on is set by the capacitor from the SS pin to RTN.

If SS pin is left open, the device will start up with the fastest output slew rate (t_{SS}) of 24V/643μs. The inrush current can be calculated using Equation 1.

$$I_{SS} = \frac{C_{SS}}{GAIN_{SS}} \times \frac{dV_{OUT}}{dt} \quad (1)$$

where:

I_{SS} = 1.96μA (TYP).

$\frac{dV_{OUT}}{dt}$ = Desired output slew rate.

$GAIN_{SS}$ = SS to V_{OUT} gain = 24.6.

Equation 2 can be used to calculate the total rise time t_{SS} of V_{OUT} from 0 to V_{IN}.

$$t_{SS} = 20.7 \times 10^3 \times V_{IN} \times C_{SS} \quad (2)$$

Reverse Polarity Protection

Input-Side Reverse Polarity Protection

The SGM25703 series features input-side reverse polarity protection, allowing the input to withstand reverse voltages of up to -60V without damage. The internal FETs are turned off during an input reverse-polarity event to prevent damage to downstream loads caused by reverse input voltage due to incorrect wiring.

Output-Side Reverse Polarity Protection

The SGM25703 series is equipped with output-side reverse polarity protection. To safeguard upstream circuits against negative voltage, the internal FETs turn off during an output reverse-polarity event. This voltage could appear at the output due to miswiring on the output-side with external isolated power supplies.

DETAILED DESCRIPTION (continued)

Overload and Short-Circuit Protection

Load current is monitored via the internal sense resistor, and FET current is monitored during start-up and normal operation.

Overload Protection

When the active current limit mode is selected, the device will regulate the output current to the user-programmed current limit I_{OL} during an overload event. Use Equation 3 to set the over-current limit threshold with an external resistor R_{ILIM}.

$$I_{OL} = \frac{6.636}{R_{ILIM}} \quad (3)$$

where:

I_{OL} is the overload current limit in A.

R_{ILIM} is the current limit resistor in kΩ.

After the T_{SD} threshold is reached or the t_{CL_DLY} timer expires, the internal FETs within the eFuse switch off. For the SGM25703A and SGM25703C, the internal FETs are latched off. To reset the latch, cycle either the nSHDN or UVLO pin, or power-cycle the VIN supply. The SGM25703B and SGM25703D initiate an auto-retry cycle after a 512ms retry delay. Following this delay, the internal FETs turn on again with SS slew-rate control. If the overload condition persists, the output current is regulated to the programmed limit I_{OL}. The maximum current-limiting time t_{CL_DLY} is 512ms.

Short-Circuit Protection

When the output short-circuit occurs, the current from IN to OUT rises very rapidly. Due to limited bandwidth, the current-limit amplifier is unable to respond quickly to this fault. To solve this, the SGM25703 integrates with a fast-trip comparator which can shut down the internal MOSFETs within 200ns (TYP). The fast-trip comparator works and cuts off the short-circuit current when the device current I_{OUT} exceeds the fast-trip threshold $I_{FAST-TRIP}$. The internal MOSFETs would remain OFF state for only a few ms, following by soft-restart in a current-limit manner where current through the device is regulated to I_{OL} under the regulation of current-limit amplifier. Then, the device behaves the same as the overload condition. The fast-trip comparator turn-off time for the internal FET is dynamically adjusted according to V_{IN} - V_{OUT} after the current surpasses $I_{FAST-TRIP}$: the greater the voltage differential, the shorter the delay $t_{FAST-TRIP\_DLY}$.

Start-Up with Short-Circuit on Output

For power-up with output short-circuit to GND, the current through the device is limited to I_{OL}. This feature facilitates rapid fault isolation and thereby maintains DC bus stability. Under any overload or short-circuit condition, enhanced thermal dissipation is recommended.

Reverse Current Protection

To provide true reverse current blocking, the device senses V_{IN} and V_{OUT} and reacts to reverse or input-power-fail events. The reverse comparator responds by turning off the internal FET quickly when V_{IN} is shorted to GND. The internal FET is turned on again within 63μs (TYP) once the forward differential voltage V_{IN} - V_{OUT} rises above 117mV.

FAULT Response

The SGM25703 features an open-drain fault indicator (nFLT) pin. This pin is pulled low to signal a fault condition when any of the following events occur: input under-voltage, over-voltage, overload, reverse current, and thermal shutdown. The nSHDN pin is pulled low or during the start-up sequence before the MOSFET is fully turned on. To avoid false reporting, this pin is designed with an internal de-glitch without additional external circuits.

The nFLT signal, besides providing fault indication, can also be used as a power-good indicator for downstream loads such as DC/DC converters. The internal PGOOD signal is ORd with the fault logic to generate the nFLT output. During start-up, both PGOOD and nFLT remain low while the device is in SS mode, and are de-asserted only after SS mode finishes and the internal FET is fully enhanced. The PGOOD signal features a rising-edge deglitch delay, which ensures that the internal FET is fully turned on before the downstream converters apply heavy loads. The delay t_{PGOODR} is 1500μs; the nFLT pin, if unused, this pin can be left open or connected to RTN; and the nFLT signal resets when V_{IN} falls below 3.4V.

DETAILED DESCRIPTION (continued)

IN, OUT, RTN, and GND Pins

The SGM25703 features two pins each for IN and OUT. The two input pins must be connected together to the input power supply, with ceramic capacitors placed near the device to suppress transient interference. Similarly, the output pins must be connected together to the load. The output voltage is calculated as shown in Equation 4.

$$V_{OUT} = V_{IN} - (R_{ON} \times I_{OUT}) \quad (4)$$

where:

R_{ON} is the total on-resistance of the internal FETs.

The GND pin must be tied to the system ground. The RTN pin serves as the reference point for all internal control circuits. When configuring the external circuitry of the SGM25703, note that components including R_{ILIM}, C_{SS}, and the resistors connected to UVLO and OVP must be referenced to RTN. To handle input reverse polarity faults, the device incorporates an internal protection circuit between RTN and GND. The input reverse polarity protection is disabled when RTN is tied directly to GND.

Thermal Shutdown

The device features over-temperature protection. When the junction temperature exceeds the thermal shutdown threshold T_{SD}, the internal FETs are turned off immediately. Once thermal shutdown is triggered, the device will time 512ms after the junction temperature cools to T_{SD} - 10℃, and then either latch off or attempt an auto-retry based on the configured fault response mode. During the thermal shutdown process, the nFLT pin is pulled low to signal the fault condition.

Device Functional Modes

Low Current Shutdown Control (nSHDN)

The device can be shut down through pulling the nSHDN pin below the 0.7V threshold with a micro-controller. In shutdown mode, the quiescent current of the device is reduced to 16.5μA (TYP). The controller or any other device should have at least 10μA sinking current capability to pull down the nSHDN pin. To enable the device, pulling nSHDN up to at least 1.5V where the device starts up with soft-start mode.

APPLICATION INFORMATION

Typical Application

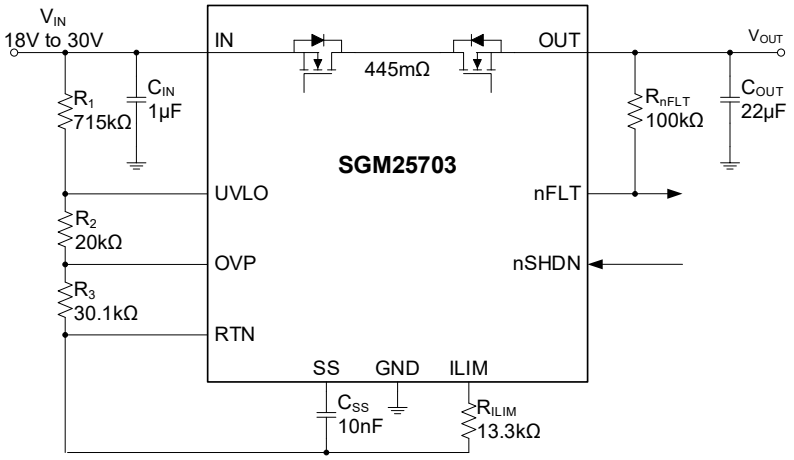


Figure 4. SGM25703 Typical Application

Design Requirements

Table 1 lists the design requirements for SGM25703.

Table 1. Design Requirements

EXAMPLE VALUE		DESIGN PARAMETER
Typical Input Voltage	V_{IN}	24V
Under-Voltage Lockout Set Point	V_{UV}	18V
Over-Voltage Cut-Off Set Point	V_{OV}	30V
Load during Start-Up	R_{L_SU}	96Ω
Overload Current-Limit	I_{OL}	500mA
Load Capacitance	C_{OUT}	22µF
Maximum Ambient Temperature	T_A	125℃

Detailed Design Procedure

Programming the Current Limit Threshold - R_{ILIM} Selection

The current limit level is set by the ILIM pin resistor R_{ILIM}, which can be determined using Equation 5.

$$R_{ILIM} = \frac{6.636}{I_{ILIM}} = 13.27k\Omega \quad (5)$$

where:

I_{LIM} = 500mA.

Choose the closest value from the standard 1% resistor series: R_{ILIM} = 13.3kΩ.

Under-Voltage Lockout and Over-Voltage Set Point

Resistors R_1, R_2, and R_3 form a network from IN to RTN, with the UVLO and OVP pins tapping into the divider, thereby setting the UVLO and OVLO threshold voltages. These resistors are selected based on Equation 6 and Equation 7.

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \quad (6)$$

$$V_{UVLOR} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \quad (7)$$

To reduce the current drawn from the power supply, resistors with higher values for R_1, R_2 and R_3 are recommended.

Form the electrical specifications, V_{OVPR} = 1.19V and V_{UVLOR} = 1.19V. For this design, V_{OV} is 30V and V_{UV} is 18V. First, choose R_3 = 30.1kΩ, and use Equation 6 to solve (R_1 + R_2) = 728.7kΩ. Combine this with Equation 7 to solve R_2 = 20.05kΩ and R_1 = 708.6kΩ.

Select the closest standard 1% resistor values: R_1 = 715kΩ, R_2 = 20kΩ, and R_3 = 30.1kΩ.

Setting Output Voltage Ramp Time - t_{SS}

The chip junction temperature must be maintained below the thermal shutdown threshold (T_{SD}) to ensure proper operation during both start-up and steady state. Since dynamic power consumption can be an order of magnitude higher than steady-state levels, the output start-up time and inrush current limiting must be considered in the design to prevent thermal shutdown events.

The soft-start capacitor (C_{SS}) can be calculated based on the following two scenarios:

APPLICATION INFORMATION (continued)

Case 1: Start-Up without Load - Only Output Capacitance C_{OUT} Draws Current during Start-Up

During a capacitive load start-up, the output voltage increases with a constant slope. As the voltage differential across the internal FET drops, its power dissipation is reduced accordingly. Figure 5 illustrates the output voltage, inrush current, and device power dissipation curves during start-up with an output capacitor. The average chip power dissipation during the start-up process equals the time-averaged value of the instantaneous power.

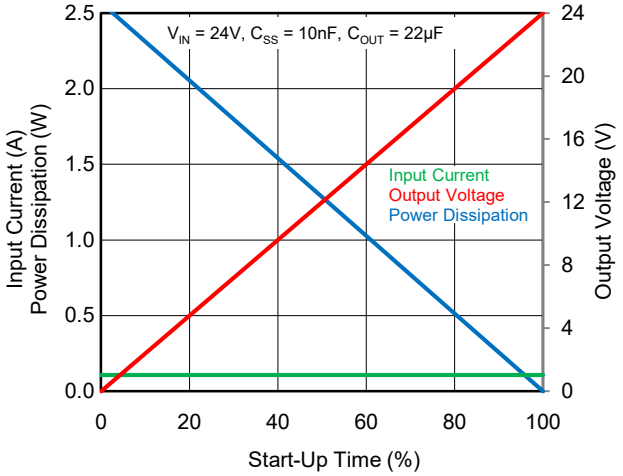


Figure 5. P_{D_INRUSH} due to Inrush Current

The inrush current is determined as shown in Equation 8.

$$I = C \times \frac{dV}{dt} \geq I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{t_{SS}} \quad (8)$$

Use Equation 9 to calculate the average power dissipated during start-up.

$$P_{D\_INRUSH} = 0.5 \times V_{IN} \times I_{INRUSH} \quad (9)$$

Equation 9 assumes the load draws no current until V_{OUT} reaches its final value.

Case 2: Start-Up with Load - Output Capacitance C_{OUT} and Load Draws Current during Start-Up

During start-up, the presence of additional loads will introduce extra power loss. Taking a resistive load R_{L_SU} as an example, *Start-Up with Load* shows its output voltage, inrush current, and the chip's instantaneous power dissipation. The Figure 6 illustrates the relationship between the power loss of the internal FET and the start-up time. During start-up, the additional power loss is obtained via Equation 10.

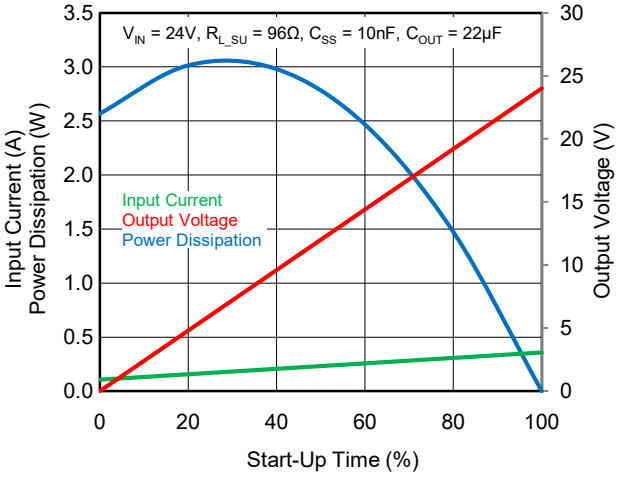


Figure 6. P_{D_INRUSH} due to Inrush and Load Current

During start-up, the additional power loss is obtained via Equation 10.

$$P_{D\_LOAD} = \frac{1}{6} \times \frac{V_{IN}^2}{R_{L\_SU}} \quad (10)$$

The total power dissipation during start-up is given by Equation 11.

$$P_{D\_START-UP} = P_{D\_INRUSH} + P_{D\_LOAD} \quad (11)$$

The total current during the start-up phase is given by Equation 12.

$$I_{START-UP} = I_{INRUSH} + I_{L\_t} \quad (12)$$

For this design example,

with the inrush current set to I_{INRUSH} = 0.1A for this case, t_{SS} = 5.28ms, calculated using Equation 8.

Based on t_{SS} = 5.28ms and V_{IN} = 24V, the C_{SS} capacitor value can be determined using Equation 2.

Select the closest standard value: 10.0nF/16V capacitor.

The inrush power dissipation is 1.2W, calculated using Equation 9.

The additional power dissipation during start-up with a 96Ω load is 1W, calculated using Equation 10. The total device power dissipation during start-up is 2.2W.

APPLICATION INFORMATION (continued)

To ensure proper chip start-up, the power dissipation during start-up must not exceed the thermal shutdown limit specified in *Thermal Shutdown Time vs. Power Dissipation.*

Based on the thermal shutdown limit graph, the thermal shutdown time for a 2.2W dissipation is approximately 190ms at T_A = +125℃. A minimum 30% margin is recommended to account for system parameter variations (load, tolerances, input voltage, and layout). With the selected 10nF C_{SS} capacitor, the start-up time (t_{SS}) is 5.28ms, which is well within the limit. This ensures successful start-up under a 96Ω load.

In the above case, a 10nF soft-start capacitor sets the start-up time to approximately 5.28ms, which meets the start-up requirement for a 96Ω load. To further reduce power dissipation, a larger soft-start capacitor (C_{SS}) value can be selected.

Support Component Selections – R_{nFLT} and C_{IN}

The nFLT pin is an open-drain output and requires an external pull-up resistor, R_{nFLT}. The maximum sink current for this pin must not exceed 10mA. It is recommended to use a resistor value between 10kΩ and 100kΩ for R_{nFLT}. C_{IN} is the input bypass capacitor, which serves to suppress noise from the power supply. A capacitor value between 0.1μF and 1μF is recommended for C_{IN}.

Application Curves

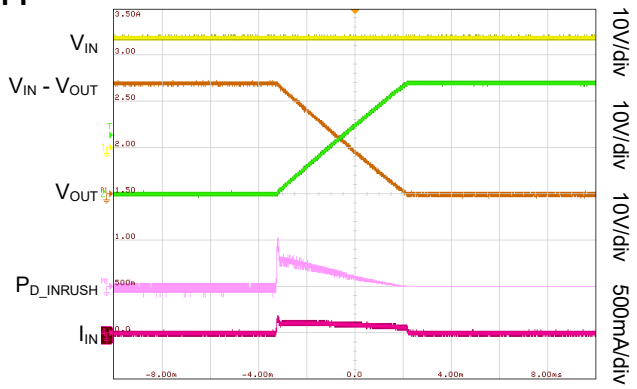


Figure 7. Start-Up without Load

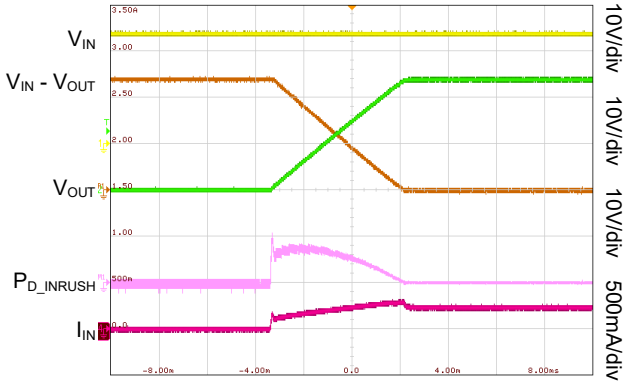


Figure 8. Start-Up with Load

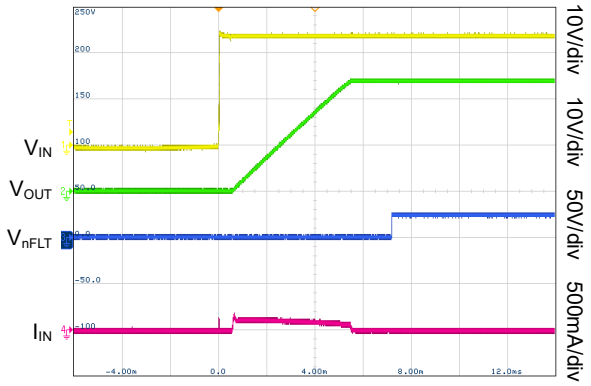


Figure 9. Start-Up with V_{IN} - No Load

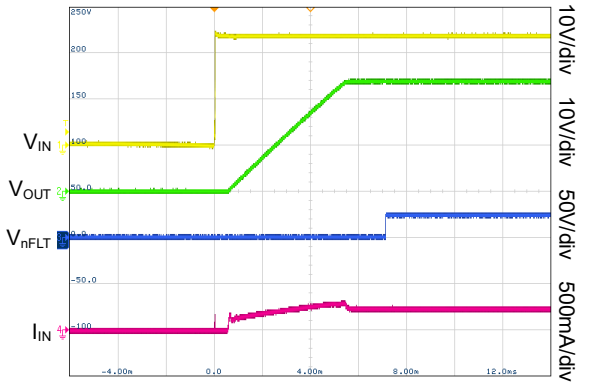


Figure 10. Start-Up with V_{IN} – 96Ω Load

APPLICATION INFORMATION (continued)

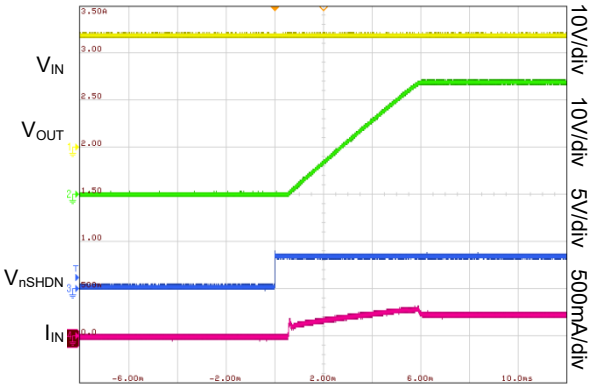


Figure 11. Start-Up with Shutdown Pin - 96Ω Load

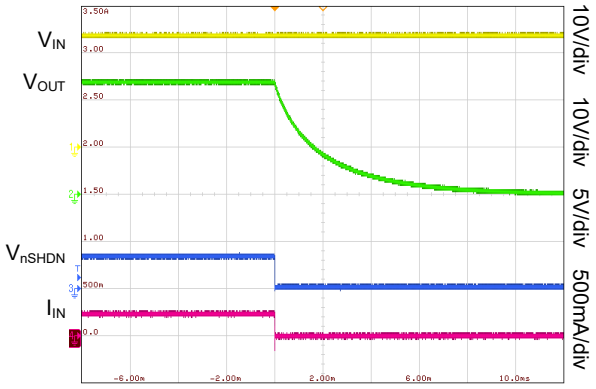


Figure 12. Power Down with Shutdown Pin - 96Ω Load

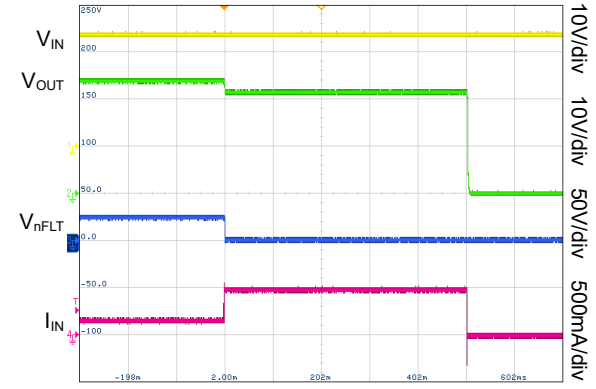


Figure 13. Overload Response - Load Stepped from 136Ω to 36Ω Load

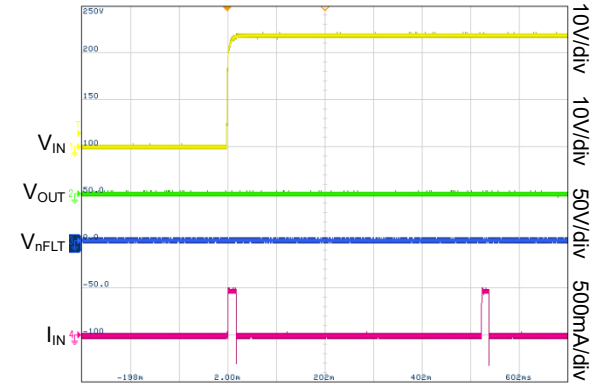


Figure 14. Turn-On with Short-Circuit on Output

APPLICATION INFORMATION (continued)

System Examples

Field Supply Protection in PLC, DCS I/O Modules

PLC and Distributed Control System (DCS) I/O modules are often powered by an external field supply to meet the higher power demands of connected sensors, actuators, and other field loads. However, power-supply faults or wiring errors can lead to improper operation or even permanent damage to these loads. The use of a front-end protection device is therefore recommended to ensure a robust and stable power feed. Such devices are equipped with under-voltage, over-voltage, and bi-directional reverse-polarity protection, which collectively prevent the loads from being exposed to voltages beyond their rated operating range, thereby averting potential permanent failure.

A single field power supply is often shared among multiple I/O modules, delivering a current exceeding the safe rating of any one module. The SGM25703 incorporates an over-current protection mechanism that actively limits the current drawn from the supply to the module, thus preventing the board from being subjected to currents above its design threshold. Its fast short-circuit protection quickly isolates faulty loads, preventing the supply voltage from dropping and disrupting other modules on the same bus. With a highly accurate current limit, the device allows more modules to be tied to the field supply. The integrated fault indicator (nFLT) enables continuous load monitoring for enhanced system reliability.

The device also functions as a smart diode, providing reverse current protection in the event of output-side miswiring. Such reverse current poses a risk of damaging the field supply, inducing excessive heating in I/O modules, and potentially resulting in irreversible hardware damage.

Field power supplies are often connected via screw terminals, making input-side reverse-polarity wiring a realistic possibility. Such a fault can apply reverse voltage to the field loads, causing permanent damage. Furthermore, during installation, the power supply may be miswired to the output terminals instead of the input. This can result in damage to the upstream power supply and its related components. The device incorporates both input-side and output-side reverse-polarity protections, effectively blocking reverse voltage from reaching either the load or the supply. This dual-side safeguarding offers comprehensive system protection against miswiring incidents in the field.

Power Stealing in Smart Thermostat

The SGM25703 eFuse offers adjustable protection features, including inrush current limiting, over-voltage, and over-current protection, which simplify power management design for smart thermostats.

Do's and Don'ts

RTN must not be tied to GND, otherwise the input reverse polarity protection will be disabled.

All external components for the SGM25703 - including R_{ILIM}, C_{SS}, and the UVLO and OVP resistor dividers - must be connected to the RTN pin.

To optimize thermal performance, the exposed pad must be tied to the RTN plane.

Power Supply Recommendations

The SGM25703 electronic fuse is recommended for a working power supply voltage range of 4.5V to 60V, with the V_{IN} (input voltage) supported up to 60V. For power supplies a few inches away, a 0.1μF or larger bypass ceramic capacitor should be placed at the input end.

APPLICATION INFORMATION (continued)

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input with a negative voltage spike occurring at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- A ceramic capacitor lower than 0.1μF is connected near the input pin to absorb the energy and suppress the transients.

The input capacitance is determined from Equation 13:

$$V_{SPIKE\_ABSOLUTE} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (13)$$

where:

V_{IN} is the rating of the input voltage.

I_{LOAD} is the load current.

L_{IN} is the effective inductance seen at the source.

C_{IN} is the input capacitance.

Certain applications may necessitate additional transient voltage suppressors (TVS) to safeguard the device from transients that might exceed its absolute maximum ratings. These transients may occur during positive-polarity and negative-polarity surge testing on the power supply lines. In such applications, add a minimum 1μF input capacitor to ensure the input voltage falling slew rate does not exceed 20V/μs.

Figure 15 illustrates the circuit implementation, including optional protection components such as a ceramic capacitor, TVS, and Schottky diode.

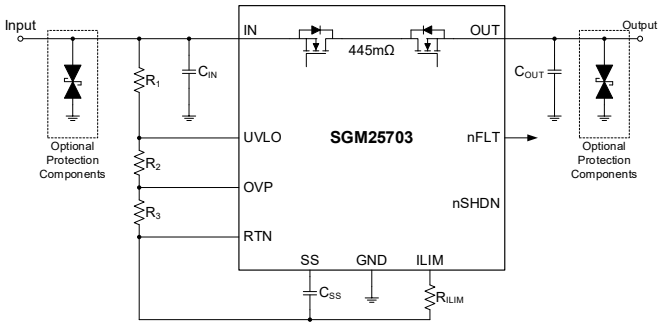


Figure 15. Circuit Implementation with Optional Protection Components

Layout

- In any application, it is recommended to connect a decoupling capacitor of 0.1μF or greater between IN and GND. This decoupling capacitor should be as close as possible to IN and GND pins.
- The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.
- RTN serves as the chip's reference ground and must be implemented as a copper plane or a dedicated copper island.
- All external components - including R_{ILIM}, C_{SS}, and the OVP and UVLO resistors - must be placed close to their respective chip pins and connected to the RTN plane. All associated traces must be made as short as possible.
- The traces for the R_{ILIM} components must be made as short as practical to minimize parasitic effects that could degrade accuracy. Furthermore, these critical traces must be routed away from any switching signals to prevent noise coupling.
- Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the circuit loop formed by the protection components should be as small as possible.
- Thermal Design Requirement: To ensure reliable operation at rated power, the exposed pad must be directly soldered to the RTN copper plane. For high-current applications, the PCB bottom layer or other internal planes should be utilized to enhance thermal dissipation.

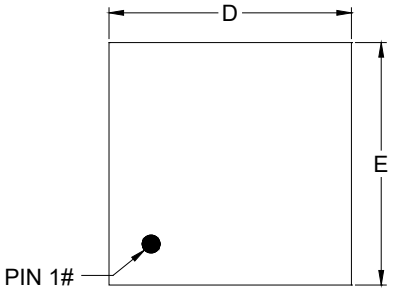
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

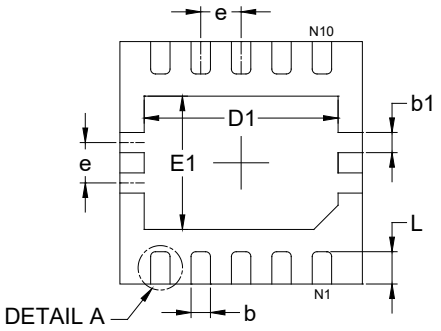
Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

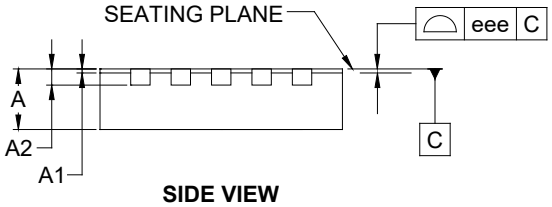
TDFN-3×3-10AL



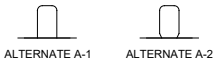
TOP VIEW



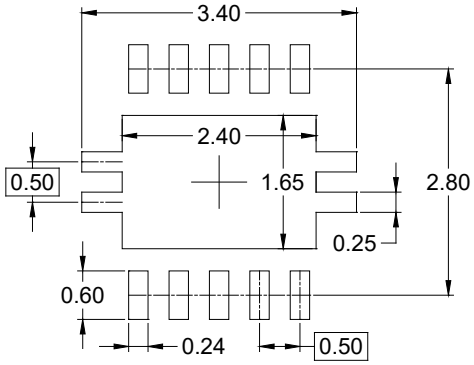
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



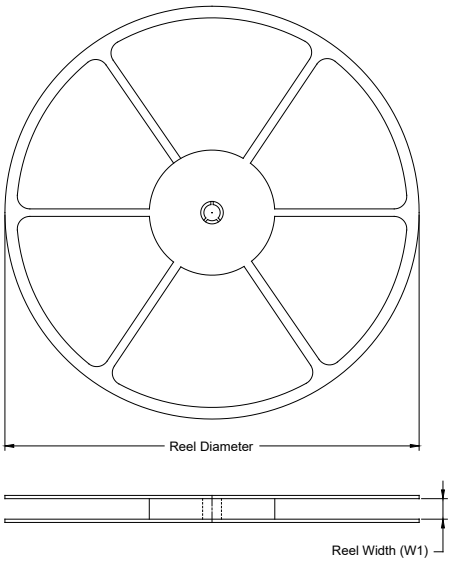
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
b1		0.250 REF	
D	2.900	-	3.100
E	2.900	-	3.100
D1	2.300	-	2.500
E1	1.550	-	1.750
e		0.500 BSC	
L	0.300	-	0.500
eee		0.080	

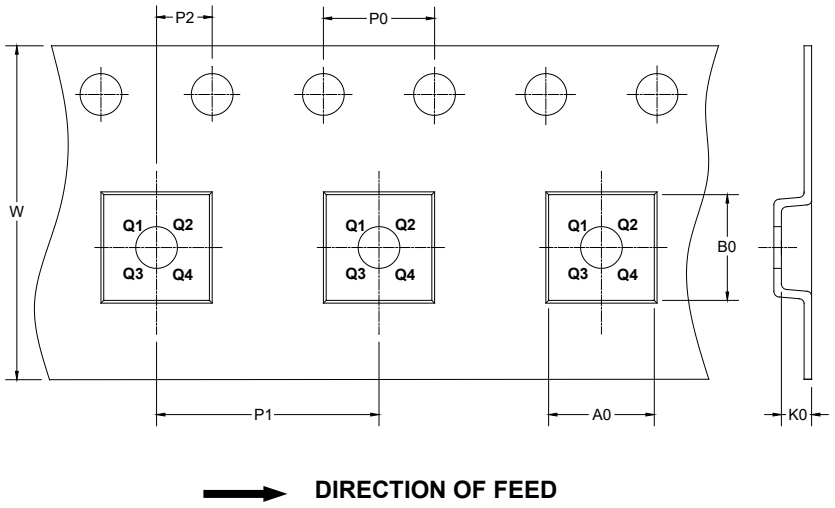
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



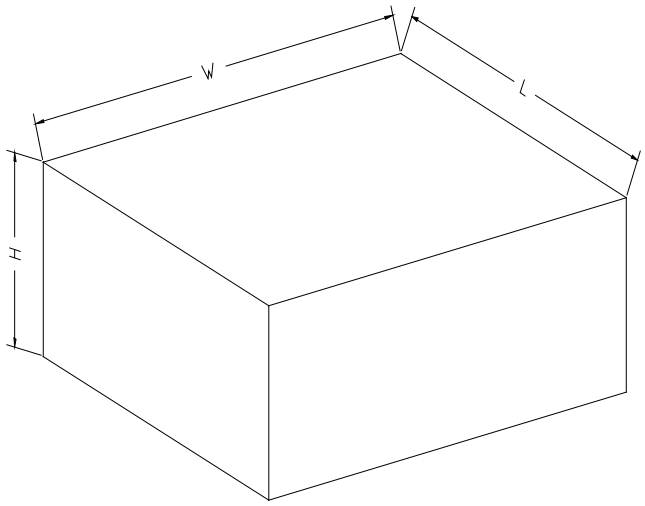
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10AL	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002