SGM8212-1/SGM8212-2
Low Noise, High Voltage Operational Amplifiers

GENERAL DESCRIPTION

The single SGM8212-1 and dual SGM8212-2 are low noise operational amplifiers optimized for high voltage operation. These devices operate from 2.7V to 36V single supply or ±1.35V to ±18V dual power supplies, and consume low quiescent current. They provide rail-to-rail input with a wide input common mode voltage range from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V, and rail-to-rail output voltage swing. However, the performance is reduced within 2V of the top rail.

The SGM8212-1/2 also feature low offset voltage and high gain-bandwidth product.

The SGM8212-1 is available in Green SOT-553-5, SOT-23-5 and SOIC-8 packages. The SGM8212-2 is available in Green SOIC-8, MSOP-8 and TDFN-3×3-8L packages. They are specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Input Offset Voltage: 1.8mV (MAX)**
- **Low Input Bias Current: 5pA (TYP)**
- **High CMRR: 98dB (TYP)**
- **Unity-Gain Stable**
- **Gain-Bandwidth Product: 2.5MHz**
- **Phase Margin: 60° for G = 1 and C_L = 10pF**
- **Low Noise: 15nV/$\sqrt{Hz}$ at 1kHz**
- **Rail-to-Rail Input and Output**
- **Support Single or Dual Power Supplies: 2.7V to 36V or ±1.35V to ±18V**
- **Low Quiescent Current: 475μA/Amplifier**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8212-1 Available in Green SOT-553-5, SOT-23-5 and SOIC-8 Packages
  SGM8212-2 Available in Green SOIC-8, MSOP-8 and TDFN-3×3-8L Packages

APPLICATIONS

Battery-Powered Equipment
Strain Gauge Amplifiers
Bridge Amplifiers
Transducer Amplifiers
Precision Integrators

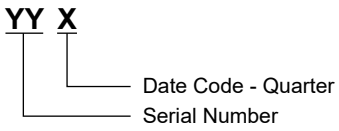
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8212-1	SOT-553-5	-40℃ to +125℃	SGM8212-1XKB5G/TR	MFX	Tape and Reel, 4000
	SOT-23-5	-40℃ to +125℃	SGM8212-1XN5G/TR	R12XX	Tape and Reel, 3000
	SOIC-8	-40℃ to +125℃	SGM8212-1XS8G/TR	SGM 82121XS8 XXXXX	Tape and Reel, 4000
SGM8212-2	SOIC-8	-40℃ to +125℃	SGM8212-2XS8G/TR	SGM 82122XS8 XXXXX	Tape and Reel, 4000
	MSOP-8	-40℃ to +125℃	SGM8212-2XMS8G/TR	SGM07C XMS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-8L	-40℃ to +125℃	SGM8212-2XTDB8G/TR	SGM 82122DB XXXXX	Tape and Reel, 4000

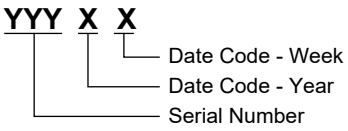
MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

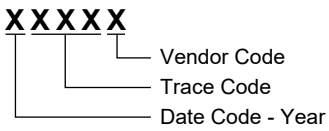
SOT-553-5



SOT-23-5



SOIC-8/MSOP-8/TDFN-3×3-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Differential Input Voltage, $|V_{ID}|$ ..... $(+V_S)$ - $(-V_S)$
Input/Output Voltage Range..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (SGM8212-1) 2500V
HBM (SGM8212-2) 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

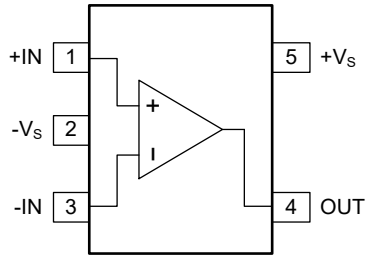
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

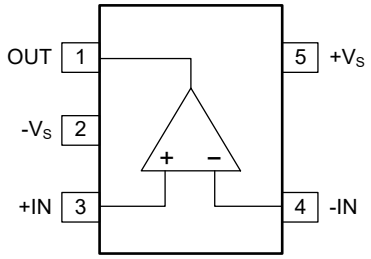
PIN CONFIGURATIONS

SGM8212-1 (TOP VIEW)



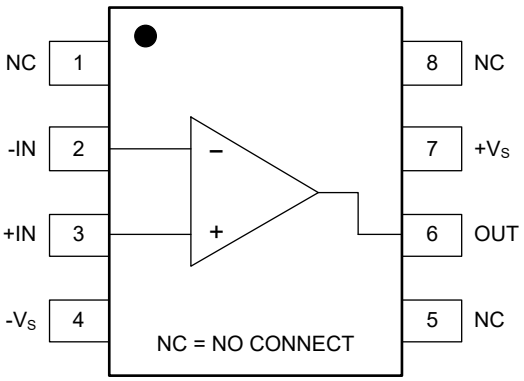
SOT-553-5

SGM8212-1 (TOP VIEW)



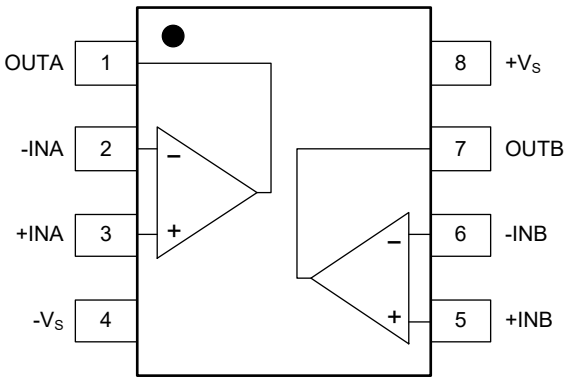
SOT-23-5

SGM8212-1 (TOP VIEW)



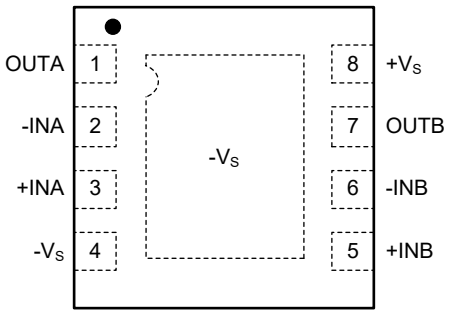
SOIC-8

SGM8212-2 (TOP VIEW)



SOIC-8/MSOP-8

SGM8212-2 (TOP VIEW)



TDFN-3×3-8L

NOTE: For the TDFN-3×3-8L package, exposed pad can be connected to $-V_S$ or left floating.

ELECTRICAL CHARACTERISTICS

(V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}	V_{CM} = 0V	+25℃		0.4	1.8	mV
			Full			2	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		1.1		μV/℃
Input Bias Current	I_B	V_{CM} = 0V	+25℃		±5	±120	pA
Input Offset Current	I_{OS}	V_{CM} = 0V	+25℃		±5	±120	pA
Maximum Input Difference Bias Current	$I I_{ID} I$	V_S = ±18V, V_{ID} = ±18V	+25℃		2	3	μA
			Full			4	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio	CMRR	V_S = ±2V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V	+25℃	63	80		dB
			Full	60			
		V_S = ±2V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ - 2V	+25℃	78	94		
			Full	75			
		V_S = ±18V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ + 0.1V	+25℃	83	98		
			Full	80			
		V_S = ±18V, $(-V_S)$ - 0.1V < V_{CM} < $(+V_S)$ - 2V	+25℃	100	115		
			Full	97			
Open-Loop Voltage Gain	A_{OL}	V_S = ±2V, $(-V_S)$ + 0.35V < V_{OUT} < $(+V_S)$ - 0.35V	+25℃	103	130		dB
			Full	100			
		V_S = ±18V, $(-V_S)$ + 0.35V < V_{OUT} < $(+V_S)$ - 0.35V	+25℃	123	140		
			Full	120			
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±18V	+25℃		110	150	mV
			Full			240	
Output Short-Circuit Current	I_{SC}	V_S = ±18V	+25℃	±16	±30		mA
Power Supply							
Operating Voltage Range	V_S		Full	2.7		36	V
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0A	+25℃		475	660	μA
			Full			720	
Power Supply Rejection Ratio	PSRR	V_S = 4V to 36V	+25℃	103	120		dB
			Full	100			

ELECTRICAL CHARACTERISTICS (continued)

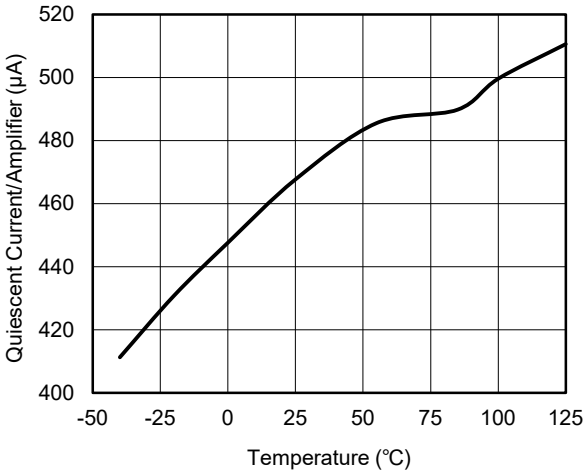
(V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP	C_L = 10pF	+25℃		2.5		MHz
Phase Margin	φ_O	C_L = 10pF	+25℃		60		°
Slew Rate	SR	V_S = ±2V to ±18V, G = +1	+25℃		1.5		V/μs
Settling Time to 0.1%	t_S	V_S = ±18V, G = +1, 10V step	+25℃		15		μs
Overload Recovery Time	ORT	V_{IN} × G > V_S	+25℃		2		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 36V, V_{OUT} = $3V_{RMS}$, f = 1kHz, G = +1	+25℃		0.0002		%
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		2.5		μV_{P-P}
Input Voltage Noise Density	e_n	f = 100Hz	+25℃		25		$nV/\sqrt{Hz}$
		f = 1kHz	+25℃		15		
Input Current Noise Density	i_n	f = 1kHz	+25℃		300		$fA/\sqrt{Hz}$

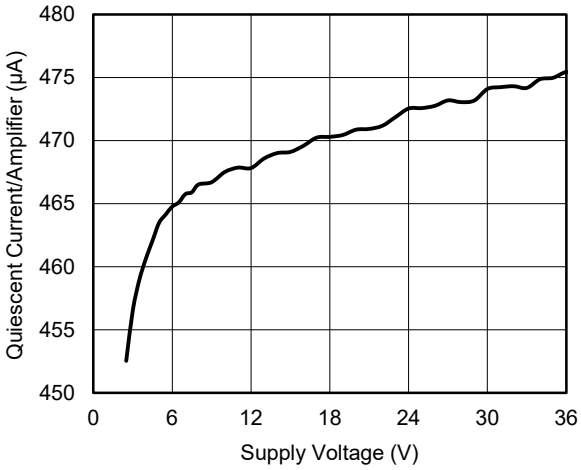
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

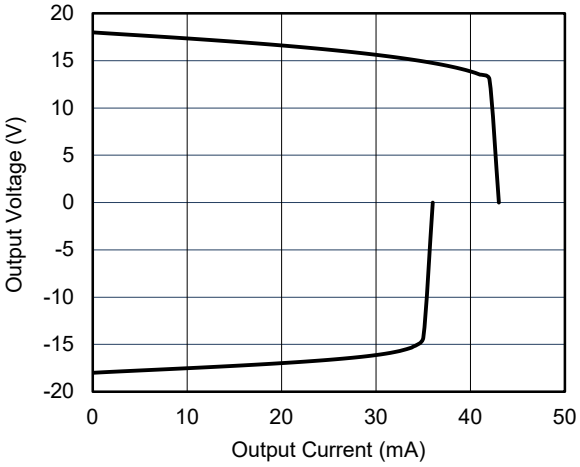
Quiescent Current vs. Temperature



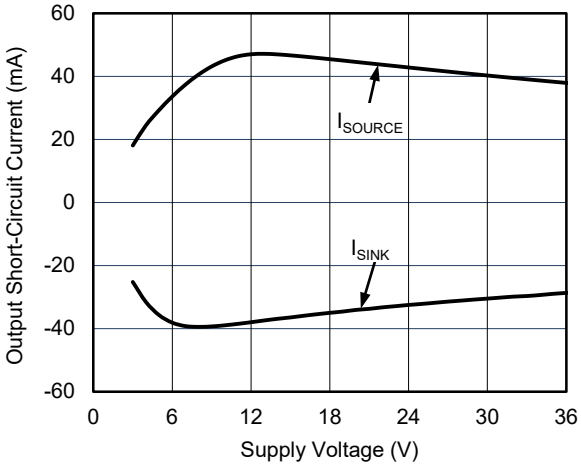
Quiescent Current vs. Supply Voltage



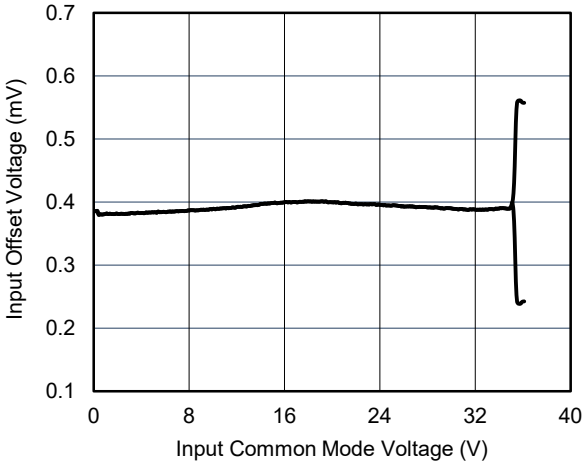
Output Voltage vs. Output Current



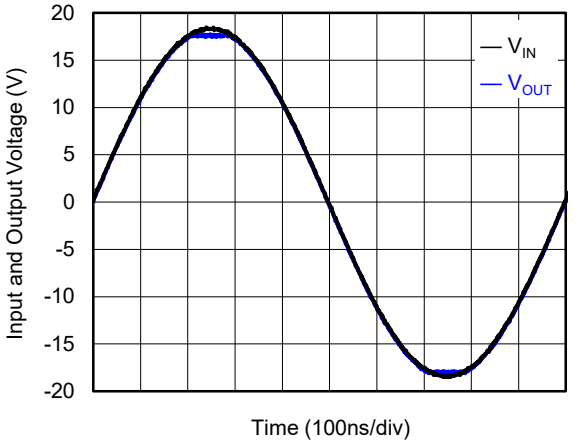
Output Short-Circuit Current vs. Supply Voltage



Input Offset Voltage vs. Input Common Mode Voltage



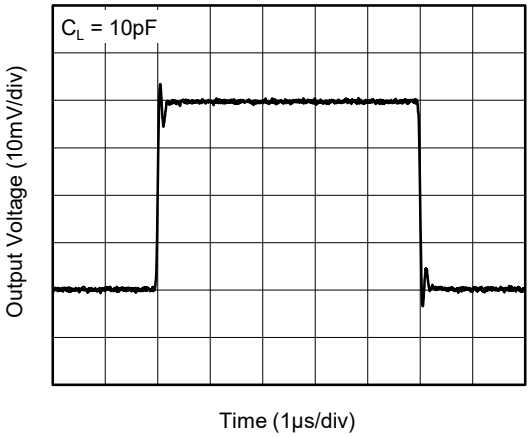
No Phase Reversal



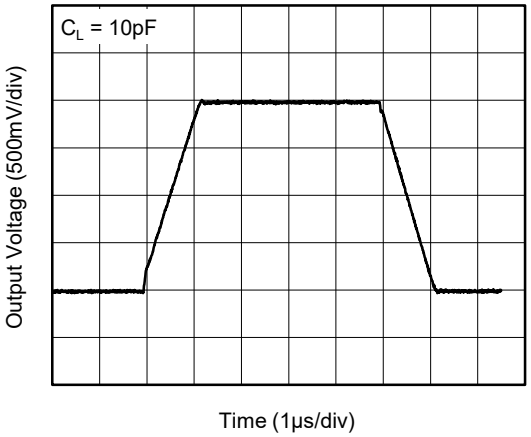
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

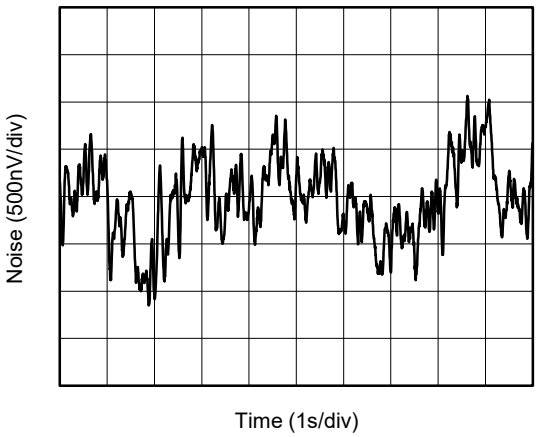
Small-Signal Step Response



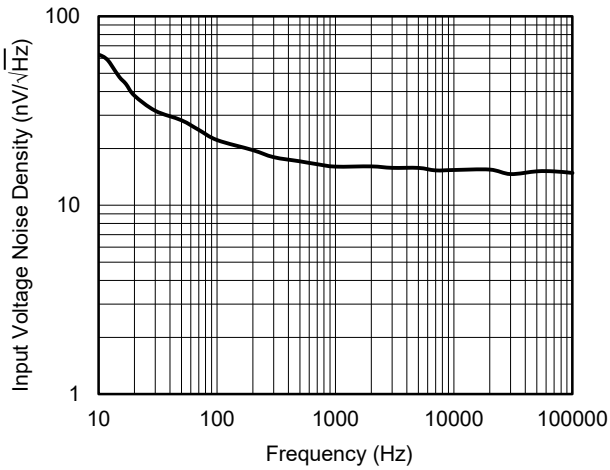
Large-Signal Step Response



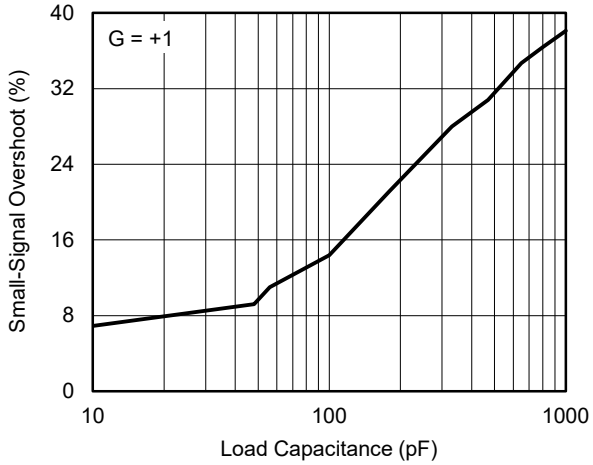
0.1Hz to 10Hz Input Voltage Noise



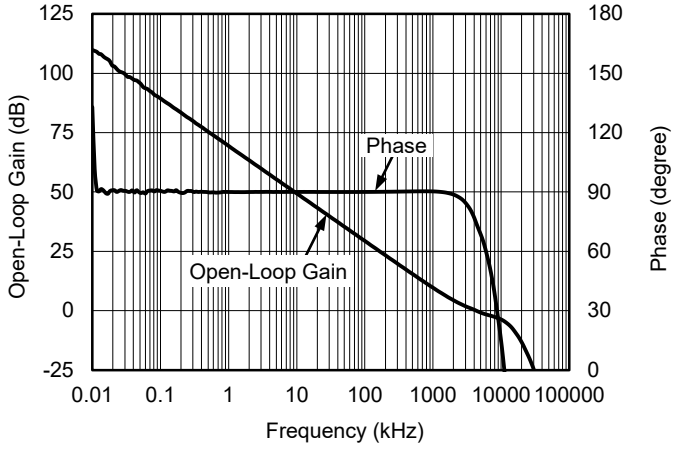
Input Voltage Noise Density vs. Frequency



Small-Signal Overshoot vs. Capacitive Load



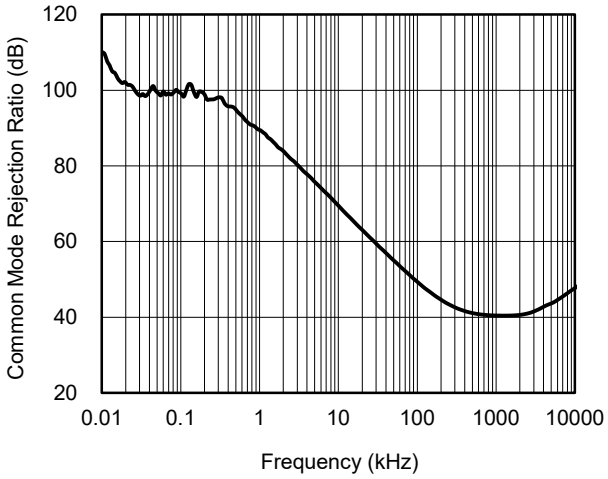
Open-Loop Gain and Phase vs. Frequency



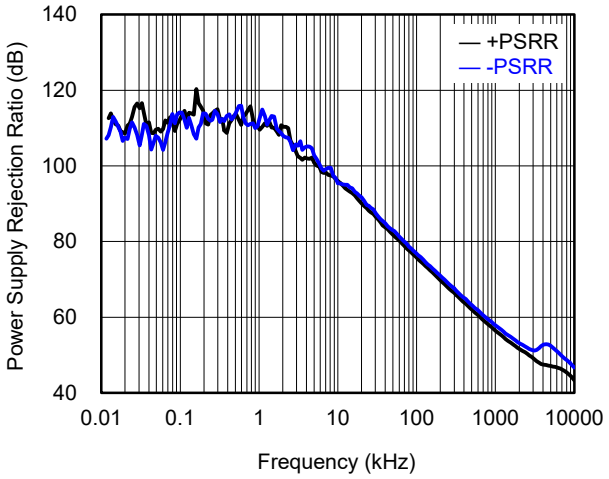
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.

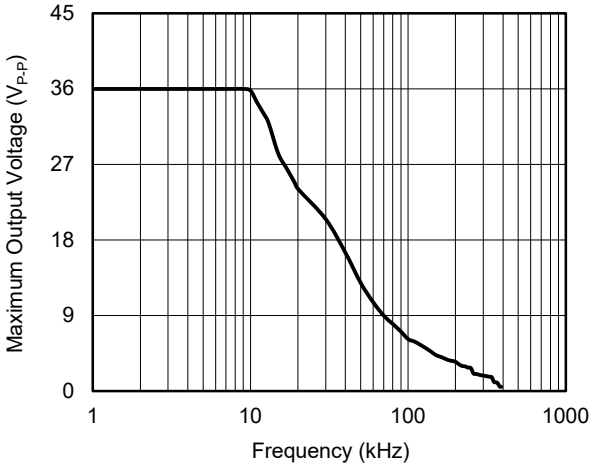
CMRR vs. Frequency



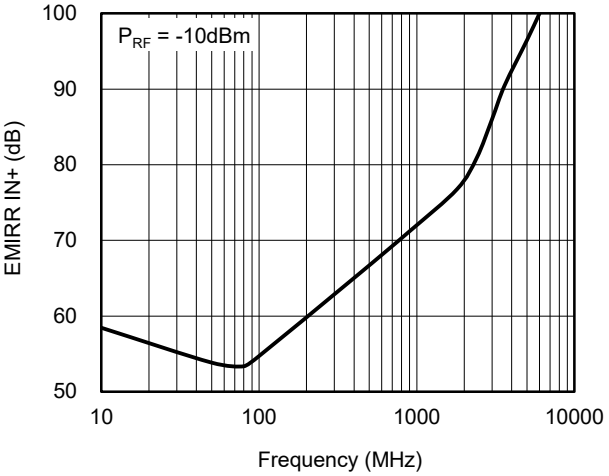
PSRR vs. Frequency



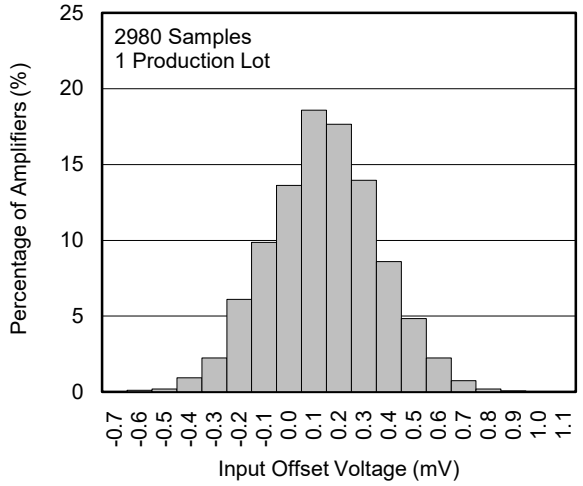
Maximum Output Voltage vs. Frequency



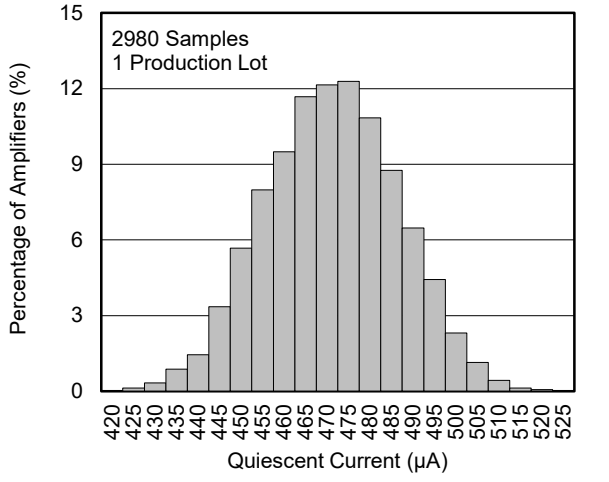
EMIRR IN+ vs. Frequency



Input Offset Voltage Production Distribution

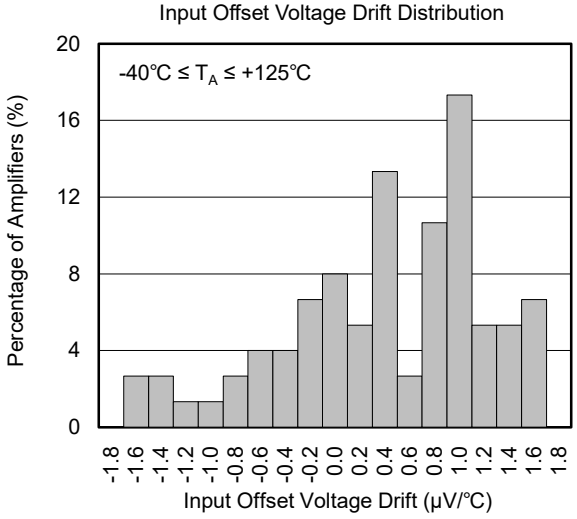


Quiescent Current Production Distribution



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±18V, R_L = 10kΩ, unless otherwise noted.



APPLICATION INFORMATION

Rail-to-Rail Input

When SGM8212-1/2 work at the power supply between 2.7V and 36V, the input common mode voltage range is from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage not to exceed the rails.

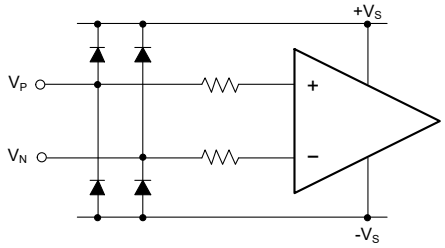


Figure 1. Input Equivalent Circuit

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

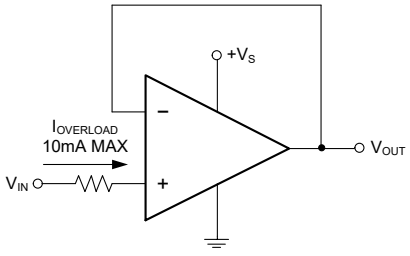


Figure 2. Input Current-Limit Protection

Rail-to-Rail Output

The SGM8212-1/2 support rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 36V, $-V_S$ = GND, 10kΩ load resistor is tied from OUT pin to ground, the typical output swing range is from 0.11V to 35.89V.

Driving Capacitive Loads

The SGM8212-1/2 are designed for driving the 300pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

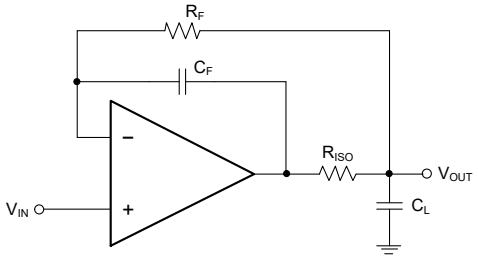


Figure 3. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifiers through $+V_S$ and $-V_S$ pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to $+V_S$ and $-V_S$ power supply pins.

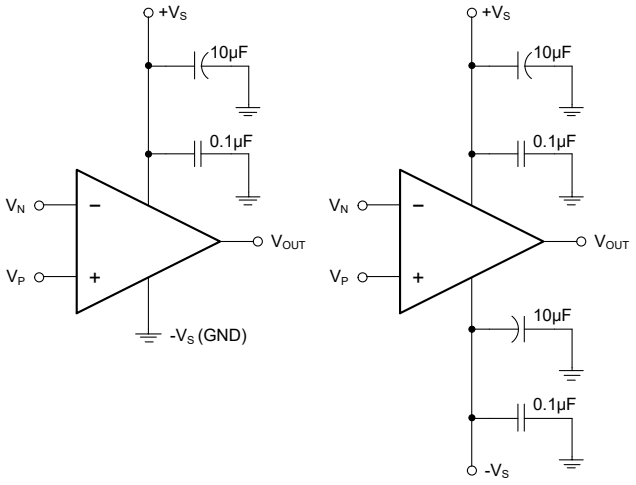


Figure 4. Amplifier Power Supply Bypassing

APPLICATION INFORMATION (continued)

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

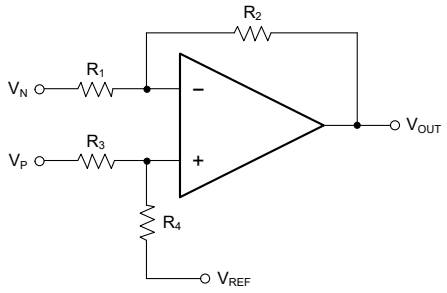


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier, the added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

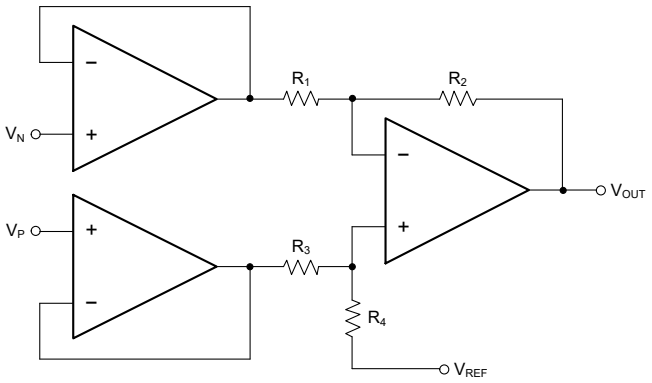


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/2\pi R_2C$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

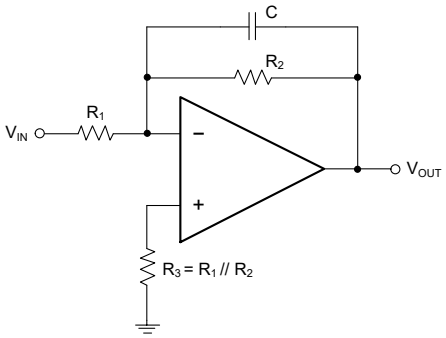


Figure 7. Active Low-Pass Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2023 – REV.A to REV.A.1	Page
Added SGM8212-2XMS8G	All
Updated Absolute Maximum Ratings section	3
Updated Electrical Characteristics section	5
Updated Typical Performance Characteristics section	9

Changes from Original (DECEMBER 2020) to REV.A	Page
Changed from product preview to production data	All