SGM38122
4-Channel LDO PMIC for Camera Applications

GENERAL DESCRIPTION

The SGM38122 is a 4-channel LDO PMIC, which has one low output DVDD channel and three high PSRR and low noise AVDD1/2/3 channels.

IN1 input voltage range is from 0.7V to 2.0V. IN2 input voltage range is from 2.5V to 5.5V. IN3 input voltage range is from 1.8V to V_{IN2}.

For DVDD, the SGM38122 uses NMOS architecture without a charge pump. IN1 is used as an input source and IN2 is used as bias voltage. The DVDD output range is from 0.528V to 1.8V. It is capable of supplying 1400mA output current with ultra-low dropout voltage.

For AVDD1/2/3, the SGM38122 uses PMOS architecture with IN2 and IN3 as an input source. All of them can supply 1.504V to 3.424V output voltage with high PSRR performance. The output current limit is 350mA.

The SGM38122 has an external EN pin and internal enable bits. Other features include high resolution output voltage configuration and adjustable hiccup function during OCP. The SGM38122 has automatic discharge function to quickly discharge V_{OUT} in the disabled status. Besides, the SGM38122 supports 1MHz I^2C interface with register address automatic increment for continuous writing.

The SGM38122 is qualified for phone camera sensors, camera sensors on wearable device.

The SGM38122 is available in a Green WLCSP-1.15×1.52-12B package. It operates over an operating temperature range of -40℃ to +85℃.

FEATURES

- **DVDD Output Voltage Range: 0.528V to 1.8V at 8mV per Step**
- **AVDD1/2/3 Output Voltage Range: 1.504V to 3.424V at 8mV per Step**
- **IN1 Input Voltage Range: 0.7V to 2.0V**
- **IN2 Input Voltage Range: 2.5V to 5.5V**
- **IN3 Input Voltage Range: 1.8V to V_{IN2}**
- **Output Voltage Accuracy: ±1%**
- **AVDD1/2/3 Output Current: 350mA**
- **DVDD Output Current: 1400mA**
- **DVDD Dropout Voltage: 100mV (TYP) at 1200mA**
- **IN2 Supply Quiescent Current: 240μA (TYP)**
- **IN2 Shutdown Current: 0.23μA (TYP)**
- **IN2 UVLO: 2.15V (TYP), Hysteresis: 100mV (TYP)**
- **AVDD1/2 to VIN2 PSRR at 100mA:**
  - **105dB (TYP) at 1kHz**
  - **85dB (TYP) at 100kHz**
  - **55dB (TYP) at 1MHz**
- **AVDD3 to VIN3 PSRR at 100mA:**
  - **105dB (TYP) at 1kHz**
  - **90dB (TYP) at 100kHz**
  - **55dB (TYP) at 1MHz**
- **AVDD1/2/3 LDO Output Noise: 9μV_{RMS} (TYP)**
- **Programmable Power Up Sequence**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green WLCSP-1.15×1.52-12B Package**

APPLICATIONS

Camera Sensor

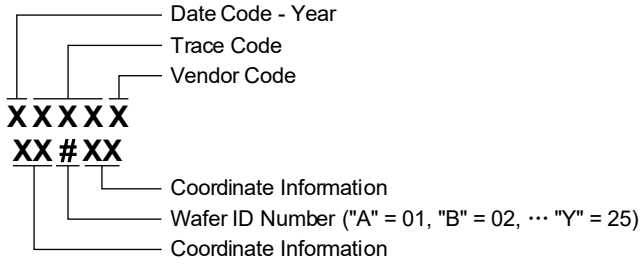
Smart Phone

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38122	WLCSP-1.15×1.52-12B	-40℃ to +85℃	SGM38122YG/TR	38122 XXXXX XX#XX	Tape and Reel, 6000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{IN2} Range ..... -0.3V to 6.5V
V_{IN1}, V_{IN3} Range ..... -0.3V to V_{IN2}
V_{EN} Range ..... -0.3V to 6.5V
V_{OUT} Range (V_{DVDD}, $V_{AVDD1/2/3}$) .....
..... -0.3V to MIN[(V_{INX} + 0.3V), 6.5V]
Interrupt ..... -0.3V to 6.5V
Serial Clock, Serial Data ..... -0.3V to 6.5V
Package Thermal Resistance
WLCSP-1.15×1.52-12B, θ_{JA} ..... 79℃/W
WLCSP-1.15×1.52-12B, θ_{JB} ..... 26.3℃/W
WLCSP-1.15×1.52-12B, θ_{JC} ..... 33.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

IN1 Operating Supply Voltage Range ..... 0.7V to 2.0V
IN2 Operating Supply Voltage Range ..... 2.5V to 5.5V
IN3 Operating Supply Voltage Range ..... 1.8V to V_{IN2}
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

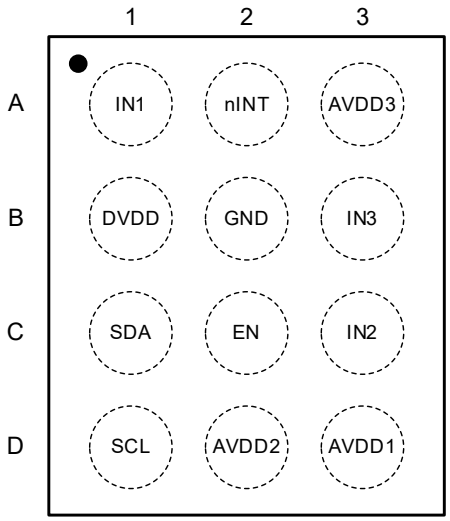
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.15×1.52-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	IN1	VIN for DVDD.
A2	nINT	Interface Pin for Interrupts. Open-drain output by default and keep high without faults.
A3	AVDD3	AVDD3 Regulated Output.
B1	DVDD	DVDD Regulated Output.
B2	GND	Ground for All Circuits.
B3	IN3	VIN for AVDD3.
C1	SDA	I^2C Communication Bus Data Signal.
C2	EN	Enable Pin. Set high to enable I^2C communication. Otherwise, reset all outputs and registers.
C3	IN2	VIN for AVDD1/2 and Bias for DVDD and AVDD3.
D1	SCL	I^2C Communication Bus Clock Signal.
D2	AVDD2	AVDD2 Regulated Output.
D3	AVDD1	AVDD1 Regulated Output.

FUNCTIONAL BLOCK DIAGRAM

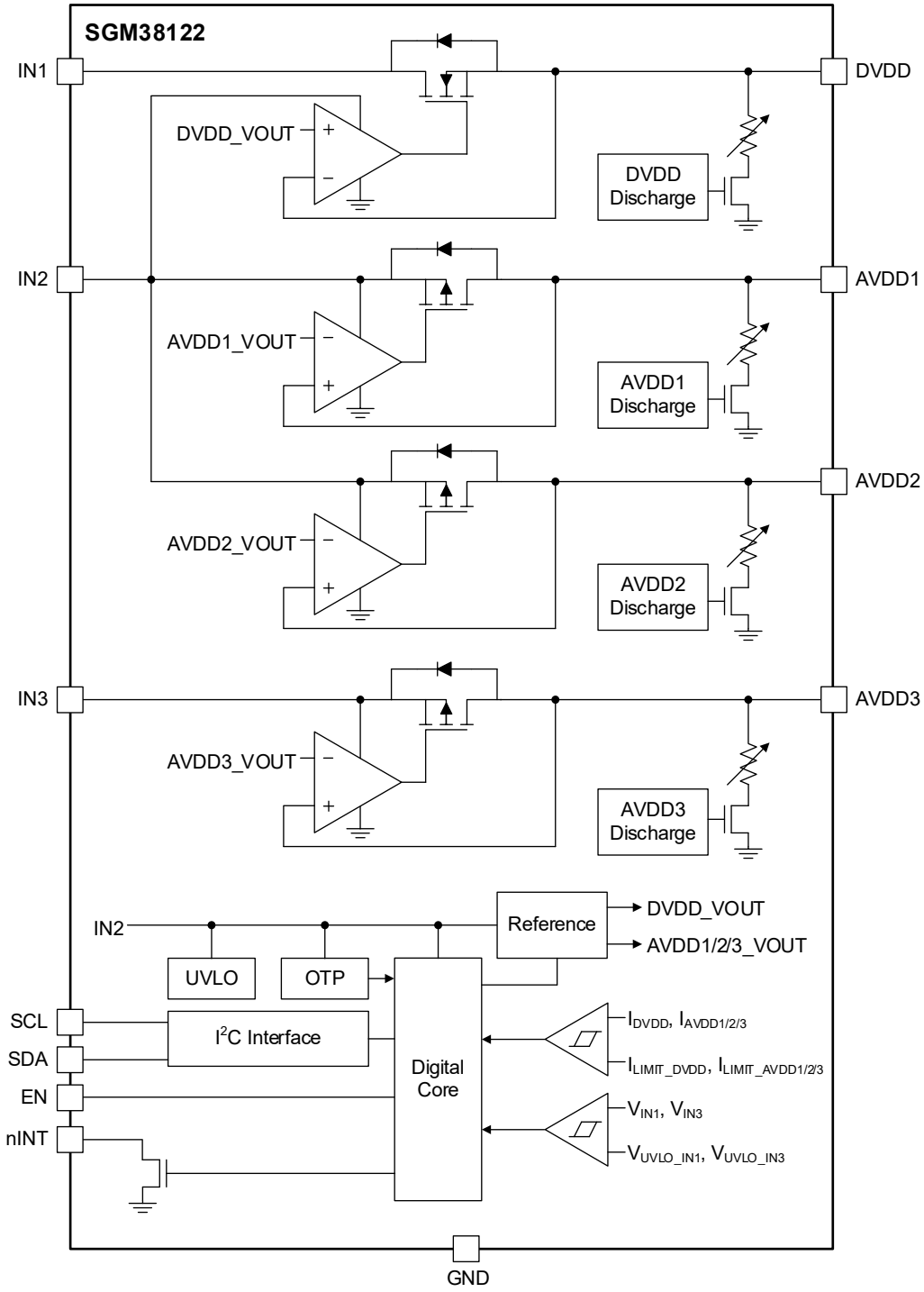


Figure 1. Block Diagram

TYPICAL APPLICATION

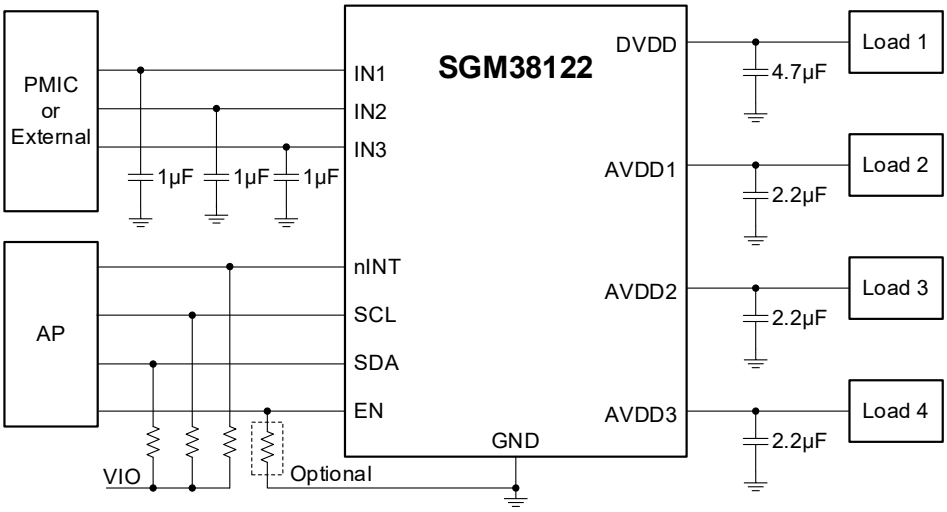


Figure 2. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, at V_{IN2} = 2.5V to 5.5V and V_{IN2} ≥ (V_{DVDD} + 1.6V) and ($V_{AVDD1/2/3}$ + 0.2V), at V_{IN1} = 0.7V to 2.0V and V_{IN1} ≥ (V_{DVDD} + 0.15V), at V_{IN3} = 1.8V to V_{IN2} and V_{IN3} ≥ (V_{AVDD3} + 0.2V). Typical values are measured at T_A = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Whole Device						
Quiescent Current	I_Q	EN pin high, all LDOs on with no load	140	240	370	μA
Sleep Mode Supply Current	I_{SLP}	EN pin high, EN_REF = L	0.3	1.75	5.5	μA
Standby Mode Supply Current	$I_{STANDBY}$	EN pin high, EN_REF = H, EN_DVDD/AVDD1/2/3 = 0	15	35	55	μA
Shutdown Current	I_{SHDN}		0.1	0.23	2.5	μA
EN Logic High Voltage	V_{ENH}		0.8			V
EN Logic Low Voltage	V_{ENL}				0.4	V
EN Pin Internal Pull-Down Resistor	R_{EN}			2.3		MΩ
Thermal Shutdown Threshold	T_{SHDN}	I_{OUT} = 1mA		140		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}	I_{OUT} = 1mA		15		℃
Output Discharge Resistor On-Resistance	R_{DCHG_DVDD}	DVDD_DISCH_SET = 0		250		Ω
		DVDD_DISCH_SET = 1		125		
	$R_{DCHG\_AVDD1/2/3}$	AVDD1/2/3_DISCH_SET = 0		250		
		AVDD1/2/3_DISCH_SET = 1		125		
Under-Voltage Lockout Threshold	$V_{UVLO\_RS\_IN1}$	Rising V_{IN1}	0.51	0.56	0.61	V
	$V_{UVLO\_FL\_IN1}$	Falling V_{IN1}	0.42	0.46	0.5	
	$V_{UVLO\_RS\_IN2}$	Rising V_{IN2}	2.15	2.25	2.40	
	$V_{UVLO\_FL\_IN2}$	Falling V_{IN2}	2.07	2.15	2.19	
	$V_{UVLO\_RS\_IN3}$	Rising V_{IN3}	1.59	1.65	1.72	
	$V_{UVLO\_FL\_IN3}$	Falling V_{IN3}	1.50	1.55	1.61	
LDO1 (DVDD)						
Input Voltage Range	V_{IN1}		0.7	1.35	2.0	V
Output Voltage Range	V_{DVDD}		0.528		1.800	V
Default Output Voltage	V_{DVDD}			1.2		V
Output Voltage Step Size				8		mV
Output Capacitance	C_{DVDD}		4.7			μF
Output Voltage Accuracy	V_{ACC_DVDD}	I_{DVDD} = 10mA, V_O = 0.744V to 1.800V	-1		+1	%
		I_{DVDD} = 10mA, V_O = 0.528V to 0.744V	-1.3		+1.3	
Dropout Voltage	V_{DROP_DVDD}	V_{IN2} = 3.8V, V_{DVDD} = 1.2V, I_{DVDD} = 1200mA	40	100	140	mV
		V_{IN2} = 3.2V, V_{DVDD} = 1.2V, I_{DVDD} = 500mA	10	50	80	
Output Current Limit	I_{LIMIT_DVDD}		1400		2300	mA
Turn-On Time	t_{ON_DVDD}	EN_REF = 1, from the EN bit assertion to the V_{OUT} start ramp		140		μs
Soft-Start Time	t_{SS_DVDD}	V_{DVDD} from 0% to 95%, I_{DVDD} = 10mA		200		μs
Startup Fault Disable Timer	t_{SUFD_DVDD}	Disable fault detection timer		1.5		ms
Hiccup Timer	t_{Hiccup}	Protection shutdown to recovery startup timer		17		ms
Load Regulation	ΔV_{LOAD_DVDD}	I_{DVDD} = 1mA to 300mA		1		mV
Line Regulation	ΔV_{LINE_DVDD}	V_{IN1} = 1.35V to 2V, I_{DVDD} = 10mA		0.1		mV
		V_{IN2} = 3V to 5.5V, I_{DVDD} = 10mA		0.1		
Output Voltage Noise	e_{n_DVDD}	f = 10Hz to 100kHz, I_{DVDD} = 100mA		26		μV_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, at V_{IN2} = 2.5V to 5.5V and V_{IN2} ≥ (V_{DVDD} + 1.6V) and ($V_{AVDD1/2/3}$ + 0.2V), at V_{IN1} = 0.7V to 2.0V and V_{IN1} ≥ (V_{DVDD} + 0.15V), at V_{IN3} = 1.8V to V_{IN2} and V_{IN3} ≥ (V_{AVDD3} + 0.2V). Typical values are measured at T_A = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	$PSRR_{\_VIN1\_DVDD}$	V_{IN1} = 1.5V + 0.2V_{P-P}, V_{IN2} = 3.8V, V_{DVDD} = 1.2V, I_{DVDD} = 150mA	f = 1kHz		85		dB
			f = 10kHz		65		
			f = 100kHz		45		
			f = 1MHz		40		
	$PSRR_{\_VIN2\_DVDD}$	V_{IN2} = 3.8V + 0.2V_{P-P}, V_{IN1} = 1.5V, V_{DVDD} = 1.2V, I_{DVDD} = 150mA	f = 1kHz		80		dB
			f = 10kHz		80		
			f = 100kHz		70		
			f = 1MHz		50		
LDO2, LDO3, LDO4 (AVDD1/2/3)							
Input Voltage Range	V_{IN2}			2.5	3.8	5.5	V
Input Voltage Range	V_{IN3}			1.8	3.8	V_{IN2}	V
Output Voltage Range	$V_{AVDD1/2/3}$			1.504		3.424	V
Default Output Voltage	$V_{AVDD1/2/3}$				2.8		V
Output Voltage Step Size					8		mV
Output Capacitance	$C_{AVDD1/2/3}$			2.2			μF
Output Voltage Accuracy	$V_{ACC\_AV1/2/3}$	$I_{AVDD1/2/3}$ = 10mA, $V_{AVDD1/2/3}$ = 1.504V to 3.424V		-0.8		+0.8	%
Dropout Voltage	$V_{DROP\_AV1/2/3}$	$V_{AVDD1/2/3}$ = 2.8V, $I_{AVDD1/2/3}$ = 300mA		60	110	160	mV
		$V_{AVDD1/2/3}$ = 3.0V, $I_{AVDD1/2/3}$ = 300mA		50	105	150	
Output Current Limit	$I_{LIMIT\_AV1/2/3}$	$V_{IN2/3}$ ≥ $V_{AVDD1/2/3}$ + 0.3V, $V_{AVDD1/2/3}$ ≥ 2.0V		350		700	mA
		$V_{IN2/3}$ ≥ $V_{AVDD1/2/3}$ + 0.5V, $V_{AVDD1/2/3}$ ≥ 1.5V		350		700	
Turn-On Time	$t_{ON\_AV1/2/3}$	EN_REF = 1, from the EN bit assertion to the V_{OUT} start ramp			320		μs
Soft-Start Time	$t_{SS\_AV1/2/3}$	$V_{AVDD1/2/3}$ from 0% to 95%, $I_{AVDD1/2/3}$ = 10mA			350		μs
Startup Fault Disable Timer	$t_{SUFD\_AV1/2/3}$	Disable fault detection timer			1.5		ms
Hiccup Timer	t_{HICCUP}	Protection shutdown to recovery startup timer			17		ms
Load Regulation	$\Delta V_{LOAD\_AV1/2/3}$	$I_{AVDD1/2/3}$ = 1mA to 200mA			1		mV
Line Regulation	$\Delta V_{LINE\_AV1/2/3}$	$V_{IN2/3}$ = 3V to 5.5V, $I_{AVDD1/2/3}$ = 10mA			0.1		mV
Output Voltage Noise	$e_{n\_AV1/2/3}$	f = 10Hz to 100kHz, $I_{AVDD1/2/3}$ = 100mA			9		μV_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

(Minimum and Maximum values are measured at T_J = -40℃ to +85℃, at V_{IN2} = 2.5V to 5.5V and V_{IN2} ≥ (V_{DVDD} + 1.6V) and ($V_{AVDD1/2/3}$ + 0.2V), at V_{IN1} = 0.7V to 2.0V and V_{IN1} ≥ (V_{DVDD} + 0.15V), at V_{IN3} = 1.8V to V_{IN2} and V_{IN3} ≥ (V_{AVDD3} + 0.2V). Typical values are measured at T_A = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	$PSRR_{\_VIN2\_AV1/2}$	V_{IN2} = 4.0V + 0.2V_{P-P}, V_{IN3} = 3.8V, $V_{AVDD1/2}$ = 2.8V, $I_{AVDD1/2}$ = 100mA	f = 1kHz		105		dB
			f = 10kHz		94		
			f = 100kHz		85		
			f = 1MHz		55		
	$PSRR_{\_VIN2\_AV3}$	V_{IN2} = 4.0V + 0.2V_{P-P}, V_{IN3} = 3.8V, V_{AVDD3} = 2.8V, I_{AVDD3} = 100mA	f = 1kHz		110		dB
			f = 10kHz		100		
			f = 100kHz		85		
			f = 1MHz		65		
	$PSRR_{\_VIN3\_AV3}$	V_{IN2} = 4.0V, V_{IN3} = 3.8V + 0.2V_{P-P}, V_{AVDD3} = 2.8V, I_{AVDD3} = 100mA	f = 1kHz		105		dB
			f = 10kHz		100		
			f = 100kHz		90		
			f = 1MHz		55		
I^2C I/O Stages and Bus Lines							
SDA and SCL Logic High threshold	V_{IH}	V_{DD} = 1.2V		0.8			V
SDA and SCL Logic Low threshold	V_{IL}	V_{DD} = 1.2V				0.4	V
SDA and SCL Input Capacitance	C_I					10	pF

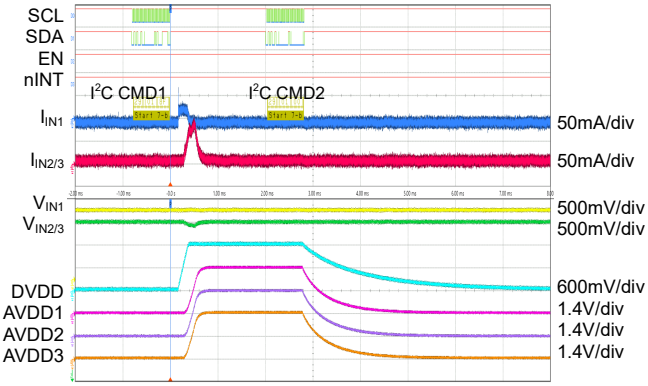
TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}				1000	kHz
START or Repeated Start Hold Time	t_{HDSTA}		0.26			μs
SCL Low Period	t_{LOW}		0.5			μs
SCL High Period	t_{HIGH}		0.26			μs
Repeated Start Setup Time	t_{SUSTA}		0.26			μs
Date Hold Time	t_{HDDAT}		0			μs
Data Setup Time	t_{SUDAT}		50			ns
SCL and SDA Rise Time	t_R				120	ns
SCL and SDA Fall Time	t_F				120	ns
STOP Condition Setup Time	t_{SUSTO}		0.26			μs
Bus-Free Time between STOP and START Conditions	t_{BUF}		0.5			μs
Capacitive Load for Each Bus Line	C_b				550	pF
Data Valid Time	t_{VDDAT}				0.45	μs
Data Valid Acknowledge Time	t_{VDACK}				0.45	μs

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.

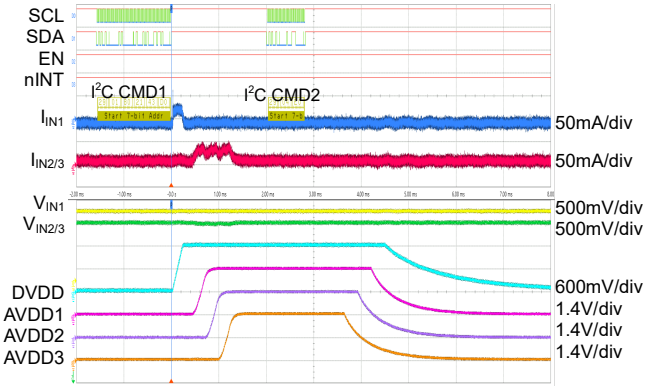
Startup and Shutdown of EN Bits



I_{DVDD} = 0mA, $I_{AVDD1/2/3}$ = 0mA, V_{IN1} = 1.5V,
Single-byte write CMD1 decoding: 29Wh-01h-8Fh
Single-byte write CMD2 decoding: 29Wh-01h-00h

Time (1ms/div)

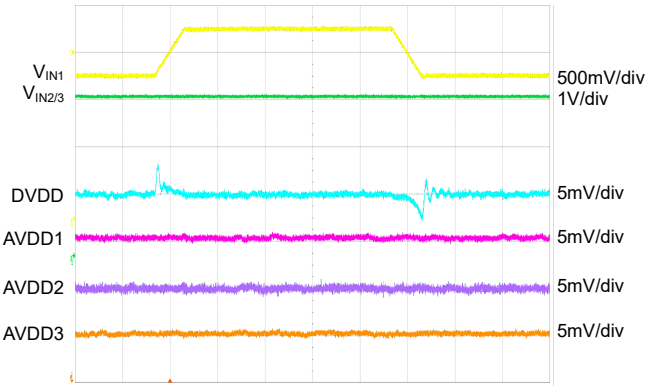
Startup and Shutdown of Sequence Control



I_{DVDD} = 0mA, $I_{AVDD1/2/3}$ = 0mA, V_{IN1} = 1.5V,
Multi-byte write CMD1 decoding: 29Wh-01h-80h-21h-43h-D0h
Single-byte write CMD2 decoding: 29Wh-04h-E0h

Time (1ms/div)

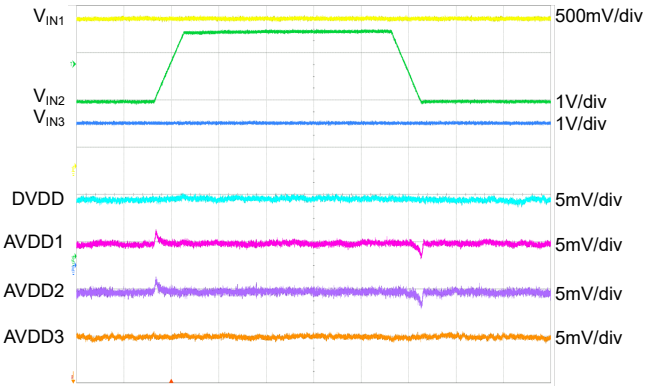
VIN1 Line Transient



I_{DVDD} = 1200mA, $I_{AVDD1/2/3}$ = 300mA, V_{IN1} = 1.5V to 2.0V,
V_{IN2} = V_{IN3} = 3.3V, t_R = t_F = 10μs

Time (20μs/div)

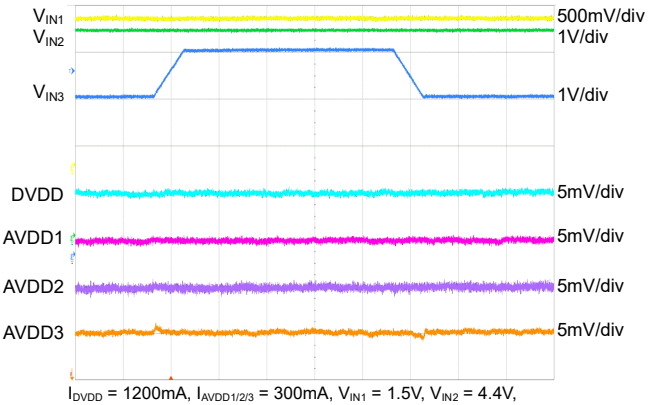
VIN2 Line Transient



I_{DVDD} = 1200mA, $I_{AVDD1/2/3}$ = 300mA, V_{IN1} = 1.5V,
V_{IN2} = 3.3V to 4.8V, V_{IN3} = 3.0V, t_R = t_F = 10μs

Time (20μs/div)

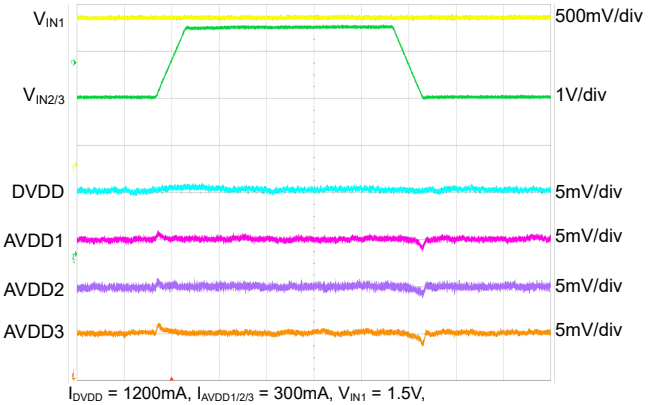
VIN3 Line Transient



I_{DVDD} = 1200mA, $I_{AVDD1/2/3}$ = 300mA, V_{IN1} = 1.5V, V_{IN2} = 4.4V,
V_{IN3} = 3.3V to 4.3V, t_R = t_F = 10μs

Time (20μs/div)

VIN2&3 Line Transient



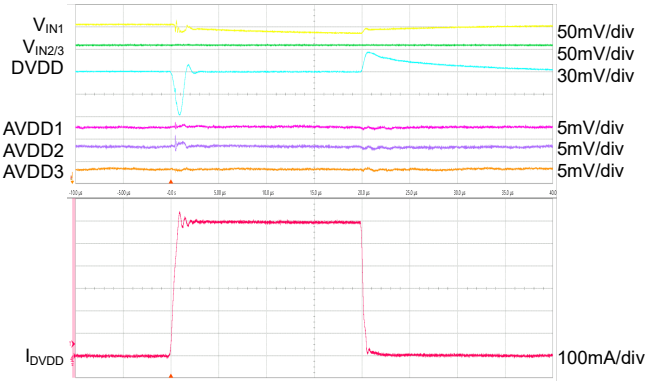
I_{DVDD} = 1200mA, $I_{AVDD1/2/3}$ = 300mA, V_{IN1} = 1.5V,
V_{IN2} = V_{IN3} = 3.3V to 4.8V, t_R = t_F = 10μs

Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.

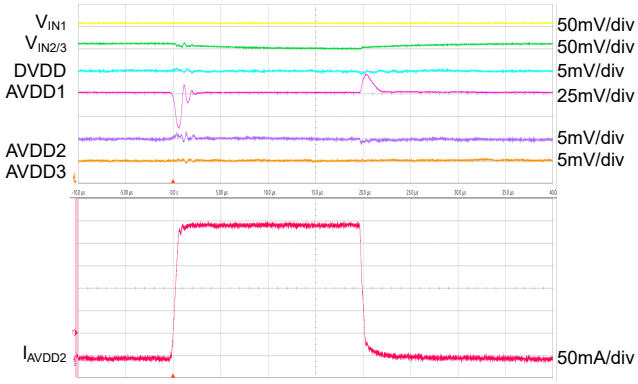
DVDD Load Transient



I_{DVDD} = 1mA to 600mA, $I_{AVDD1/2/3}$ = 300mA, V_{IN1} = 1.5V, t_R = t_F = 1μs

Time (5μs/div)

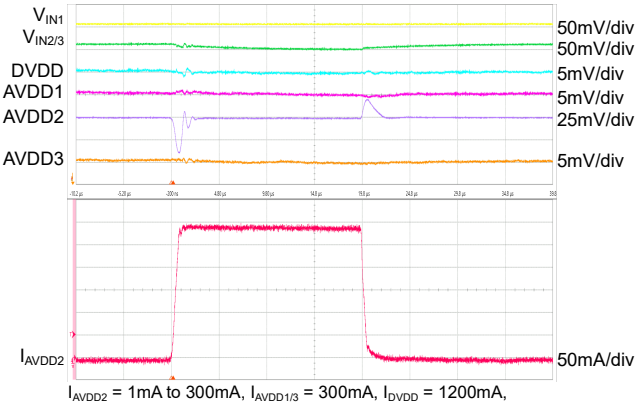
AVDD1 Load Transient



I_{AVDD1} = 1mA to 300mA, $I_{AVDD2/3}$ = 300mA, I_{DVDD} = 1200mA, V_{IN1} = 1.5V, t_R = t_F = 1μs

Time (5μs/div)

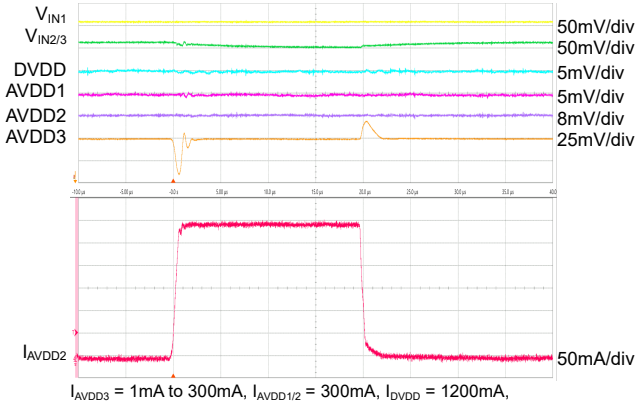
AVDD2 Load Transient



I_{AVDD2} = 1mA to 300mA, $I_{AVDD1/3}$ = 300mA, I_{DVDD} = 1200mA, V_{IN1} = 1.5V, t_R = t_F = 1μs

Time (5μs/div)

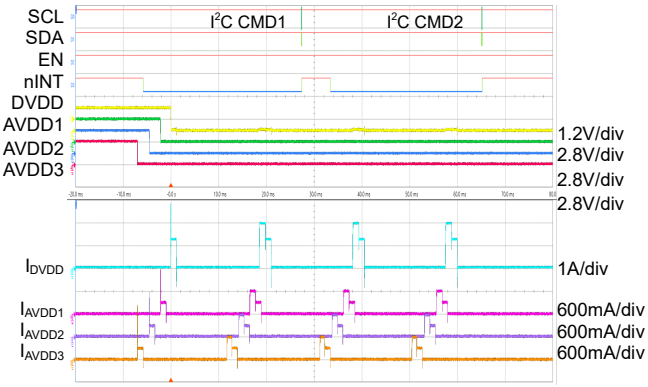
AVDD3 Load Transient



I_{AVDD3} = 1mA to 300mA, $I_{AVDD1/2}$ = 300mA, I_{DVDD} = 1200mA, V_{IN1} = 1.5V, t_R = t_F = 1μs

Time (5μs/div)

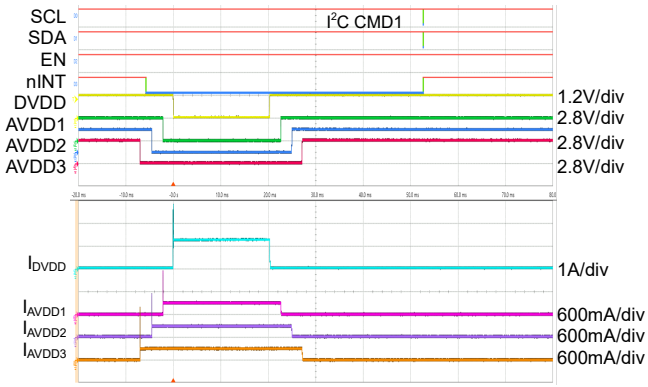
Short Protection in Hiccup Mode



$I_{DVDD/AVDD1/2/3}$ = 0mA to short, V_{IN1} = 1.5V, 0x0A[4] = 0,
Single-byte read CMD1 decoding: 29Rh-0Bh-0Fh
Single-byte read CMD2 decoding: 29Rh-0Bh-0Fh

Time (10ms/div)

Short Protection in Constant Current Mode



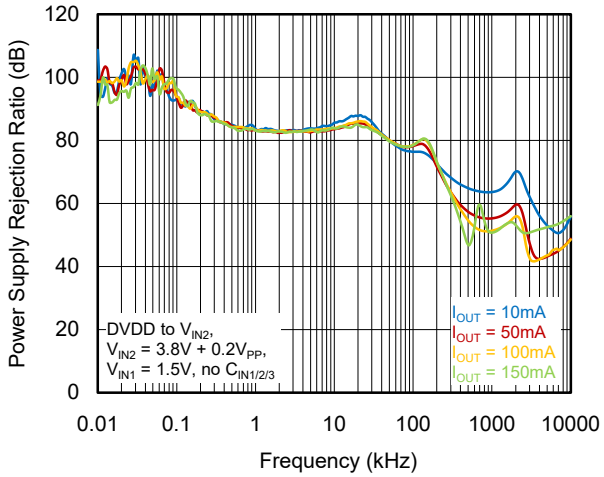
$I_{DVDD/AVDD1/2/3}$ = 0mA to short to 0mA, V_{IN1} = 1.5V, 0x0A[4] = 1,
Single-byte read CMD1 decoding: 29Rh-0Bh-0Fh

Time (10ms/div)

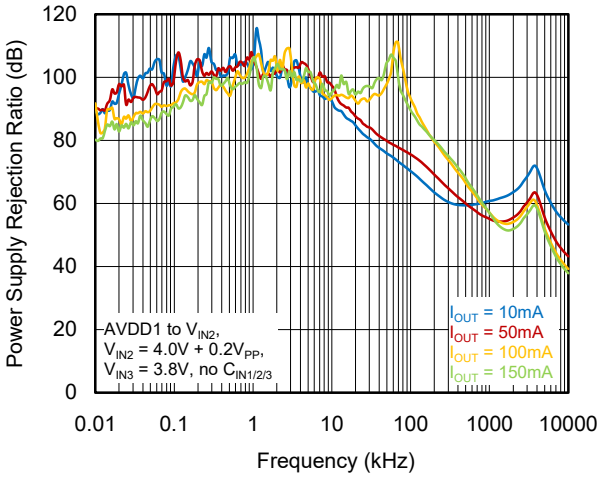
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.

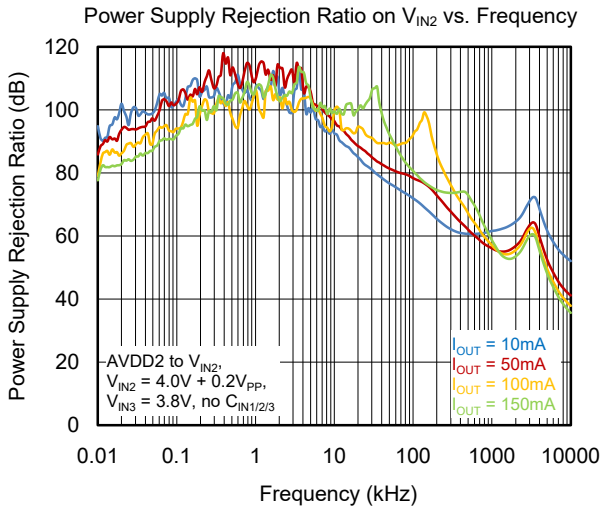
Power Supply Rejection Ratio on V_{IN2} vs. Frequency



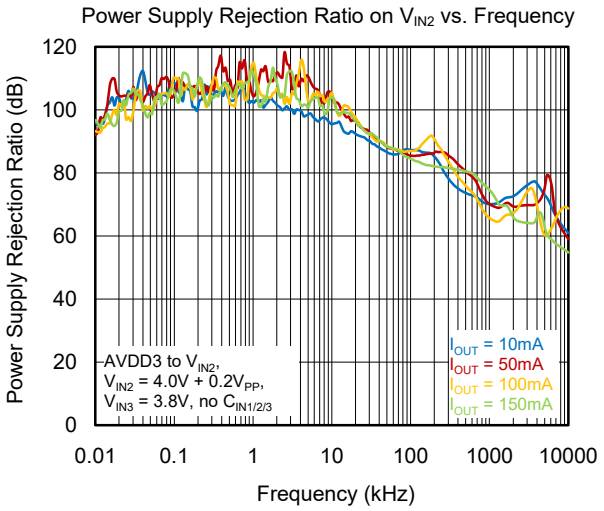
Power Supply Rejection Ratio on V_{IN2} vs. Frequency



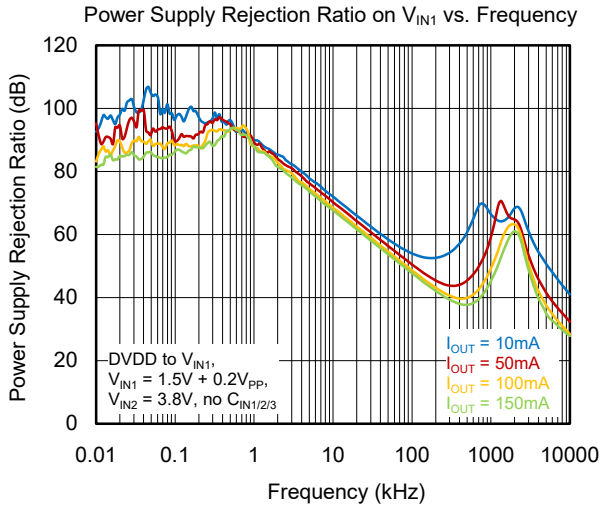
Power Supply Rejection Ratio on V_{IN2} vs. Frequency



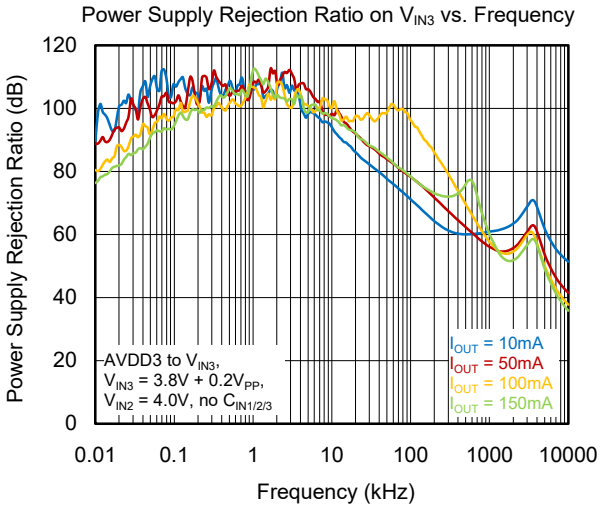
Power Supply Rejection Ratio on V_{IN2} vs. Frequency



Power Supply Rejection Ratio on V_{IN1} vs. Frequency



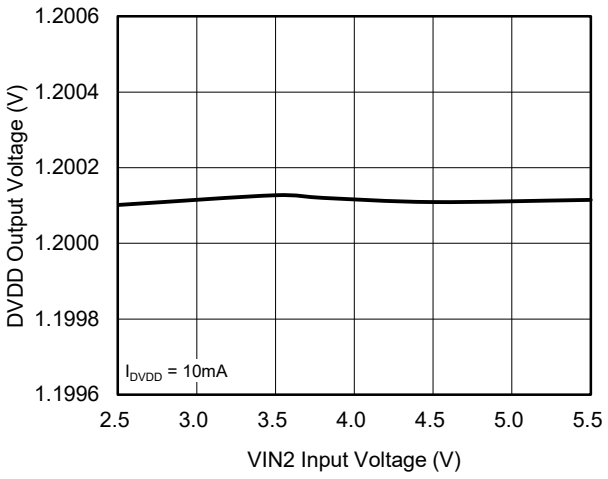
Power Supply Rejection Ratio on V_{IN3} vs. Frequency



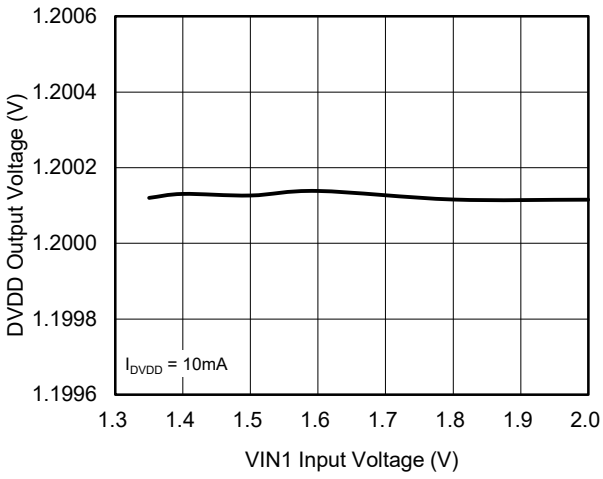
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.

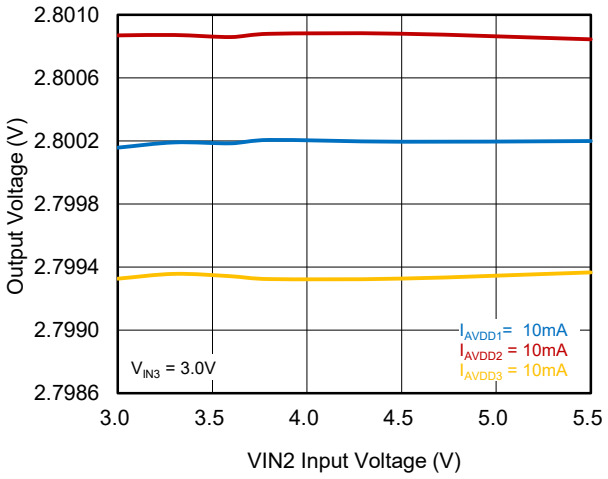
DVDD Output Voltage vs. VIN2 Input Voltage



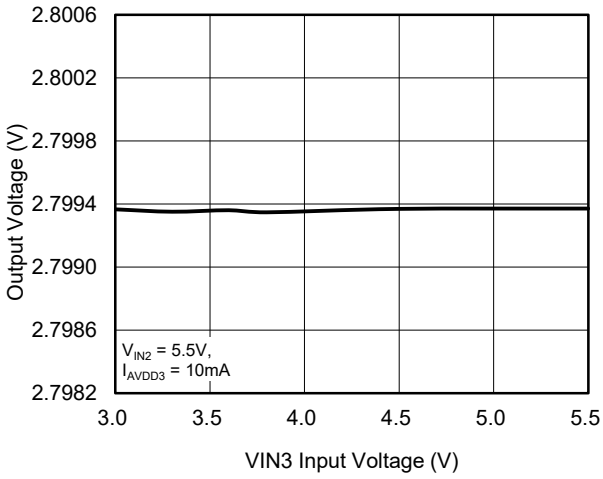
DVDD Output Voltage vs. VIN1 Input Voltage



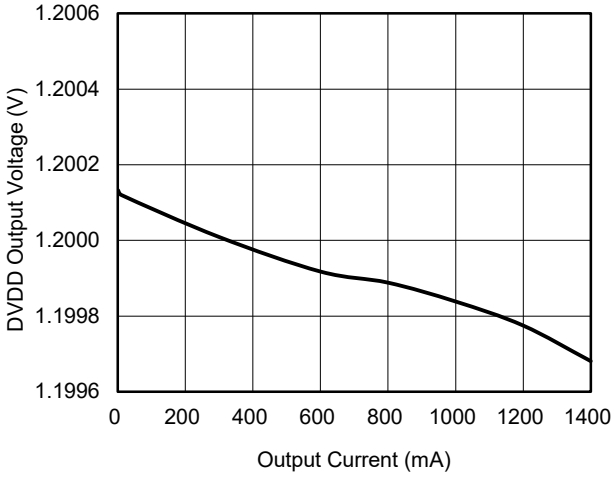
AVDD1/2/3 Output Voltage vs. VIN2 Input Voltage



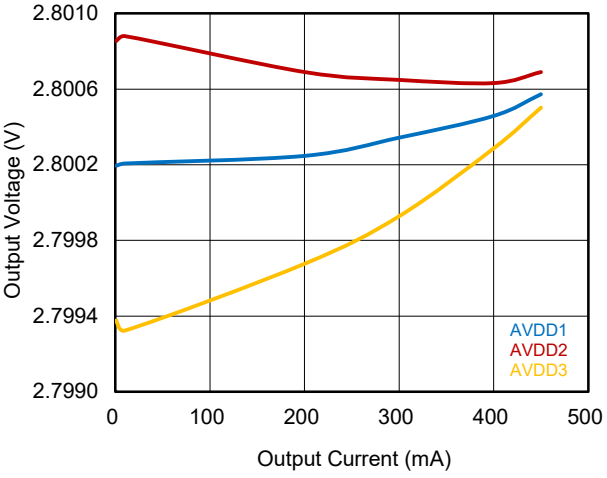
AVDD3 Output Voltage vs. VIN3 Input Voltage



DVDD Output Voltage vs. Output Current



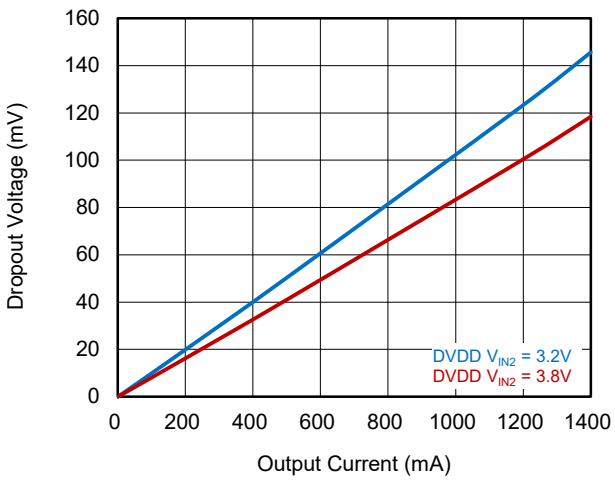
AVDD1/2/3 Output Voltage vs. Output Current



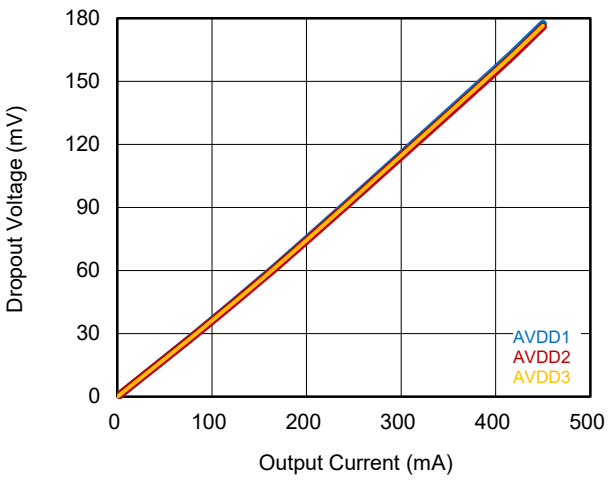
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = V_{IN3} = 3.8V, V_{DVDD} = 1.2V, $V_{AVDD1/2/3}$ = 2.8V, $C_{IN1/2/3}$ = 1μF, C_{DVDD} = 4.7μF and $C_{AVDD1/2/3}$ = 2.2μF, unless otherwise noted.

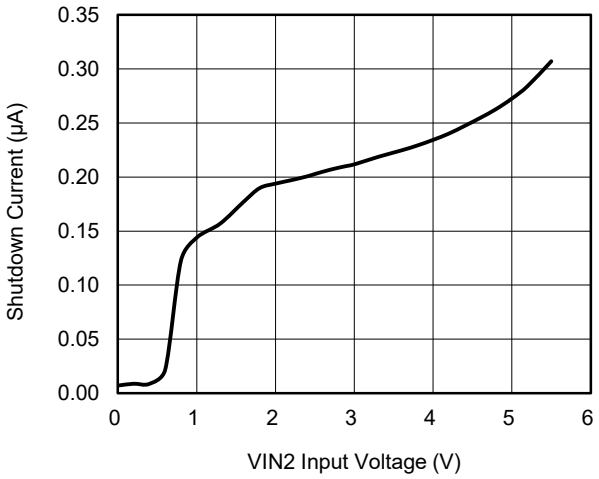
Dropout Voltage vs. Output Current



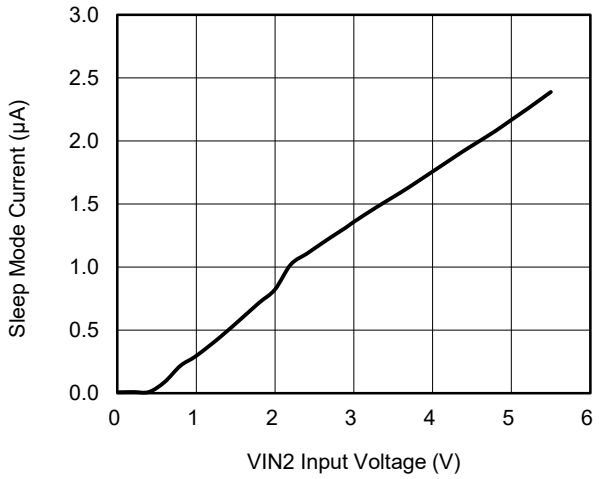
Dropout Voltage vs. Output Current



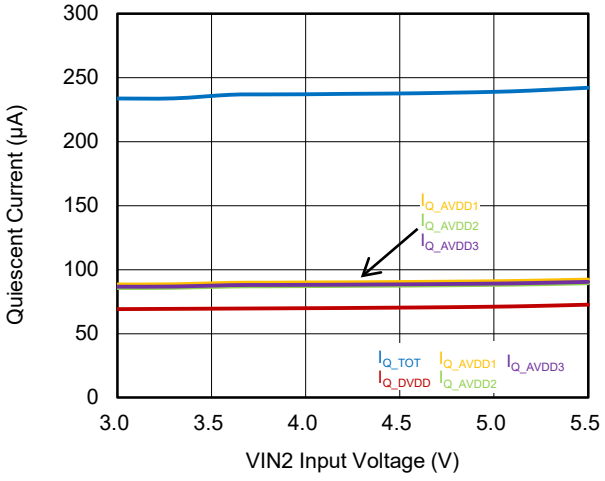
Shutdown Current vs. VIN2 Input Voltage



Sleep Mode Current vs. VIN2 Input Voltage



Quiescent Current vs. VIN2 Input Voltage



DETAILED DESCRIPTION

Output Startup and Shutdown Behavior

The SGM38122 has four LDO regulators. Since the hardware EN pin has high priority to shut down the chip, it should set high before the I^2C communication and register configuration on each outputs. Next is to set the EN_REF bit to high, which enables the internal reference voltage and the LDO regulators are ready for powering up.

The registers of DVDD_SEQ and AVDD1/2/3_SEQ are to determine the power on/off method of DVDD and AVDD1/2/3 respectively. If the relative LDO sequence number is configured to 0, this LDO can be controlled by its EN register for outputting and shutdown. For example, if DVDD_SEQ = 0, setting DVDD_EN bit to 1 can enable the output. While the relative LDO sequence number is configured to non-zero, its EN register function will be masked and the chip uses SEQ_CTRL[1:0] bits to trigger sequential on/off (see Figure 3).

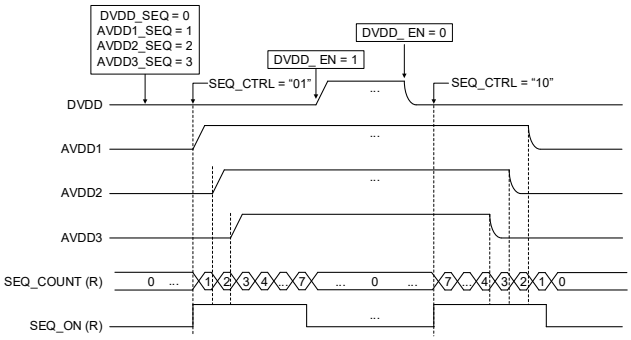


Figure 3. Power-Up and Shutdown by SEQ_CTRL or DVDD_EN Bit

It is required to set the voltage level of each channel through output voltage level definition registers before outputting.

For shutdown behavior, there are three methods.
1. Pull the hardware EN pin to low.
2. If enabled by its EN register, set EN bit to 0.
3. If enabled by SEQ_CTRL[1:0] bits, set SEQ_CTRL[1:0] = 0b10 to trigger shutdown sequence.

Sequence On/Off Control

Once the sequence startup function is activated by SEQ_CTRL[1:0] by writing to 2-bit code, 0b01, SEQ_COUNT[2:0] begins to increment immediately. When the LDO encounters its time slot equal to the SEQ_COUNT[2:0], the LDO will be activated. The period of the time slot can be configured by SEQ_SPEED[1:0], and SEQ_ON bit indicates the counting status of the time slot. After SEQ_COUNT counts to seven and last for one SEQ_SPEED[1:0] time, SEQ_COUNT[2:0] will be reset to 0. This reset behavior helps to reconfigure other unactivated LDOs to start using the sequence enable function again through SEQ_CTRL (see Figure 4).

The shutdown behavior of the sequence is initiated by writing SEQ_CTRL[1:0] to 2-bit code, 0b10, causing SEQ_COUNT[2:0] to immediately change from 0 to 7, and then count down to zero at periods configured by SEQ_SPEED[1:0]. When the LDO encounters its time slot equal to the SEQ_COUNT[2:0], the LDO will be turned off (see Figure 4).

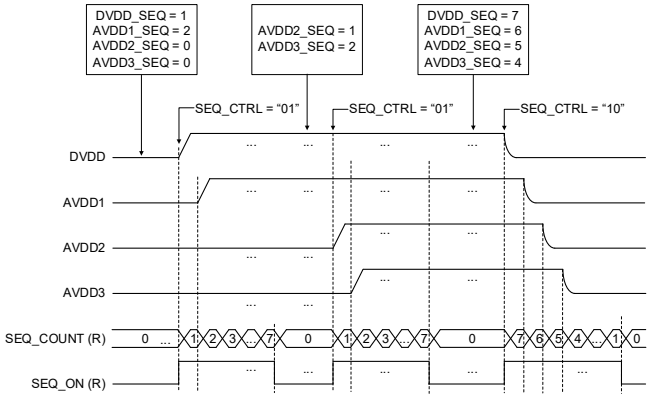


Figure 4. Power-Up and Shutdown by SEQ_CTRL

Over-Temperature Protection

The SGM38122 has over-temperature protection to prevent the chip from overheating. If the die temperature is greater than +140℃, all the enabled LDO outputs will shut down immediately. The outputs can re-start up when the die temperature is lower than +125℃.

Besides, the output voltages and enable functions, especially for those related to the sequential power-on configuration will be kept and used in the recovery.

Input Under-Voltage Lockout Protection

The SGM38122 includes input under-voltage lockout protection for $V_{IN1/2/3}$. If V_{IN2} as the system voltage is lower than the falling threshold, $V_{UVLO\_FL\_IN2}$, the chip will shut down and all registers will be reset. For $V_{IN1/3}$ UVLO events, the corresponding outputs will shut down when UVLO happening and recover when UVLO disappeared.

DETAILED DESCRIPTION (continued)

Output Over-Current Protection

The LDOs are protected from excessive load and short-circuit. When an overload event occurs, the output current is automatically limited to the current limit or the foldback current. The foldback current is two-thirds of the DVDD's current limit and half of the AVDD1/2/3's, respectively. And the trigger condition is 57% of DVDD_VOUT and 40% of AVDD1/2/3_VOUT. The foldback current will return to normal current limit when the output voltage is higher than 71% of DVDD_VOUT and 60% of AVDD1/2/3_VOUT. After a fixed 1ms OCP deglitch timer, the chip will take actions to the OCP fault.

FLT_SD_B bit selects the OCP protection behavior (see Figure 5).

1. FLT_SD_B = 0 (default): the over-current output makes 4 times hiccup and then permanently shut down.

2. FLT_SD_B = 1: the over-current output keeps outputting. The output voltage is proportional to the output impedance.

Output Discharge Setting

The output discharge resistor for each channel is 250Ω and is always on by default. It can be adjusted to 125Ω for quick discharging by setting DVDD_DISCH_SET and AVDD1/2/3_DISCH_SET bits. And the discharge function can be disabled by register DVDD_DISCH_EN and AVDD1/2/3_DISCH_EN.

When $V_{IN1/2/3} \geq V_{UVLO\_FL\_IN1/2/3}$, the output discharge can be used in the LDO disable cases and the fault shutdown cases, including output over-current and over-temperature.

Programmable I²C Address Selection

The SGM38122 operates as a slave device that address is 7'h29 by default. In the I²C_ADDR register, there are other three select-able device address for I²C communication. In the two or more SGM38122 application (see Figure 6), those applications that need to adjust the address of I²C should first pull up the EN pin for address setting.

The programmed device address will be reset by soft reset function, EN pin reset and VIN2 input voltage under $V_{UVLO\_FL\_IN2}$

Layout Guidelines

Layout design is an important step in all PMIC design. Good layout plays a positive role in loop stability, signal integrity and low EMI. Key guidelines to follow for the layout are:

VIN1, VIN2, VIN3, DVDD and AVDD1/2/3 traces must be as wide as possible to reduce trace impedance and improve heat dissipation. To get high transient response performance and low output noise, the input and output bypass capacitors must be placed as close as possible to the device on the same side of the PCB. Additionally, to maintain the effective PSRR performance not to degrade by the EMI, the source trace needs to be directly above/below the return ground path, which helps to cancel each other electromagnetic field out.

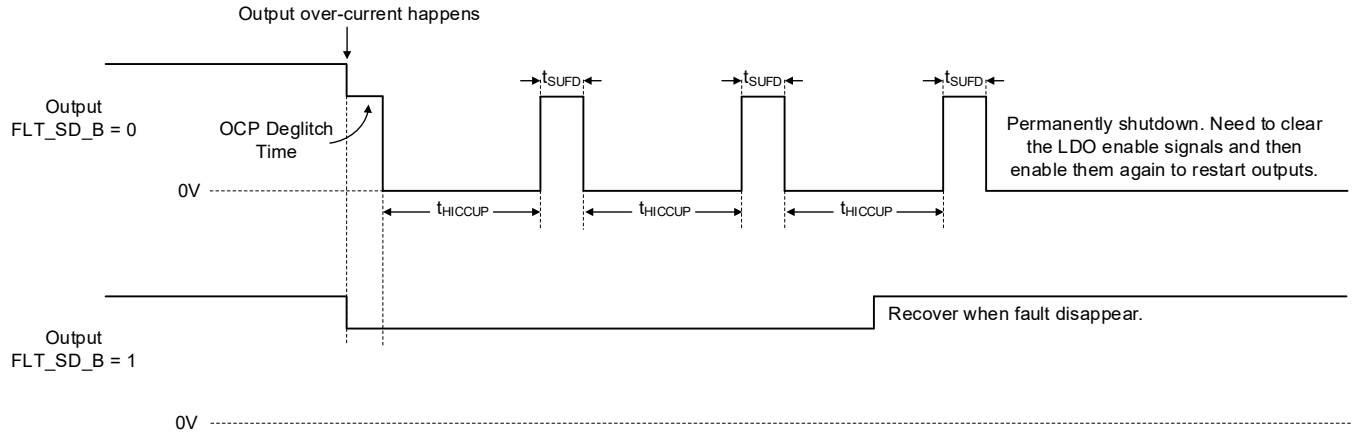


Figure 5. Over-Current Protection Behavior

DETAILED DESCRIPTION (continued)

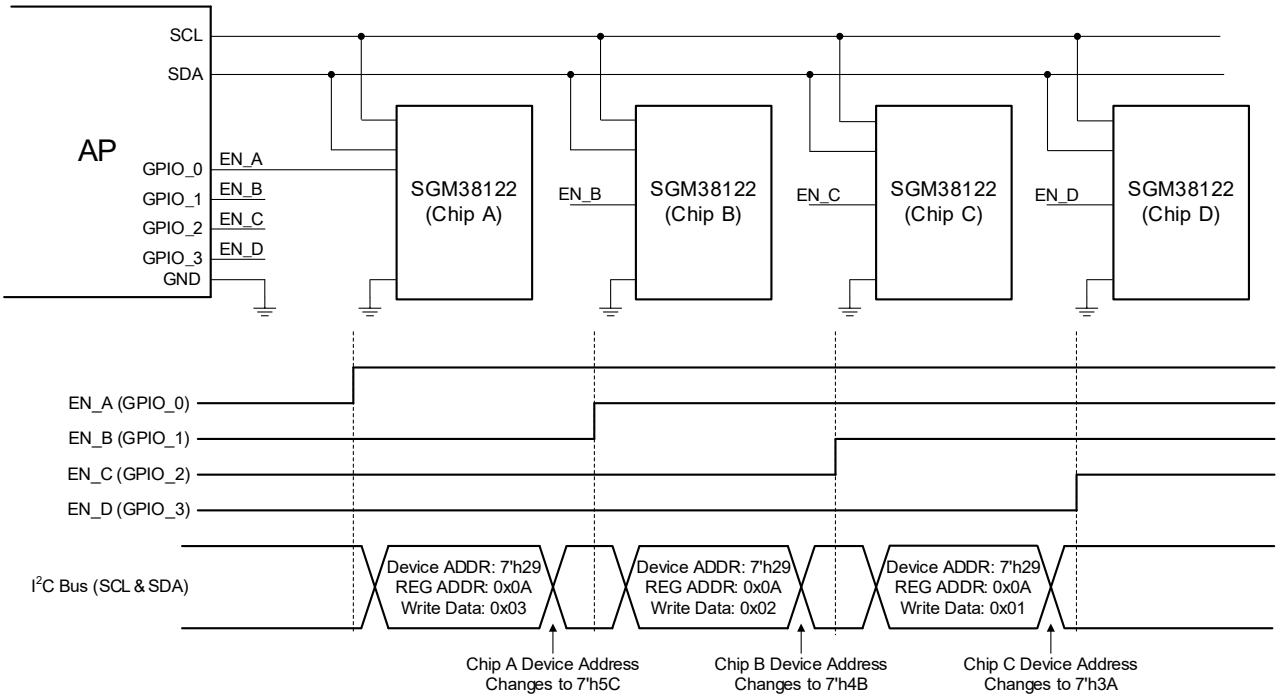


Figure 6. I²C Address Configuration in Four SGM38122 Application

REGISTER MAPS

FUNCTION	STAT	FLAG	MASK	ENABLE	SET
CHIP_REV	0x00[7:0]				
EN_REF				0x01[7]	
DVDD_EN	0x0C[0]			0x01[0]	
DVDD_DISCH_EN				0x05[0]	
DVDD_DISCH_SET					0x05[4]
DVDD_VOUT	0x06[7:0]				
AVDD1_EN	0x0C[1]			0x01[1]	
AVDD1_DISCH_EN				0x05[1]	
AVDD1_DISCH_SET					0x05[5]
AVDD1_VOUT	0x07[7:0]				
AVDD2_EN	0x0C[2]			0x01[2]	
AVDD2_DISCH_EN				0x05[2]	
AVDD2_DISCH_SET					0x05[6]
AVDD2_VOUT	0x08[7:0]				
AVDD3_EN	0x0C[3]			0x01[3]	
AVDD3_DISCH_EN				0x05[3]	
AVDD3_DISCH_SET					0x05[7]
AVDD3_VOUT	0x09[7:0]				
nINT_SETTING	0x0A[3:2]				
I^2C_ADDR	0x0A[1:0]				
TSD	0x0D[7]	0x0B[7]	0x0E[7]		
DVDD_OCP	0x0D[0]	0x0B[0]	0x0E[0]		
AVDD1_OCP	0x0D[1]	0x0B[1]	0x0E[1]		
AVDD2_OCP	0x0D[2]	0x0B[2]	0x0E[2]		
AVDD3_OCP	0x0D[3]	0x0B[3]	0x0E[3]		
DVDD_SEQ	0x02[2:0]	0x04[3]			
AVDD1_SEQ	0x02[6:4]	0x04[3]			
AVDD2_SEQ	0x03[2:0]	0x04[3]			
AVDD3_SEQ	0x03[6:4]	0x04[3]			
SEQ_CTRL	0x04[5:4]				
SEQ_SPEED	0x04[7:6]				
SEQ_COUNT	0x04[2:0]				

REGISTER MAPS (continued)

I²C Slave Address of SGM38122: 7'h29

Bit Types:

R: Read only

R/W: Read/Write

REG0x00: Chip Revision Register [Reset = 0x26]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	CHIP_REV[7:0]	00100110	R	Indicates the device ID with revision.	N/A

REG0x01: Enable Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_REF	0	R/W	Enable bit for system bias. 0 = Disabled (default) 1 = Enabled	SOFT_RESET
D[6:4]	Reserved	000	R	Reserved	N/A
D[3]	AVDD3_EN	0	R/W	Chip Enable Control Register. This register can be written to enable or disable the corresponding LDO regulator. Bit0 for DVDD_EN Bit1 for AVDD1_EN Bit2 for AVDD2_EN Bit3 for AVDD3_EN 0 = Disable (default) 1 = Enable	SOFT_RESET
D[2]	AVDD2_EN	0	R/W		
D[1]	AVDD1_EN	0	R/W		
D[0]	DVDD_EN	0	R/W		

REG0x02: AVDD1 and DVDD Sequence Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:4]	AVDD1_SEQ[2:0]	000	R/W	The AVDD1 power up and down sequence by using SEQ_CTRL register. 000 = Controlled by the AVDD1_EN bit. (default) 001 = Set the AVDD1 power up and down sequence to slot1. 010 = Set the AVDD1 power up and down sequence to slot2. 011 = Set the AVDD1 power up and down sequence to slot3. 100 = Set the AVDD1 power up and down sequence to slot4. 101 = Set the AVDD1 power up and down sequence to slot5. 110 = Set the AVDD1 power up and down sequence to slot6. 111 = Set the AVDD1 power up and down sequence to slot7.	SOFT_RESET
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	DVDD_SEQ[2:0]	000	R/W	The DVDD power up and down sequence by using SEQ_CTRL register. 000 = Controlled by the DVDD_EN bit. (default) 001 = Set the DVDD power up and down sequence to slot1. 010 = Set the DVDD power up and down sequence to slot2. 011 = Set the DVDD power up and down sequence to slot3. 100 = Set the DVDD power up and down sequence to slot4. 101 = Set the DVDD power up and down sequence to slot5. 110 = Set the DVDD power up and down sequence to slot6. 111 = Set the DVDD power up and down sequence to slot7.	SOFT_RESET

REGISTER MAPS (continued)

REG0x03: AVDD3 and AVDD2 Sequence Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:4]	AVDD3_SEQ[2:0]	000	R/W	The AVDD3 power up and down sequence by using SEQ_CTRL register. 000 = Controlled by the AVDD3_EN bit. (default) 001 = Set the AVDD3 power up and down sequence to slot1. 010 = Set the AVDD3 power up and down sequence to slot2. 011 = Set the AVDD3 power up and down sequence to slot3. 100 = Set the AVDD3 power up and down sequence to slot4. 101 = Set the AVDD3 power up and down sequence to slot5. 110 = Set the AVDD3 power up and down sequence to slot6. 111 = Set the AVDD3 power up and down sequence to slot7.	SOFT_RESET
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	AVDD2_SEQ[2:0]	000	R/W	The AVDD2 power up and down sequence by using SEQ_CTRL register. 000 = Controlled by the AVDD2_EN bit. (default) 001 = Set the AVDD2 power up and down sequence to slot1. 010 = Set the AVDD2 power up and down sequence to slot2. 011 = Set the AVDD2 power up and down sequence to slot3. 100 = Set the AVDD2 power up and down sequence to slot4. 101 = Set the AVDD2 power up and down sequence to slot5. 110 = Set the AVDD2 power up and down sequence to slot6. 111 = Set the AVDD2 power up and down sequence to slot7.	SOFT_RESET

REG0x04: Sequence Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	SEQ_SPEED[1:0]	00	R/W	Define the slot period as following: 00 = 2.0ms (default) 01 = 1.0ms 10 = 0.5ms 11 = 0.25ms	SOFT_RESET
D[5:4]	SEQ_CTRL[1:0]	00	WCLR	Enables power-up or shutdown of SEQ. Write and clear: 00 = Default 01 = Power-up 10 = Shutdown 11 = Ignored	SOFT_RESET, SEQ_CTRL
D[3]	SEQ_ON	0	R	Indicates the activation signal of SEQ. Read only: 0 = Sequencing process off (default). Indicates the sequence is not in process. 1 = Sequencing process on. Indicates the sequence is executing and somewhere between the start of slot1 and the end of slot 7.	N/A
D[2:0]	SEQ_COUNT[2:0]	000	R	Indicates the slot number of SEQ at the moment. Read only: 000 = Indicates sequence has completed or not started. (default) 001 = Indicates in slot1 during register read. 010 = Indicates in slot2 during register read. 011 = Indicates in slot3 during register read. 100 = Indicates in slot4 during register read. 101 = Indicates in slot5 during register read. 110 = Indicates in slot6 during register read. 111 = Indicates in slot7 during register read.	N/A

REGISTER MAPS (continued)

REG0x05: Discharge Resistor Selection Register [Reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	AVDD3_DISCH_SET	0	R/W	AVDD3 Discharge Resistor Setting 0 = 250Ω (default) 1 = 125Ω	SOFT_RESET
D[6]	AVDD2_DISCH_SET	0	R/W	AVDD2 Discharge Resistor Setting 0 = 250Ω (default) 1 = 125Ω	SOFT_RESET
D[5]	AVDD1_DISCH_SET	0	R/W	AVDD1 Discharge Resistor Setting 0 = 250Ω (default) 1 = 125Ω	SOFT_RESET
D[4]	DVDD_DISCH_SET	0	R/W	DVDD Discharge Resistor Setting 0 = 250Ω (default) 1 = 125Ω	SOFT_RESET
D[3]	AVDD3_DISCH_EN	1	R/W	AVDD3 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)	SOFT_RESET
D[2]	AVDD2_DISCH_EN	1	R/W	AVDD2 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)	SOFT_RESET
D[1]	AVDD1_DISCH_EN	1	R/W	AVDD1 Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)	SOFT_RESET
D[0]	DVDD_DISCH_EN	1	R/W	DVDD Discharge Resistor Enable/Disable Control 0 = Disable 1 = Enable (default)	SOFT_RESET

REGISTER MAPS (continued)

REG0x06: DVDD Output Voltage Register [Reset = 0x57]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							RESET BY
D[7:0]	DVDD_VOUT[7:0]	01010111	R/W	Sets DVDD regulation target voltage. Equation: V_{DVDD} = (504 + 8 × *dec*) × 1mV, where *dec* is the decimal value of the register.							SOFT_RESET
				Hex	V_{DVDD}	Hex	V_{DVDD}	Hex	V_{DVDD}	Hex	V_{DVDD}
				00	Reserved	40	1.016V	80	1.528V	C0	Reserved
				01	Reserved	41	1.024V	81	1.536V	C1	Reserved
				02	Reserved	42	1.032V	82	1.544V	C2	Reserved
				03	0.528V	43	1.040V	83	1.552V	C3	Reserved
				04	0.536V	44	1.048V	84	1.560V	C4	Reserved
				05	0.544V	45	1.056V	85	1.568V	C5	Reserved
				06	0.552V	46	1.064V	86	1.576V	C6	Reserved
				07	0.560V	47	1.072V	87	1.584V	C7	Reserved
				08	0.568V	48	1.080V	88	1.592V	C8	Reserved
				09	0.576V	49	1.088V	89	1.600V	C9	Reserved
				0A	0.584V	4A	1.096V	8A	1.608V	CA	Reserved
				0B	0.592V	4B	1.104V	8B	1.616V	CB	Reserved
				0C	0.600V	4C	1.112V	8C	1.624V	CC	Reserved
				0D	0.608V	4D	1.120V	8D	1.632V	CD	Reserved
				0E	0.616V	4E	1.128V	8E	1.640V	CE	Reserved
				0F	0.624V	4F	1.136V	8F	1.648V	CF	Reserved
				10	0.632V	50	1.144V	90	1.656V	D0	Reserved
				11	0.640V	51	1.152V	91	1.664V	D1	Reserved
				12	0.648V	52	1.160V	92	1.672V	D2	Reserved
				13	0.656V	53	1.168V	93	1.680V	D3	Reserved
				14	0.664V	54	1.176V	94	1.688V	D4	Reserved
				15	0.672V	55	1.184V	95	1.696V	D5	Reserved
				16	0.680V	56	1.192V	96	1.704V	D6	Reserved
				17	0.688V	**57**	**1.200V**	97	1.712V	D7	Reserved
				18	0.696V	58	1.208V	98	1.720V	D8	Reserved
				19	0.704V	59	1.216V	99	1.728V	D9	Reserved
				1A	0.712V	5A	1.224V	9A	1.736V	DA	Reserved
				1B	0.720V	5B	1.232V	9B	1.744V	DB	Reserved
				1C	0.728V	5C	1.240V	9C	1.752V	DC	Reserved
				1D	0.736V	5D	1.248V	9D	1.760V	DD	Reserved
				1E	0.744V	5E	1.256V	9E	1.768V	DE	Reserved
				1F	0.752V	5F	1.264V	9F	1.776V	DF	Reserved
				20	0.760V	60	1.272V	A0	1.784V	E0	Reserved
				21	0.768V	61	1.280V	A1	1.792V	E1	Reserved
				22	0.776V	62	1.288V	A2	1.800V	E2	Reserved
				23	0.784V	63	1.296V	A3	Reserved	E3	Reserved
				24	0.792V	64	1.304V	A4	Reserved	E4	Reserved
				25	0.800V	65	1.312V	A5	Reserved	E5	Reserved
				26	0.808V	66	1.320V	A6	Reserved	E6	Reserved

REGISTER MAPS (continued)

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{DVDD}	Hex	V_{DVDD}	Hex	V_{DVDD}	Hex	V_{DVDD}
D[7:0]	DVDD_VOUT[7:0]	01010111	R/W	27	0.816V	67	1.328V	A7	Reserved	E7	Reserved
				28	0.824V	68	1.336V	A8	Reserved	E8	Reserved
				29	0.832V	69	1.344V	A9	Reserved	E9	Reserved
				2A	0.840V	6A	1.352V	AA	Reserved	EA	Reserved
				2B	0.848V	6B	1.360V	AB	Reserved	EB	Reserved
				2C	0.856V	6C	1.368V	AC	Reserved	EC	Reserved
				2D	0.864V	6D	1.376V	AD	Reserved	ED	Reserved
				2E	0.872V	6E	1.384V	AE	Reserved	EE	Reserved
				2F	0.880V	6F	1.392V	AF	Reserved	EF	Reserved
				30	0.888V	70	1.400V	B0	Reserved	F0	Reserved
				31	0.896V	71	1.408V	B1	Reserved	F1	Reserved
				32	0.904V	72	1.416V	B2	Reserved	F2	Reserved
				33	0.912V	73	1.424V	B3	Reserved	F3	Reserved
				34	0.920V	74	1.432V	B4	Reserved	F4	Reserved
				35	0.928V	75	1.440V	B5	Reserved	F5	Reserved
				36	0.936V	76	1.448V	B6	Reserved	F6	Reserved
				37	0.944V	77	1.456V	B7	Reserved	F7	Reserved
				38	0.952V	78	1.464V	B8	Reserved	F8	Reserved
				39	0.960V	79	1.472V	B9	Reserved	F9	Reserved
				3A	0.968V	7A	1.480V	BA	Reserved	FA	Reserved
				3B	0.976V	7B	1.488V	BB	Reserved	FB	Reserved
				3C	0.984V	7C	1.496V	BC	Reserved	FC	Reserved
				3D	0.992V	7D	1.504V	BD	Reserved	FD	Reserved
				3E	1.000V	7E	1.512V	BE	Reserved	FE	Reserved
				3F	1.008V	7F	1.520V	BF	Reserved	FF	Reserved

REGISTER MAPS (continued)

REG0x07: AVDD1 Output Voltage Register [Reset = 0xB1]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							RESET BY
D[7:0]	AVDD1_VOUT[7:0]	10110001	R/W	Sets AVDD1 regulation target voltage. Equation: V_{AVDD1} = (1384 + 8 × *dec*) × 1mV, where *dec* is the decimal value of the register.							SOFT_RESET
				Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}
				00	Reserved	40	1.896V	80	2.408V	C0	2.920V
				01	Reserved	41	1.904V	81	2.416V	C1	2.928V
				02	Reserved	42	1.912V	82	2.424V	C2	2.936V
				03	Reserved	43	1.920V	83	2.432V	C3	2.944V
				04	Reserved	44	1.928V	84	2.440V	C4	2.952V
				05	Reserved	45	1.936V	85	2.448V	C5	2.960V
				06	Reserved	46	1.944V	86	2.456V	C6	2.968V
				07	Reserved	47	1.952V	87	2.464V	C7	2.976V
				08	Reserved	48	1.960V	88	2.472V	C8	2.984V
				09	Reserved	49	1.968V	89	2.480V	C9	2.992V
				0A	Reserved	4A	1.976V	8A	2.488V	CA	3.000V
				0B	Reserved	4B	1.984V	8B	2.496V	CB	3.008V
				0C	Reserved	4C	1.992V	8C	2.504V	CC	3.016V
				0D	Reserved	4D	2.000V	8D	2.512V	CD	3.024V
				0E	Reserved	4E	2.008V	8E	2.520V	CE	3.032V
				0F	1.504V	4F	2.016V	8F	2.528V	CF	3.040V
				10	1.512V	50	2.024V	90	2.536V	D0	3.048V
				11	1.520V	51	2.032V	91	2.544V	D1	3.056V
				12	1.528V	52	2.040V	92	2.552V	D2	3.064V
				13	1.536V	53	2.048V	93	2.560V	D3	3.072V
				14	1.544V	54	2.056V	94	2.568V	D4	3.080V
				15	1.552V	55	2.064V	95	2.576V	D5	3.088V
				16	1.560V	56	2.072V	96	2.584V	D6	3.096V
				17	1.568V	57	2.080V	97	2.592V	D7	3.104V
				18	1.576V	58	2.088V	98	2.600V	D8	3.112V
				19	1.584V	59	2.096V	99	2.608V	D9	3.120V
				1A	1.592V	5A	2.104V	9A	2.616V	DA	3.128V
				1B	1.600V	5B	2.112V	9B	2.624V	DB	3.136V
				1C	1.608V	5C	2.120V	9C	2.632V	DC	3.144V
				1D	1.616V	5D	2.128V	9D	2.640V	DD	3.152V
				1E	1.624V	5E	2.136V	9E	2.648V	DE	3.160V
				1F	1.632V	5F	2.144V	9F	2.656V	DF	3.168V
				20	1.640V	60	2.152V	A0	2.664V	E0	3.176V
				21	1.648V	61	2.160V	A1	2.672V	E1	3.184V
				22	1.656V	62	2.168V	A2	2.680V	E2	3.192V
				23	1.664V	63	2.176V	A3	2.688V	E3	3.200V
				24	1.672V	64	2.184V	A4	2.696V	E4	3.208V
				25	1.680V	65	2.192V	A5	2.704V	E5	3.216V
				26	1.688V	66	2.200V	A6	2.712V	E6	3.224V

REGISTER MAPS (continued)

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}
				27	1.696V	67	2.208V	A7	2.720V	E7	3.232V
				28	1.704V	68	2.216V	A8	2.728V	E8	3.240V
				29	1.712V	69	2.224V	A9	2.736V	E9	3.248V
				2A	1.720V	6A	2.232V	AA	2.744V	EA	3.256V
				2B	1.728V	6B	2.240V	AB	2.752V	EB	3.264V
				2C	1.736V	6C	2.248V	AC	2.760V	EC	3.272V
				2D	1.744V	6D	2.256V	AD	2.768V	ED	3.280V
				2E	1.752V	6E	2.264V	AE	2.776V	EE	3.288V
				2F	1.760V	6F	2.272V	AF	2.784V	EF	3.296V
				30	1.768V	70	2.280V	B0	2.792V	F0	3.304V
				31	1.776V	71	2.288V	**B1**	**2.800V**	F1	3.312V
				32	1.784V	72	2.296V	B2	2.808V	F2	3.320V
				33	1.792V	73	2.304V	B3	2.816V	F3	3.328V
D[7:0]	AVDD1_VOUT[7:0]	10110001	R/W	34	1.800V	74	2.312V	B4	2.824V	F4	3.336V
				35	1.808V	75	2.320V	B5	2.832V	F5	3.344V
				36	1.816V	76	2.328V	B6	2.840V	F6	3.352V
				37	1.824V	77	2.336V	B7	2.848V	F7	3.360V
				38	1.832V	78	2.344V	B8	2.856V	F8	3.368V
				39	1.840V	79	2.352V	B9	2.864V	F9	3.376V
				3A	1.848V	7A	2.360V	BA	2.872V	FA	3.384V
				3B	1.856V	7B	2.368V	BB	2.880V	FB	3.392V
				3C	1.864V	7C	2.376V	BC	2.888V	FC	3.400V
				3D	1.872V	7D	2.384V	BD	2.896V	FD	3.408V
				3E	1.880V	7E	2.392V	BE	2.904V	FE	3.416V
				3F	1.888V	7F	2.400V	BF	2.912V	FF	3.424V

REGISTER MAPS (continued)

REG0x08: AVDD2 Output Voltage Register [Reset = 0xB1]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							RESET BY
D[7:0]	AVDD2_VOUT[7:0]	10110001	R/W	Sets AVDD2 regulation target voltage. Equation: V_{AVDD2} = (1384 + 8 × *dec*) × 1mV, where *dec* is the decimal value of the register.							SOFT_RESET
				Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}
				00	Reserved	40	1.896V	80	2.408V	C0	2.920V
				01	Reserved	41	1.904V	81	2.416V	C1	2.928V
				02	Reserved	42	1.912V	82	2.424V	C2	2.936V
				03	Reserved	43	1.920V	83	2.432V	C3	2.944V
				04	Reserved	44	1.928V	84	2.440V	C4	2.952V
				05	Reserved	45	1.936V	85	2.448V	C5	2.960V
				06	Reserved	46	1.944V	86	2.456V	C6	2.968V
				07	Reserved	47	1.952V	87	2.464V	C7	2.976V
				08	Reserved	48	1.960V	88	2.472V	C8	2.984V
				09	Reserved	49	1.968V	89	2.480V	C9	2.992V
				0A	Reserved	4A	1.976V	8A	2.488V	CA	3.000V
				0B	Reserved	4B	1.984V	8B	2.496V	CB	3.008V
				0C	Reserved	4C	1.992V	8C	2.504V	CC	3.016V
				0D	Reserved	4D	2.000V	8D	2.512V	CD	3.024V
				0E	Reserved	4E	2.008V	8E	2.520V	CE	3.032V
				0F	1.504V	4F	2.016V	8F	2.528V	CF	3.040V
				10	1.512V	50	2.024V	90	2.536V	D0	3.048V
				11	1.520V	51	2.032V	91	2.544V	D1	3.056V
				12	1.528V	52	2.040V	92	2.552V	D2	3.064V
				13	1.536V	53	2.048V	93	2.560V	D3	3.072V
				14	1.544V	54	2.056V	94	2.568V	D4	3.080V
				15	1.552V	55	2.064V	95	2.576V	D5	3.088V
				16	1.560V	56	2.072V	96	2.584V	D6	3.096V
				17	1.568V	57	2.080V	97	2.592V	D7	3.104V
				18	1.576V	58	2.088V	98	2.600V	D8	3.112V
				19	1.584V	59	2.096V	99	2.608V	D9	3.120V
				1A	1.592V	5A	2.104V	9A	2.616V	DA	3.128V
				1B	1.600V	5B	2.112V	9B	2.624V	DB	3.136V
				1C	1.608V	5C	2.120V	9C	2.632V	DC	3.144V
				1D	1.616V	5D	2.128V	9D	2.640V	DD	3.152V
				1E	1.624V	5E	2.136V	9E	2.648V	DE	3.160V
				1F	1.632V	5F	2.144V	9F	2.656V	DF	3.168V
				20	1.640V	60	2.152V	A0	2.664V	E0	3.176V
				21	1.648V	61	2.160V	A1	2.672V	E1	3.184V
				22	1.656V	62	2.168V	A2	2.680V	E2	3.192V
				23	1.664V	63	2.176V	A3	2.688V	E3	3.200V
				24	1.672V	64	2.184V	A4	2.696V	E4	3.208V
				25	1.680V	65	2.192V	A5	2.704V	E5	3.216V
				26	1.688V	66	2.200V	A6	2.712V	E6	3.224V

REGISTER MAPS (continued)

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}
				27	1.696V	67	2.208V	A7	2.720V	E7	3.232V
				28	1.704V	68	2.216V	A8	2.728V	E8	3.240V
				29	1.712V	69	2.224V	A9	2.736V	E9	3.248V
				2A	1.720V	6A	2.232V	AA	2.744V	EA	3.256V
				2B	1.728V	6B	2.240V	AB	2.752V	EB	3.264V
				2C	1.736V	6C	2.248V	AC	2.760V	EC	3.272V
				2D	1.744V	6D	2.256V	AD	2.768V	ED	3.280V
				2E	1.752V	6E	2.264V	AE	2.776V	EE	3.288V
				2F	1.760V	6F	2.272V	AF	2.784V	EF	3.296V
				30	1.768V	70	2.280V	B0	2.792V	F0	3.304V
				31	1.776V	71	2.288V	**B1**	**2.800V**	F1	3.312V
				32	1.784V	72	2.296V	B2	2.808V	F2	3.320V
				33	1.792V	73	2.304V	B3	2.816V	F3	3.328V
D[7:0]	AVDD2_VOUT[7:0]	10110001	R/W	34	1.800V	74	2.312V	B4	2.824V	F4	3.336V
				35	1.808V	75	2.320V	B5	2.832V	F5	3.344V
				36	1.816V	76	2.328V	B6	2.840V	F6	3.352V
				37	1.824V	77	2.336V	B7	2.848V	F7	3.360V
				38	1.832V	78	2.344V	B8	2.856V	F8	3.368V
				39	1.840V	79	2.352V	B9	2.864V	F9	3.376V
				3A	1.848V	7A	2.360V	BA	2.872V	FA	3.384V
				3B	1.856V	7B	2.368V	BB	2.880V	FB	3.392V
				3C	1.864V	7C	2.376V	BC	2.888V	FC	3.400V
				3D	1.872V	7D	2.384V	BD	2.896V	FD	3.408V
				3E	1.880V	7E	2.392V	BE	2.904V	FE	3.416V
				3F	1.888V	7F	2.400V	BF	2.912V	FF	3.424V

REGISTER MAPS (continued)

REG0x09: AVDD3 Output Voltage Register [Reset = 0xB1]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION								RESET BY
D[7:0]	AVDD3_VOUT[7:0]	10110001	R/W	Sets AVDD3 regulation target voltage. Equation: V_{AVDD3} = (1384 + 8 × *dec*) × 1mV, where *dec* is the decimal value of the register.								SOFT_RESET
				Hex	V_{AVDD3}	Hex	V_{AVDD3}	Hex	V_{AVDD3}	Hex	V_{AVDD3}	
				00	Reserved	40	1.896V	80	2.408V	C0	2.920V	
				01	Reserved	41	1.904V	81	2.416V	C1	2.928V	
				02	Reserved	42	1.912V	82	2.424V	C2	2.936V	
				03	Reserved	43	1.920V	83	2.432V	C3	2.944V	
				04	Reserved	44	1.928V	84	2.440V	C4	2.952V	
				05	Reserved	45	1.936V	85	2.448V	C5	2.960V	
				06	Reserved	46	1.944V	86	2.456V	C6	2.968V	
				07	Reserved	47	1.952V	87	2.464V	C7	2.976V	
				08	Reserved	48	1.960V	88	2.472V	C8	2.984V	
				09	Reserved	49	1.968V	89	2.480V	C9	2.992V	
				0A	Reserved	4A	1.976V	8A	2.488V	CA	3.000V	
				0B	Reserved	4B	1.984V	8B	2.496V	CB	3.008V	
				0C	Reserved	4C	1.992V	8C	2.504V	CC	3.016V	
				0D	Reserved	4D	2.000V	8D	2.512V	CD	3.024V	
				0E	Reserved	4E	2.008V	8E	2.520V	CE	3.032V	
				0F	1.504V	4F	2.016V	8F	2.528V	CF	3.040V	
				10	1.512V	50	2.024V	90	2.536V	D0	3.048V	
				11	1.520V	51	2.032V	91	2.544V	D1	3.056V	
				12	1.528V	52	2.040V	92	2.552V	D2	3.064V	
				13	1.536V	53	2.048V	93	2.560V	D3	3.072V	
				14	1.544V	54	2.056V	94	2.568V	D4	3.080V	
				15	1.552V	55	2.064V	95	2.576V	D5	3.088V	
				16	1.560V	56	2.072V	96	2.584V	D6	3.096V	
				17	1.568V	57	2.080V	97	2.592V	D7	3.104V	
				18	1.576V	58	2.088V	98	2.600V	D8	3.112V	
				19	1.584V	59	2.096V	99	2.608V	D9	3.120V	
				1A	1.592V	5A	2.104V	9A	2.616V	DA	3.128V	
				1B	1.600V	5B	2.112V	9B	2.624V	DB	3.136V	
				1C	1.608V	5C	2.120V	9C	2.632V	DC	3.144V	
				1D	1.616V	5D	2.128V	9D	2.640V	DD	3.152V	
				1E	1.624V	5E	2.136V	9E	2.648V	DE	3.160V	
				1F	1.632V	5F	2.144V	9F	2.656V	DF	3.168V	
				20	1.640V	60	2.152V	A0	2.664V	E0	3.176V	
				21	1.648V	61	2.160V	A1	2.672V	E1	3.184V	
				22	1.656V	62	2.168V	A2	2.680V	E2	3.192V	
				23	1.664V	63	2.176V	A3	2.688V	E3	3.200V	
				24	1.672V	64	2.184V	A4	2.696V	E4	3.208V	
				25	1.680V	65	2.192V	A5	2.704V	E5	3.216V	
				26	1.688V	66	2.200V	A6	2.712V	E6	3.224V	

REGISTER MAPS (continued)

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{AVDD3}	Hex	V_{AVDD3}	Hex	V_{AVDD3}	Hex	V_{AVDD3}
				27	1.696V	67	2.208V	A7	2.720V	E7	3.232V
				28	1.704V	68	2.216V	A8	2.728V	E8	3.240V
				29	1.712V	69	2.224V	A9	2.736V	E9	3.248V
				2A	1.720V	6A	2.232V	AA	2.744V	EA	3.256V
				2B	1.728V	6B	2.240V	AB	2.752V	EB	3.264V
				2C	1.736V	6C	2.248V	AC	2.760V	EC	3.272V
				2D	1.744V	6D	2.256V	AD	2.768V	ED	3.280V
				2E	1.752V	6E	2.264V	AE	2.776V	EE	3.288V
				2F	1.760V	6F	2.272V	AF	2.784V	EF	3.296V
				30	1.768V	70	2.280V	B0	2.792V	F0	3.304V
				31	1.776V	71	2.288V	**B1**	**2.800V**	F1	3.312V
				32	1.784V	72	2.296V	B2	2.808V	F2	3.320V
				33	1.792V	73	2.304V	B3	2.816V	F3	3.328V
D[7:0]	AVDD3_VOUT[7:0]	10110001	R/W	34	1.800V	74	2.312V	B4	2.824V	F4	3.336V
				35	1.808V	75	2.320V	B5	2.832V	F5	3.344V
				36	1.816V	76	2.328V	B6	2.840V	F6	3.352V
				37	1.824V	77	2.336V	B7	2.848V	F7	3.360V
				38	1.832V	78	2.344V	B8	2.856V	F8	3.368V
				39	1.840V	79	2.352V	B9	2.864V	F9	3.376V
				3A	1.848V	7A	2.360V	BA	2.872V	FA	3.384V
				3B	1.856V	7B	2.368V	BB	2.880V	FB	3.392V
				3C	1.864V	7C	2.376V	BC	2.888V	FC	3.400V
				3D	1.872V	7D	2.384V	BD	2.896V	FD	3.408V
				3E	1.880V	7E	2.392V	BE	2.904V	FE	3.416V
				3F	1.888V	7F	2.400V	BF	2.912V	FF	3.424V

REGISTER MAPS (continued)

REG0x0A: System Settings Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	SOFT_RESET[2:0]	000	WCLR	Writing a “101” begins a soft reset of the device I²C registers to their default values. These bits are cleared upon the execution of the reset function. Any other value than “101” will be ignored.	SOFT_RESET
D[4]	FLT_SD_B	0	R/W	0 = if OCP occurs, LDO will shut down and run in the hiccup mode (default) 1 = if OCP occurs, LDO will not shut down and run in the constant current mode	SOFT_RESET
D[3]	nINT_LEVEL	0	R/W	nINT Push-Pull Output Voltage Level, only for D[2] = 1’b1. 0 = 1.2V (default) 1 = 1.8V	SOFT_RESET
D[2]	nINT_MODE	0	R/W	nINT Mode Selection 0 = Open-Drain on nINT pin (default) 1 = Push-Pull on nINT pin	SOFT_RESET
D[1:0]	I2C_ADDR[1:0]	00	R/W	I²C Address Settings 00 = 7'h29 (default) 01 = 7'h3A 10 = 7'h4B 11 = 7'h5C	SOFT_RESET

REG0x0B: Interrupt Flag Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSD_INT	0	RCLR	Thermal Shutdown Interrupt 0 = Clear (default) 1 = A thermal shutdown event detected or that the temperature has fallen below the hysteresis level.	SOFT_RESET, Read REG0x0B
D[6:4]	Reserved	000	R	Reserved	N/A
D[3]	AVDD3_OCP_INT	0	RCLR	AVDD3 OCP Interrupt 0 = Clear (default) 1 = Over-current event detected on AVDD3 output.	SOFT_RESET, Read REG0x0B
D[2]	AVDD2_OCP_INT	0	RCLR	AVDD2 OCP Interrupt 0 = Clear (default) 1 = Over-current event detected on AVDD2 output.	SOFT_RESET, Read REG0x0B
D[1]	AVDD1_OCP_INT	0	RCLR	AVDD1 OCP Interrupt 0 = Clear (default) 1 = Over-current event detected on AVDD1 output.	SOFT_RESET, Read REG0x0B
D[0]	DVDD_OCP_INT	0	RCLR	DVDD OCP Interrupt 0 = Clear (default) 1 = Over-current event detected on DVDD output.	SOFT_RESET, Read REG0x0B

REG0x0C: LDO Suspended Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	AVDD3_SUSD	0	R	AVDD3 Output Suspended 0 = AVDD3 in normal state (default) 1 = AVDD3 has been suspended due to a fault condition.	N/A
D[2]	AVDD2_SUSD	0	R	AVDD2 Output Suspended 0 = AVDD2 in normal state (default) 1 = AVDD2 has been suspended due to a fault condition.	N/A
D[1]	AVDD1_SUSD	0	R	AVDD1 Output Suspended 0 = AVDD1 in normal state (default) 1 = AVDD1 has been suspended due to a fault condition.	N/A
D[0]	DVDD_SUSD	0	R	DVDD Output Suspended 0 = DVDD in normal state (default) 1 = DVDD has been suspended due to a fault condition.	N/A

REGISTER MAPS (continued)

REG0x0D: Fault Status Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSD_STAT	0	R	Thermal Shutdown Status 0 = Normal Operation (default) 1 = Device is in thermal shutdown.	N/A
D[6:4]	Reserved	000	R	Reserved	N/A
D[3]	AVDD3_OCP_STAT	0	R	AVDD3 OCP Status 0 = Normal Operation (default) 1 = An over-current condition exists on AVDD3 output.	N/A
D[2]	AVDD2_OCP_STAT	0	R	AVDD2 OCP Status 0 = Normal Operation (default) 1 = An over-current condition exists on AVDD2 output.	N/A
D[1]	AVDD1_OCP_STAT	0	R	AVDD1 OCP Status 0 = Normal Operation (default) 1 = An over-current condition exists on AVDD1 output.	N/A
D[0]	DVDD_OCP_STAT	0	R	DVDD OCP Status 0 = Normal Operation (default) 1 = An over-current condition exists on DVDD output.	N/A

REG0x0E: Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSD_MASK	0	R/W	Thermal Shutdown MASK 0 = No masking of interrupt (default) 1 = nINT pin and TSD_INT register will not change states when a thermal shutdown interrupt occurs.	SOFT_RESET
D[6:4]	Reserved	000	R	Reserved	N/A
D[3]	AVDD3_OCP_MASK	0	R/W	AVDD3 OCP Mask 0 = No masking of interrupt (default) 1 = nINT pin and AVDD3_OCP_INT register will not change states when AVDD3 over-current interrupt occurs.	SOFT_RESET
D[2]	AVDD2_OCP_MASK	0	R/W	AVDD2 OCP Mask 0 = No masking of interrupt (default) 1 = nINT pin and AVDD2_OCP_INT register will not change states when AVDD2 over-current interrupt occurs.	SOFT_RESET
D[1]	AVDD1_OCP_MASK	0	R/W	AVDD1 OCP Mask 0 = No masking of interrupt (default) 1 = nINT pin and AVDD1_OCP_INT register will not change states when AVDD1 over-current interrupt occurs.	SOFT_RESET
D[0]	DVDD_OCP_MASK	0	R/W	DVDD OCP Mask 0 = No masking of interrupt (default) 1 = nINT pin and DVDD_OCP_INT register will not change states when DVDD over-current interrupt occurs.	SOFT_RESET

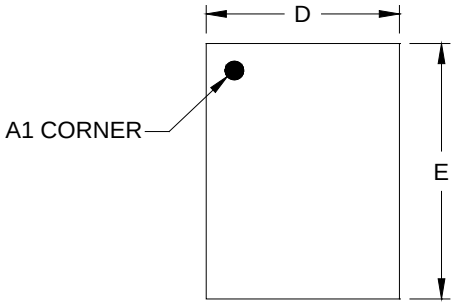
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

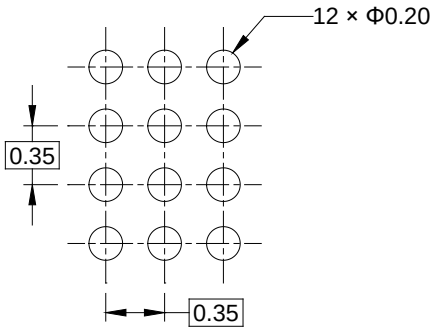
Changes from Original to REV.A (OCTOBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

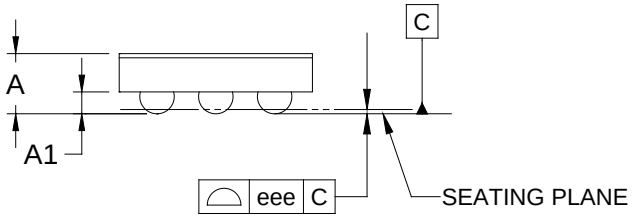
WLCSP-1.15×1.52-12B



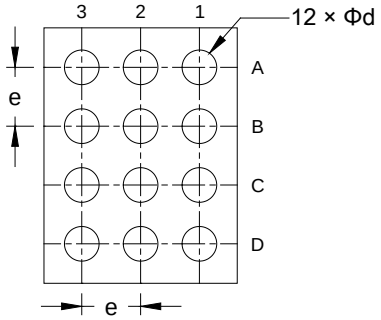
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



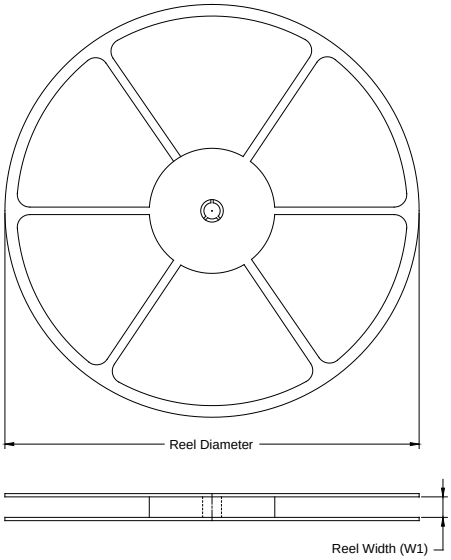
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.400
A1	0.107	-	0.147
D	1.120	-	1.180
E	1.490	-	1.550
d	0.176	-	0.236
e	0.350 BSC		
ccc	0.050		

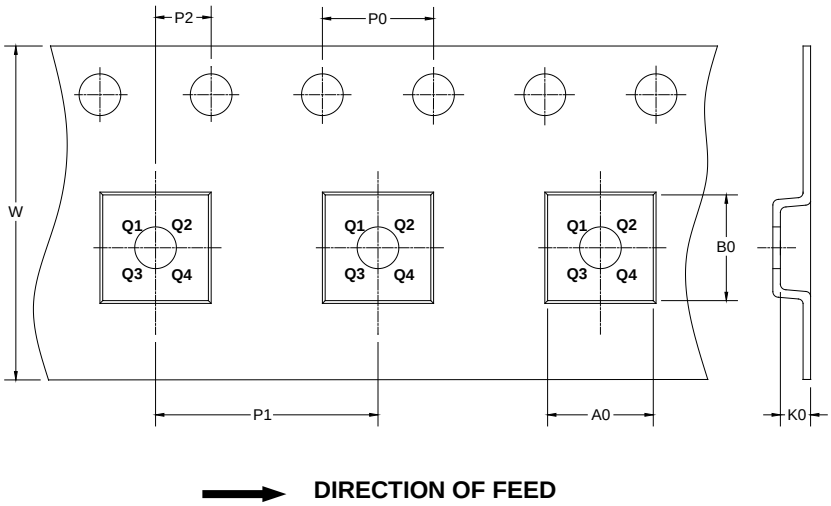
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

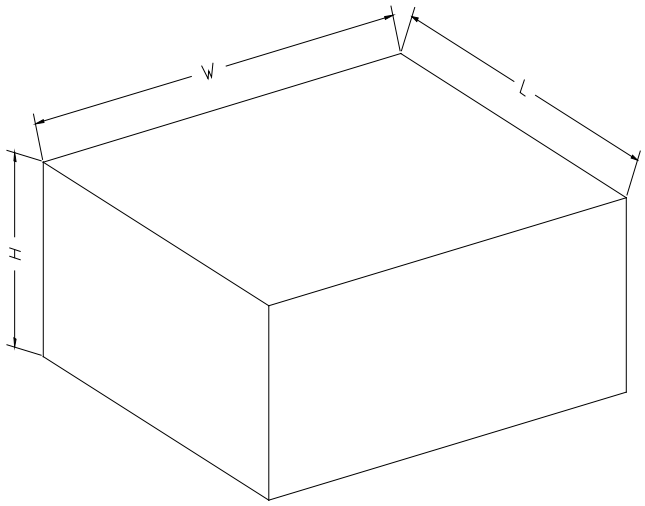
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.15×1.52-12B	7"	9.5	1.30	1.70	0.60	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002