SGM843
28V, 12-Bit, Current, Voltage and Power Monitor with an I²C Interface

GENERAL DESCRIPTION

The SGM843 is a 12-bit high-precision I²C and SMBus compatible interface current, voltage, power monitor with alert function. It operates in a wide common-mode voltage range from -0.3V to 28V and a single 2.7V to 5.5V power supply.

The SGM843 has three operating modes: continuous, triggered and shutdown modes that can reduce quiescent current. Programmable averaging and conversion times allow for more flexibility to meet the timing requirements in a variety of applications. It monitors the bus voltage existing on the IN- pin continuously. Besides, it also integrates alert functions with configured priority and can be capable of triggering an alert in cases of over-current, under-current, over-voltage, under-voltage or over-power conditions.

Considering the low input bias current feature, the device is capable of applying a larger sensing resistor, so as to ensure the accuracy of current detection within micro-amp range.

The SGM843 is available in a Green WLCSP-0.75×1.5-8B package. It is specified over the operating temperature range of -40℃ to +85℃.

FEATURES

- **2.7V to 5.5V Supply Voltage Range**
- **High-side or Low-side Sensing**
- **Current, Voltage and Power Monitor**
- **Programmable Full Scale Range: 20mV/80mV**
- **-0.3V to 28V Input Common-Mode Range**
- **Current Monitoring Accuracy:**
  - **12-bit ADC Resolution**
  - **0.4% Gain Error (MAX)**
  - **100μV Offset (MAX)**
- **Low Input Bias Current: 20nA (MAX)**
- **Programmable Averaging and Conversion Times**
- **Programmable Alert outputs**
- **1.2V, 1.8V, 3.3V, 5.0V Interface (I²C/SMBus)**
- **3 Programmable Addresses**
- **Available in a Green WLCSP-0.75×1.5-8B Package**

APPLICATIONS

Battery Monitor and Balancer
Communication Equipment
Power Management
Servers
Test Equipment

TYPICAL APPLICATION

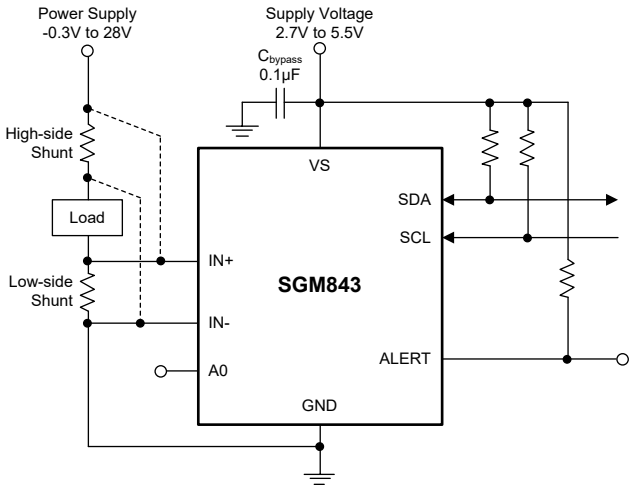


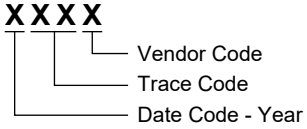
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM843A	WLCSP-0.75×1.5-8B	-40℃ to +85℃	SGM843AYG/TR	XXXX 843A	Tape and Reel, 10000
SGM843B	WLCSP-0.75×1.5-8B	-40℃ to +85℃	SGM843BYG/TR	XXXX 843B	Tape and Reel, 10000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S 6V
Differential V_{IN+} - V_{IN-} ..... -26V to 26V
Common-Mode, V_{IN+}, V_{IN-} ..... GND - 0.3V to 30V
SDA, SCL, ALERT, A0 Voltage ..... GND - 0.3V to 6V
Input Current into Any Pin 5mA
Package Thermal Resistance
WLCSP-0.75×1.5-8B, θ_{JA} ..... 159℃/W
WLCSP-0.75×1.5-8B, θ_{JB} ..... 51.5℃/W
WLCSP-0.75×1.5-8B, θ_{JC} ..... 50.4℃/W
Open-Drain Digital Output Current (SDA, ALERT) 10mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Common-Mode Input Range, V_{CM} ..... GND - 0.3V to 28V
Operating Supply Voltage ..... 2.7V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

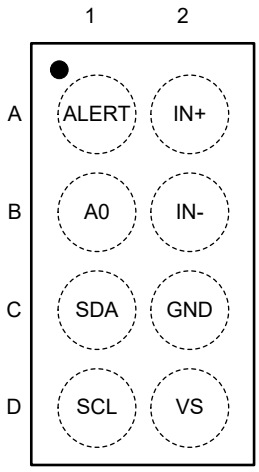
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-0.75×1.5-8B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	ALERT	DO	Multi-Functional Alert Pin.
A2	IN+	AI	Positive Input for high-side or low-side sensing.
B1	A0	DI	Address Pin. Three options: GND, SDA, or VS with corresponding addresses.
B2	IN-	AI	Negative Input for high-side or low-side sensing.
C1	SDA	DI/DO	Open-Drain Data Input/Output Pin.
C2	GND	G	Ground.
D1	SCL	DI	Open-Drain Clock Input Pin.
D2	VS	P	Power Supply.

NOTE: AI: analog input, DI: digital input, DO: digital output, DI/DO: digital input/digital output, G = ground, P= power.

ELECTRICAL CHARACTERISTICS

(V_S = 3.3V, T_A = +25℃, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV, V_{IN-} = V_{BUS} = 12V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Common-Mode Rejection	CMRR	V_{CM} = -0.3V to 28V, T_A = -40℃ to +85℃	100	120		dB
Shunt Voltage Input Range		ADCRANGE = 0	-81.92		81.88	mV
		ADCRANGE = 1	-20.48		20.47	mV
Shunt Offset Voltage	V_{OS}	V_{CM} = 12V		±40	±100	μV
Shunt Offset Voltage Drift	dV_{OS}/d_T	T_A = -40℃ to +85℃		0.2	1.0	μV/℃
IN- Bus Offset Voltage	V_{OS_B}			±25.6	±100	mV
IN- Bus Offset Voltage Drift	dV_{OS_B}/d_T	T_A = -40℃ to +85℃		10	30	μV/℃
Power Supply Rejection Ratio (Current Measurements)	$PSRR_{SHUNT}$	V_S = 2.7V to 5.5V, T_A = -40℃ to +85℃		±10		μV/V
Power Supply Rejection Ratio (Voltage Measurements)	$PSRR_{BUS}$	V_S = 2.7V to 5.5V, V_{IN-} = 1V, T_A = -40℃ to +85℃		±4		mV/V
IN- Input Impedance	Z_{IN-}	Bus voltage measurement mode		1.1		MΩ
Input Leakage	I_{B_SHDWN}	IN+, IN-, shutdown mode		0.5	18	nA
Input Bias Current	I_B	IN+, IN-, current measurement mode		1.0	20	nA
DC Accuracy						
Differential Input Impedance (IN+ to IN-)	R_{DIFF}	Shunt or current measurement modes, V_{IN+} - V_{IN-} < 82mV		450		kΩ
ADC Resolution		T_A = -40℃ to +85℃		12		Bits
1 LSB Step Size		Shunt voltage, ADCRANGE = 0		40		μV
		Shunt voltage, ADCRANGE = 1		10		μV
		Bus voltage		25.6		mV
ADC Conversion-Time (T_A = -40℃ to +85℃)		CT bit = 000	240	265	290	μs
		CT bit = 001	240	265	290	μs
		CT bit = 010	240	265	290	μs
		CT bit = 011	560	620	680	μs
		CT bit = 100	1.03	1.15	1.26	ms
		CT bit = 101	1.95	2.15	2.35	ms
		CT bit = 110	3.8	4.22	4.64	ms
		CT bit = 111	7.50	8.40	9.3	ms
Shunt Voltage Gain Error	G_{SERR}			±0.03	±0.4	%
Shunt Voltage Gain Error Drift	G_{S_DRFT}	T_A = -40℃ to +85℃		15	40	ppm/℃
VIN- Voltage Gain Error	G_{BERR}			±0.06	±0.45	%
VIN- Voltage Gain Error Drift	G_{B_DRFT}	T_A = -40℃ to +85℃		30	60	ppm/℃
Integral Non-Linearity	INL			±15		m%
Differential Non-Linearity	DNL			±0.2		LSB
Power Supply						
Quiescent Current	I_Q	V_{SENSE} = 0mV		480	580	μA
		I_Q vs. temperature, T_A = -40℃ to +85℃			600	
		Shutdown		3	5.5	
Power-On Reset Threshold	V_{POR}	V_S falling		1.6		V
SMBus						
SMBus Timeout				28	35	ms
Digital Input/Output						
Input Capacitance				4.5		pF
High-Level Input Voltage	V_{IH}	V_S = 2.7V to 5.5V, T_A = -40℃ to +85℃	1.1		5.5	V
Low-Level Input Voltage	V_{IL}	V_S = 2.7V to 5.5V, T_A = -40℃ to +85℃	0		0.4	V
Hysteresis	V_{HYS}			80		mV
Low-Level Output Voltage	V_{OL}	I_{OL} = 3mA, V_S = 2.7V to 5.5V, T_A = -40℃ to +85℃		0.25	0.5	V
Digital Leakage Input Current		0V ≤ V_{INPUT} ≤ V_S		0.05	0.3	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
I^2C Clock Frequency	f_{SCL}	1	400	10	3400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}	600		160		ns
Hold Time after Repeated START Condition (After this period, the first clock is generated.)	t_{HDSTA}	100		100		ns
Repeated START Condition Setup Time	t_{SUSTA}	100		100		ns
STOP Condition Setup Time	t_{SUSTO}	100		100		ns
Data Hold Time	t_{HDDAT}	10	900	10	70	ns
Data Setup Time	t_{SUDAT}	100		20		ns
SCL Clock Low Period	t_{LOW}	1300		160		ns
SCL Clock High Period	t_{HIGH}	600		60		ns
Data Fall Time	t_{FDA}		300		80	ns
Clock Fall Time	t_{FCL}		300		40	ns
Clock Rise Time	t_R		300		40	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000		40	ns

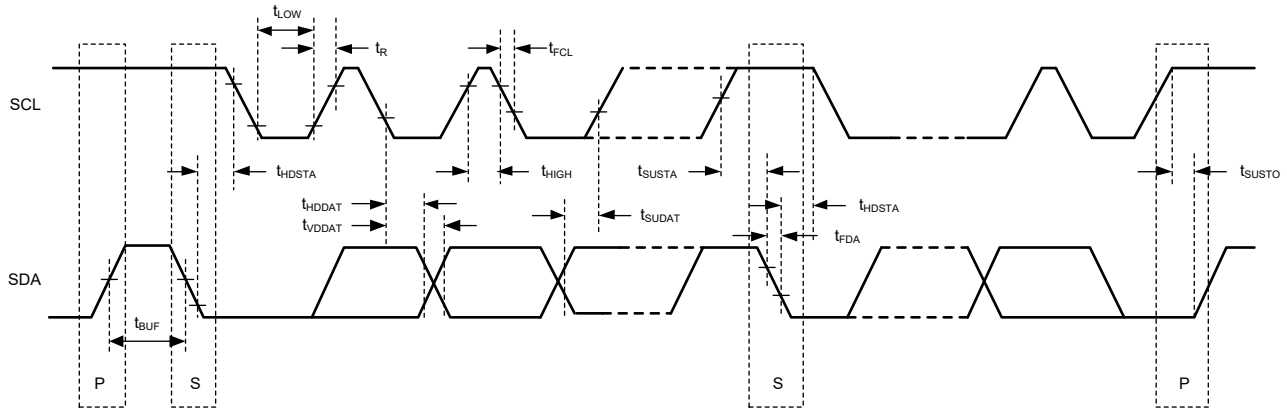
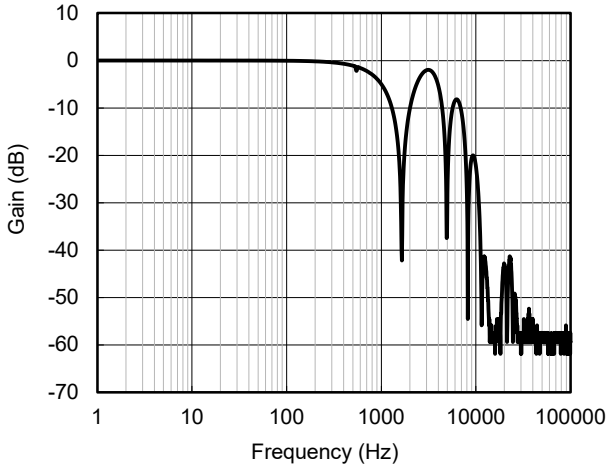


Figure 2. Bus Timing Diagram

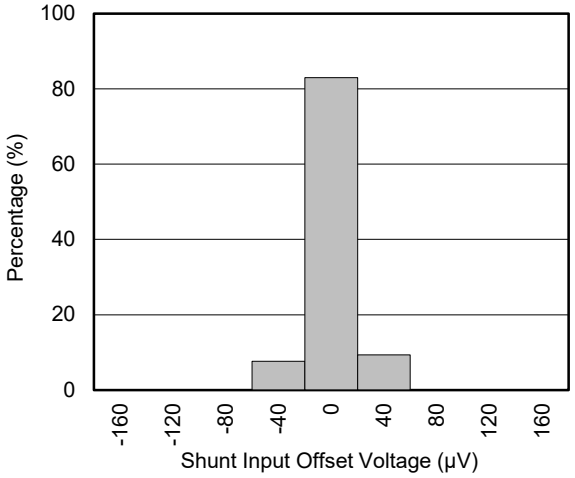
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV, unless otherwise noted.

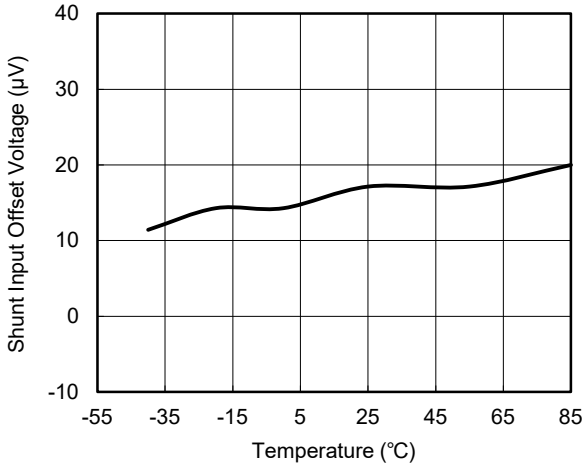
Frequency Response



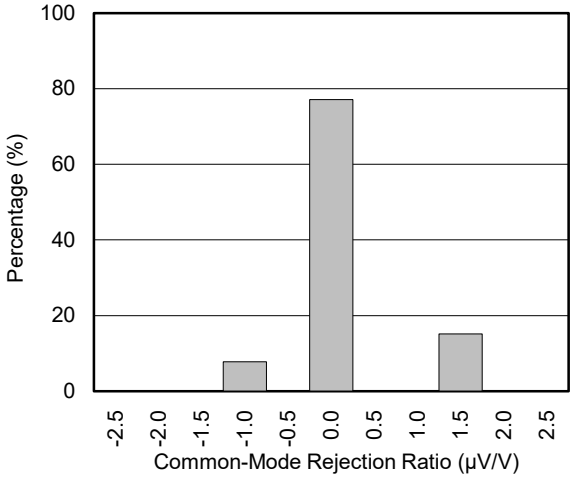
Shunt Input Offset Voltage Production Distribution



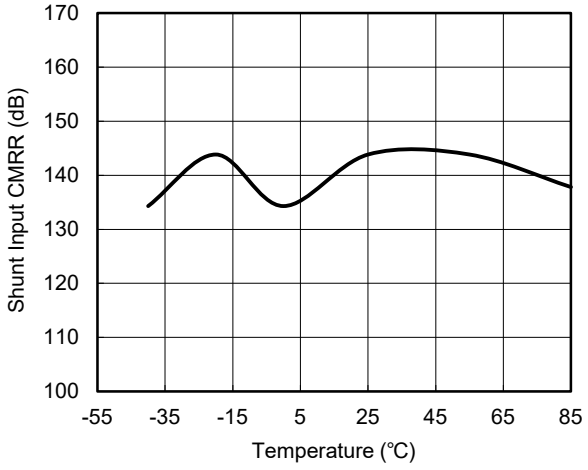
Shunt Input Offset Voltage vs. Temperature



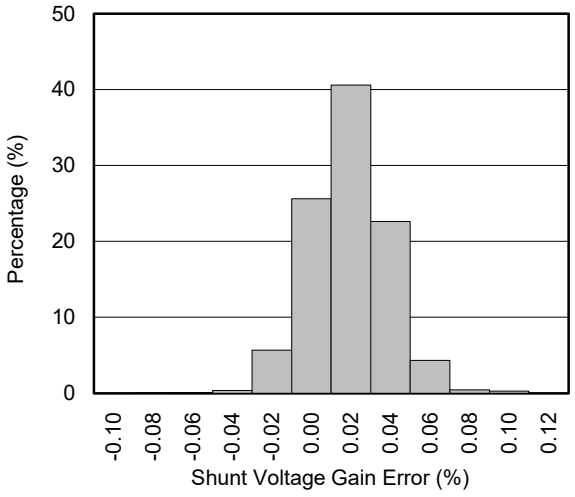
CMRR Production Distribution



Shunt Input CMRR vs. Temperature



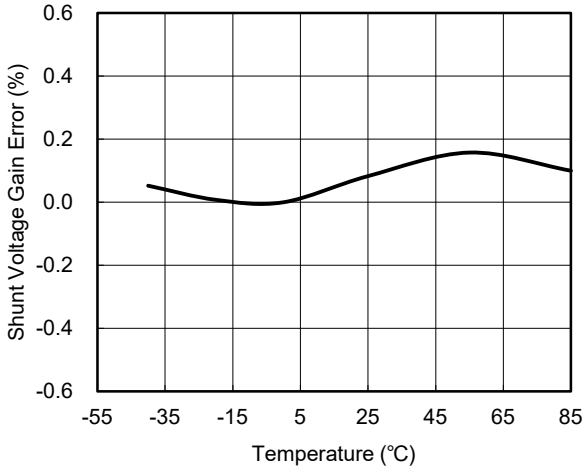
Shunt Voltage Gain Error Production Distribution



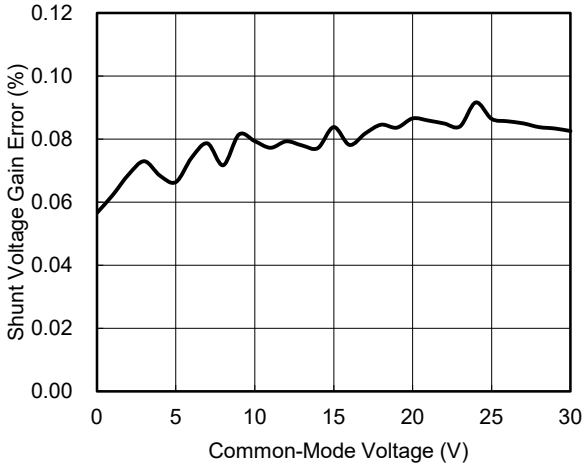
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV, unless otherwise noted.

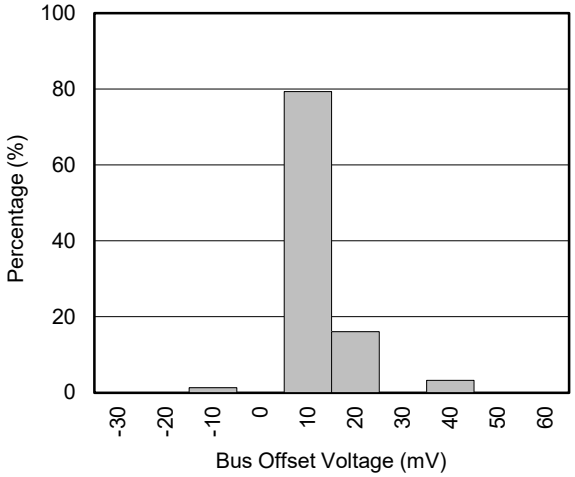
Shunt Voltage Gain Error vs. Temperature



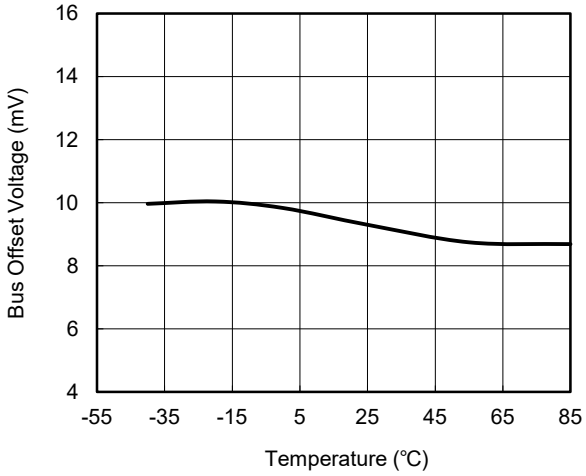
Shunt Voltage Gain Error vs. Common-Mode Voltage



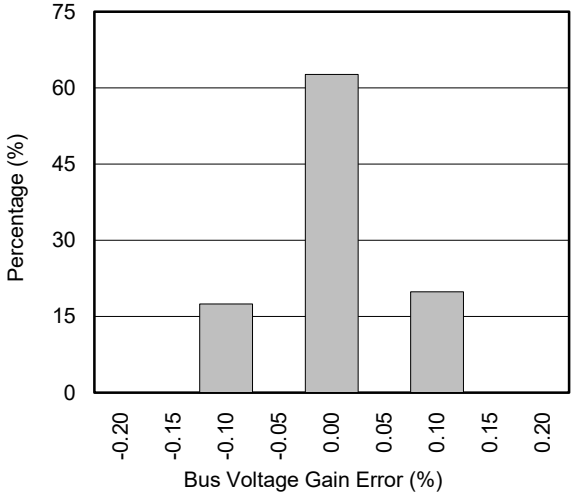
Bus Offset Voltage (V_{IN-}) Production Distribution



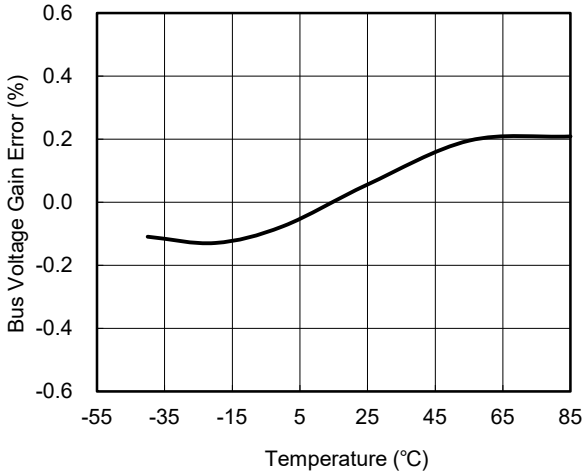
Bus Offset Voltage (V_{IN-}) vs. Temperature



Bus Voltage (V_{IN-}) Gain Error Production Distribution



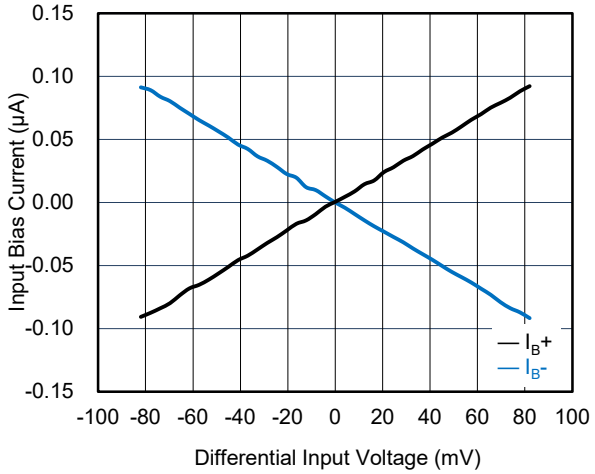
Bus Voltage (V_{IN-}) Gain Error vs. Temperature



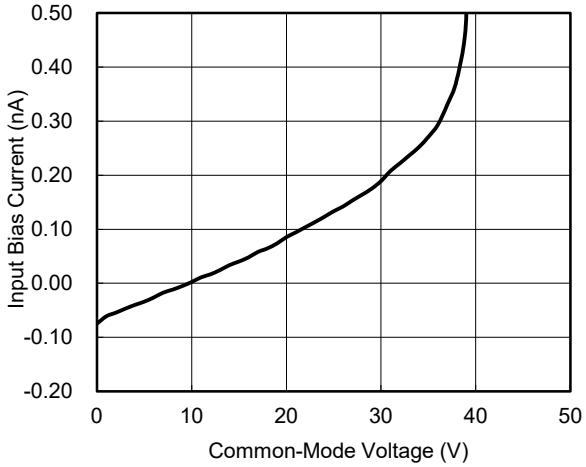
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV, unless otherwise noted.

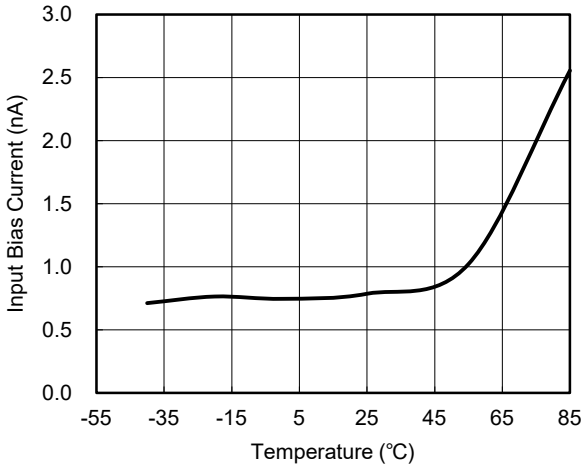
Input Bias Current vs. Differential Input Voltage



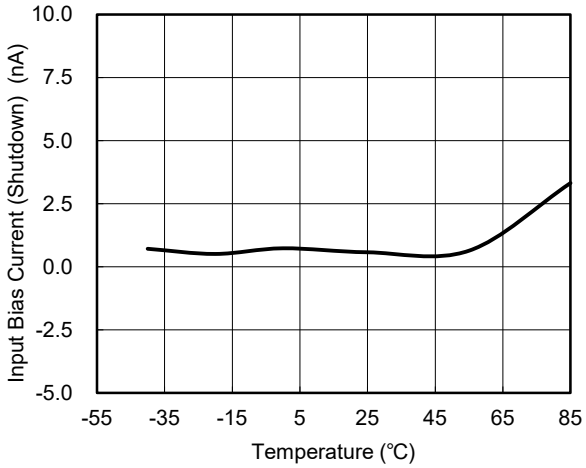
Input Bias Current vs. Common-Mode Voltage (I_{B+}, I_{B-})



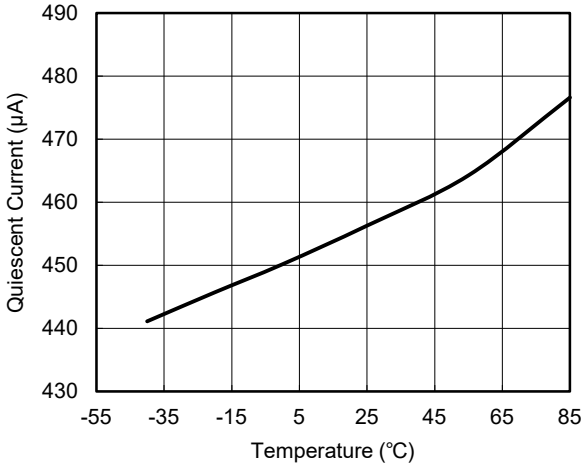
Input Bias Current vs. Temperature



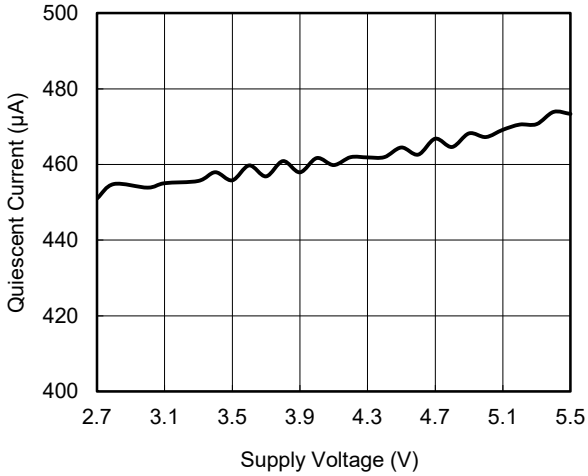
Input Bias Current vs. Temperature (Shutdown)



Quiescent Current vs. Temperature



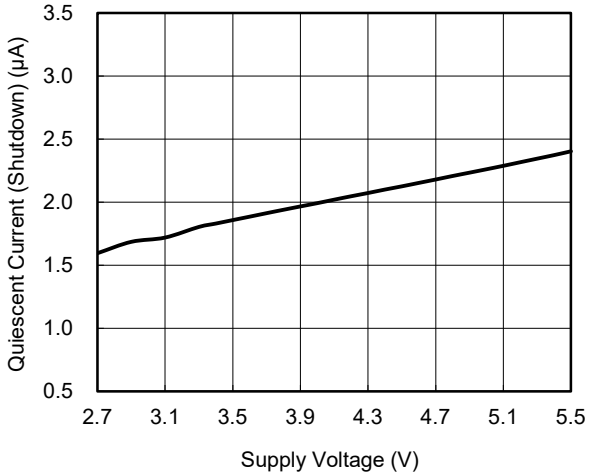
Quiescent Current vs. Supply Voltage



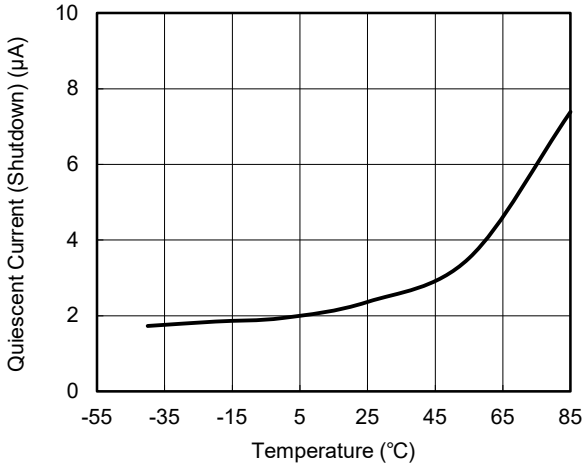
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{VS} = 3.3V, V_{CM} = 12V, V_{SENSE} = (V_{IN+} - V_{IN-}) = 0mV, unless otherwise noted.

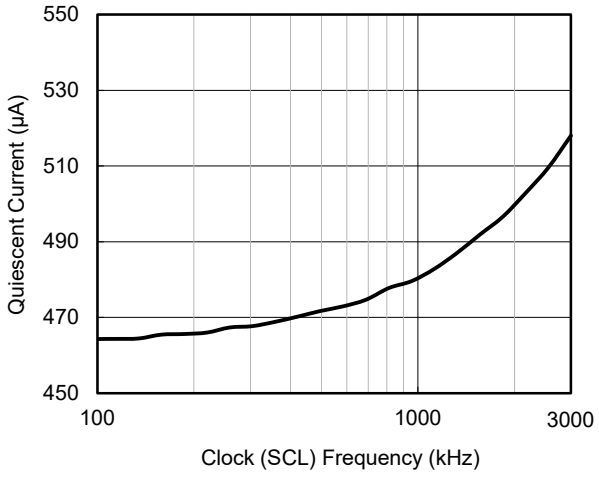
Quiescent Current (Shutdown) vs. Supply Voltage



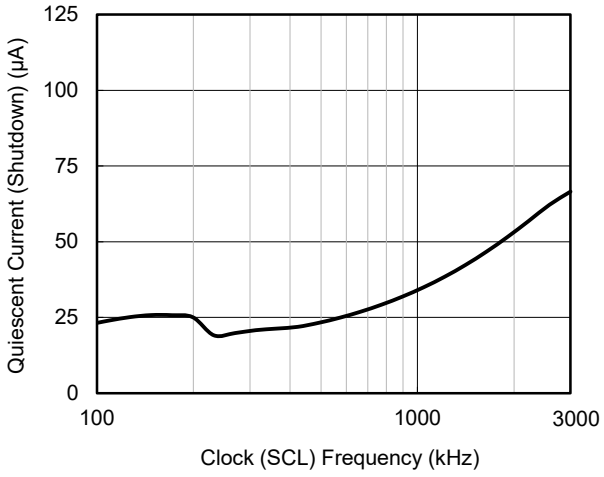
Quiescent Current (Shutdown) vs. Temperature



Quiescent Current vs. Clock (SCL) Frequency



Quiescent Current (Shutdown) vs. SCL Frequency



FUNCTIONAL BLOCK DIAGRAM

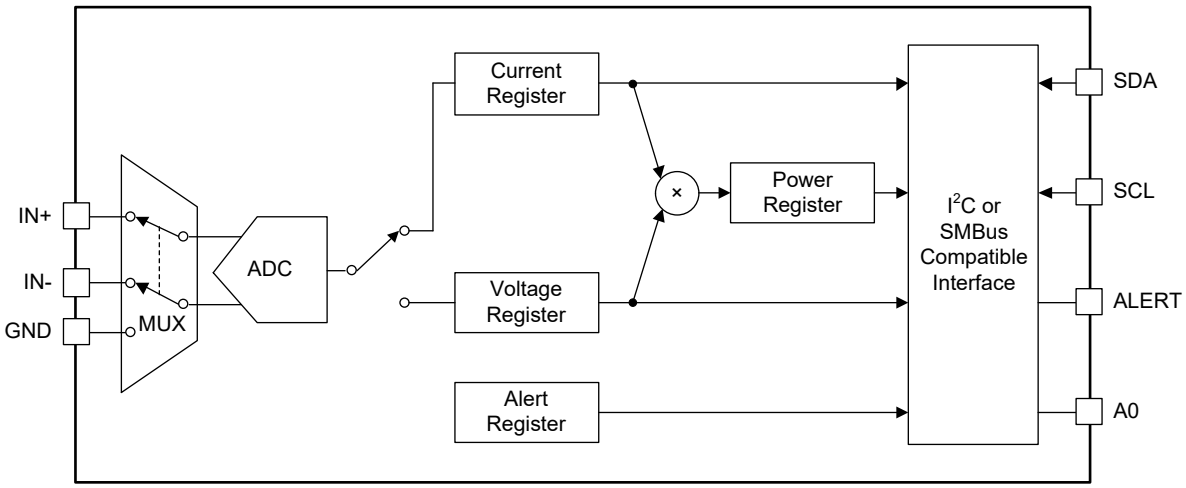


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM843 is a 12-bit current, voltage and power monitor with I²C interface. The device senses both shunt and bus voltages, and provides digital voltages, current and power readings in the data registers. Besides, it provides programmable registers to flexibly configure the device such as operating modes, conversion time, averaging times and alert functions.

Feature Description

Voltage and Current Measurement

The SGM843 is capable of measuring two distinct input voltages: the differential voltage across the IN+ and IN- terminals, as well as the bus voltage between the IN- pin and ground. Powered by a supply voltage ranging from 2.7V to 5.5V, the device supports current sensing and bus voltage monitoring on power rails up to 28V. The input common-mode voltage of the SGM843 can exceed its supply voltage, since its input circuitry operates independently of the device power domain. The voltage monitored at the IN- pin, typically representing the system bus voltage when adopting the high-side shunt sensing architecture, covers a range from 0V to 28V. Because the device's power supply is isolated from its input voltage, no special constraints are imposed on the power-up sequence. As a result, bus and shunt voltages can be safely applied to the input terminals even when the device is in a power-off state.

In typical applications, a current-sense shunt resistor is connected between the IN+ and IN- pins. And the load current flowing through this resistor generates a differential shunt voltage that is then measured by the device. Meanwhile, the bus voltage relative to ground is sensed via the IN- pin in the high-side shunt sensing architecture.

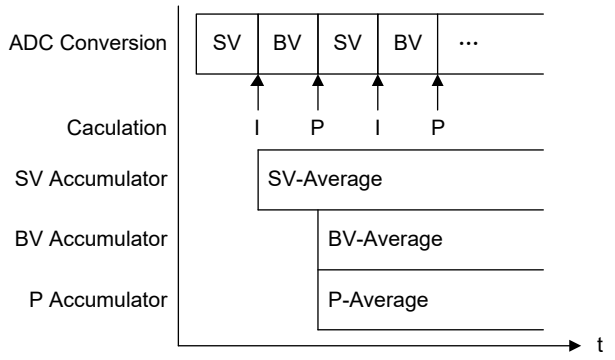
Power Calculation

Upon completion of each shunt voltage and bus voltage measurement, the corresponding current and power are calculated, as illustrated in Figure 4. The current calculation is performed in accordance with the value configured in the SHUNT_CAL[14:0] in the Calibration register (05h) immediately following a shunt voltage measurement. In the event that no value is written to the SHUNT_CAL, the current result stored in the Current register will be zero. Likewise, the power calculation is executed based on the measured bus voltage and the previously newly-calculated current value after each bus voltage sampling. Similarly, the power value retained in the Power register will default to zero if the SHUNT_CAL register remains no value.

DETAILED DESCRIPTION (continued)

With the exception of cases where the averaging time is set to 1, the calculated current and power values are treated as intermediate results and stored within an accumulator instead of the direct output data registers. During each conversion sequence, the newly calculated current and power values are cumulatively added to the previously accumulated data until the specified number of averaging sequences is attained. Subsequently, the accumulated values are averaged, and the final current and power results are updated into their corresponding output registers.

Similar to the current and power values, the shunt voltage and bus voltage measurements are also acquired and accumulated after each measurement sequence. Once the number of conversion sequences meets the predefined averaging count, the accumulated voltage values are averaged, and the final results are updated to the corresponding voltage registers.



Note: SV: Shunt Voltage; BV: Bus Voltage; I: Current; P: Power.

Figure 4. Power Calculation Scheme

Low Bias Current

The SGM843 features an extremely low input bias current, which provides significant advantages in power consumption control for the device under both active and shutdown states. Specifically, the minimal input bias current effectively reduces unnecessary power dissipation by minimizing the leakage current flowing through the amplifier's input stage, thereby improving the overall power efficiency of the system. This power-saving characteristic is particularly critical in low-power electronic applications, where extending battery lifespan and reducing energy consumption are core design criteria.

Another advantage associated with the low input bias current of the SGM843 is its compatibility with the integration of the filter circuit at the front end of the digital current sensing amplifier. The filter configuration, which can be designed as passive RC filters, is capable of suppressing high-frequency noise introduced by the surrounding electronic environment or the sensing circuit itself. Furthermore, the low input bias current of the SGM843 enables the adoption of sensing resistors with larger resistance values in the current detection circuit. This capability is of great significance for improving the precision of current measurement, especially in the sub-mA range. In low-current detection scenarios, the voltage drop across the sensing resistor is typically extremely small; the use of a larger sensing resistor can amplify this voltage drop to a measurable range without resulting in excessive power loss.

When the sensed current is zero, the input bias current of SGM843 is the smallest. When the detection current increases and the differential voltage drop on the sense resistor becomes larger, the input bias current will gradually increase.

ALERT Function

The SGM843 features an open-drain ALERT pin that can respond to any of the five selectable alert functions or a conversion ready signal. These alert functions include shunt voltage over-limit (SOL), shunt voltage under-limit (SUL), bus voltage over-limit (BOL), bus voltage under-limit (BUL) and power over-limit (POL). The alert functions and conversion ready signal can be individually activated via the corresponding Mask/Enable registers (06h, D[15:10]). The device incorporates dedicated Alert Limit register which is used to establish the reference values for comparison operations. The ALERT pin is asserted to its active state whenever an alert condition is detected. Besides, only a single alert function can be activated and monitored at any given time. In scenarios where multiple alert functions are enabled simultaneously, the function associated with the highest-order bit position is granted priority and is compared in accordance with the value configured in the Alert Limit register. For example, in the event that both SOL and SUL are selected, the ALERT pin will be activated as soon as each individual shunt voltage conversion result which is stored within an accumulator during the conversion sequence exceeds the threshold specified in the Alert Limit register.

DETAILED DESCRIPTION (continued)

The ALERT pin can also be configured to monitor the conversion ready state through setting the CNVR bit of the Mask/Enable register (06h, D[10]). The ALERT pin is asserted when the device has finished the previous conversion and the conversion ready flag is set. The conversion ready flag (CVRF) bit can be monitored at the ALERT pin in conjunction with any of the available alert functions. In situations where both an alert function and the CNVR bit are enabled for monitoring via the ALERT pin, it is necessary to read the CVRF bit (06h, D[3]) and the AFF bit (06h, D[4]) within the Mask/Enable register following an alert assertion, so as to identify the actual alert source. If the corresponding bits in Mask/Enable registers (06h, D[15:10]) remain disabled, the ALERT pin will not take any action.

The SGM843 incorporates an alert latch mechanism, which can be activated by configuring the LEN (Alert Latch Enable) bit in the Mask/Enable register (06h, D[0]). Once triggered, this function retains the ALERT pin in a persistent asserted state. Besides, the AFF bit and ALERT pin can be reset by performing a read operation on the Mask/Enable register (06h) when LEN = 1. When LEN = 0, the ALERT pin and AFF flag are automatically cleared at the end of the conversion once the alert condition is no longer present.

The SGM843 provides configurable alert polarity. Setting the APOL (Alert Polarity) bit in the Mask/Enable register (06h, D[1]) high configures the ALERT pin as active-high when asserted, and its open-drain output requires an external resistor pulled up to the supply voltage.

Most importantly, the alert function assesses whether each individual conversion result meets the predefined alert threshold. As an example, when the shunt voltage over-limit (SOL) or the shunt voltage under-limit (SUL) alert function is activated, the value stored in the Alert Limit register is compared with the measured shunt voltage after each shunt voltage conversion, so as to judge whether the measured value has exceeded the predefined threshold. Besides, the bus voltage alert functions (BOL and BUL) will compare the sampled bus voltage with the Alert Limit register upon completion of each bus voltage conversion. Similarly, the power over-limit (POL) alert function compares the calculated power value against the predefined threshold after each bus voltage conversion.

Device Functional Modes

Continuous Mode and Triggered Mode

The SGM843 supports two operational modes, namely continuous mode and triggered mode, which govern the operational behavior of the ADC during subsequent conversion sequences.

In continuous mode, when MODE[2:0] in the Configuration register (00h) is configured to 111b, the device performs continuous conversions, where a shunt voltage measurement is sequentially followed by a bus voltage measurement. Besides, when MODE[2:0] in Configuration register (00h) is configured to 101b, the device only performs continuous conversions of the shunt voltage measurement.

In triggered mode, when MODE[2:0] in the Configuration register (00h) is configured to 011b, the device initiates a one-shot conversion, generating a single set of measurement outputs, where a shunt voltage measurement and a bus voltage measurement perform only once. Besides, when MODE[2:0] in Configuration register (00h) is configured to 001b, the device performs a shunt voltage measurement only once. To trigger next one-shot conversion, a write operation to the Configuration register (00h) is mandatory, even if the operating mode remains unaltered.

The CVRF bit in the Mask/Enable register (06h) is asserted upon the full completion of all conversion, averaging, and multiplication procedures within one measurement cycle. Furthermore, the CVRF bit can be cleared under the two following conditions. One is a write operation to the Configuration register (00h), which excludes shutdown mode, the other is a read operation executed on the Mask/Enable register (06h).

Shutdown Mode

The SGM843 features a shutdown mode enabled when the MODE[2:0] bit in the Configuration register (00h) is configured to 000b or 100b. In shutdown mode, the quiescent current drops significantly to reduce power consumption. Register access via I²C remains operational during shutdown. ADC conversions resume only after reconfiguring the MODE[2:0] bits to an active state.

DETAILED DESCRIPTION (continued)

Power-On Reset and Software Reset

The device initiates a power-on reset (POR) when the supply voltage drops below 1.6V (TYP), restoring all registers to default values. Alternatively, initiate a manual register reset by asserting the RST bit in the Configuration register (00h, D[15]). Default register values are provided in the Register Maps section.

Flexible Conversion Times and Averaging

The conversion times and averaging are programmed via the Configuration Register (00h). Six levels of conversion time from 265μs to 8.4ms are available. The programmable conversion and average times allow the device to match different time requirements in real applications. For example, if a system requires reading the shunt voltage and bus voltage every 5ms, the conversion time for shunt and bus voltage measurement can be set to 620μs, with the average time set to 4. With this configuration, the shunt and bus voltage values are updated approximately every 4.96ms. Also, the conversion time for shunt and bus voltage measurement can be different, which allows the device to focus on one of the two voltages. Suppose the system desires more conversion time for shunt voltage, 4.22ms of conversion time can be set for shunt voltage and 620μs of conversion time for bus voltage while average time setting to '1'. With this configuration, the shunt and bus voltage values are updated approximately every 4.84ms.

There are trade-offs between the conversion times and average times used. The averaging can filter the input signal, thus effectively improving the measurement accuracy. With more average times, the device would reduce the noise of the input signal more effectively.

Similarly, the conversion time also affects the measurement accuracy. A longer conversion time results in better measurement accuracy. Therefore, to achieve the highest measurement accuracy, use the longest conversion time with the most average times, under the premise of meeting the system's time requirements. The impact of conversion time and averaging on an input signal is demonstrated in Figure 5 and Figure 6 below.

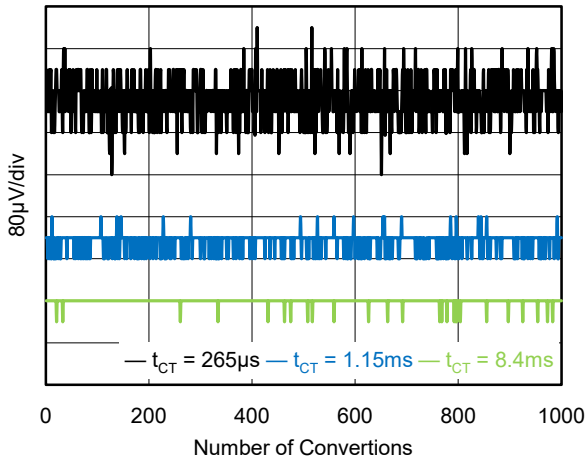


Figure 5.Noise vs. Conversion Time (Averaging = 1)

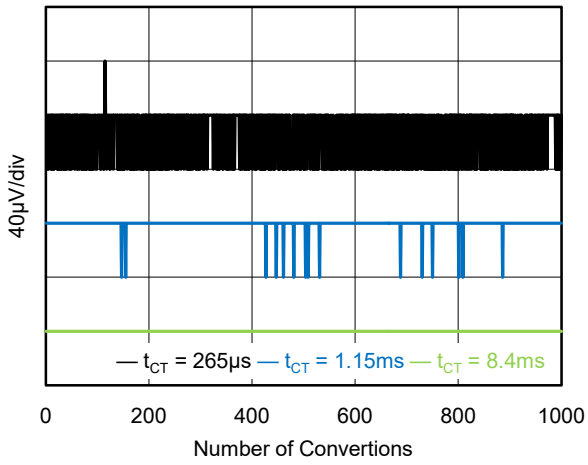


Figure 6. Noise vs. Conversion Time (Averaging = 16)

DETAILED DESCRIPTION (continued)

Programming

Serial Bus Address

For the definition of I²C communication, before sending data, the master device should address the specified slave device. There are seven bits for the address of the slave device and another one bit is for the command of reading or writing.

Table 1. Address Pin and Slave Addresses

A0	Slave Address for SGM843A	Slave Address for SGM843B
GND	1000000	1001000
VS	1000001	1001001
SDA	1000010	1001010

A0 is used to determine the address of the device. As shown in Table 1, if A0 is at different logic levels, the A and B versions of the device will have different addresses. The device will sample the state of A0 pin before each communication, so it is necessary to ensure the stability of the state of A0 pin before any actions are taken on the interface.

Serial Interface

On the I²C bus or SMBus, the SGM843 can be operated as a slave device, which is controlled by the master. When connecting to the bus, both SDA and SCL pins are connected through the topology of open-drain. In addition, in order to improve the performance of slave devices under the condition of input spikes and noise bus, filter and Schmitt flip-flop are adopted. Although the device has integrated tip suppression in the digital I/O lines, it is recommended that proper layout be used to minimize coupling in the communication lines. Noise in communication lines mainly comes from two sources: capacitive coupling generated at the signal edges between two communication lines, or switching noise generated by other parts of the system. Keeping lines parallel to ground when routing can reduce coupling effects between communication lines. In addition, shielded signal lines reduce the possibility of unintended noise coupling into digital I/O lines that could be misinterpreted as a START or STOP command.

There are four modes of transmission protocol: standard mode (100kHz), fast mode (400kHz), fast mode plus (1MHz) and high-speed mode (3.4MHz). MSB is the first bit to be transferred when transmitting a byte.

Writing and Reading Operation

In order to access the specified pointer register of SGM843, it is necessary to send the values of the desired pointer register after addressing the slave device. As already illustrated in Figure 7, the values of pointer register are required after each write command.

The first byte written to a register is the address of the slave device, and R/$\overline{W}$ bit is low, then the device acknowledges receipt of a valid address. The second byte sent by the host is the address of the register to be written, which updates the register pointer to the desired register. The following two bytes are written to the register addressed by the register pointer, and the device then acknowledges receipt of each byte. Finally, the master generates a START or STOP condition to terminate data transfer (Figure 8).

If the master device desires to read the information of the specified register, a write command must be sent by the master at first to indicate which pointer register is needed. First, the slave address should be sent with the low state of R/$\overline{W}$ bit, followed by the address of the pointer address (Figure 7). Second, the START command should be sent by the master, the slave address of the specified SGM843, and then followed by the high state of R/$\overline{W}$ bit to indicate a read command (Figure 9). The slave transmits the next byte, which is the most significant byte of the register indicated by the register pointer. For the condition of repeated reading, it is not required to send the bytes of pointer register again, unless the device is reset or the address of pointer register is altered by the write command.

DETAILED DESCRIPTION (continued)

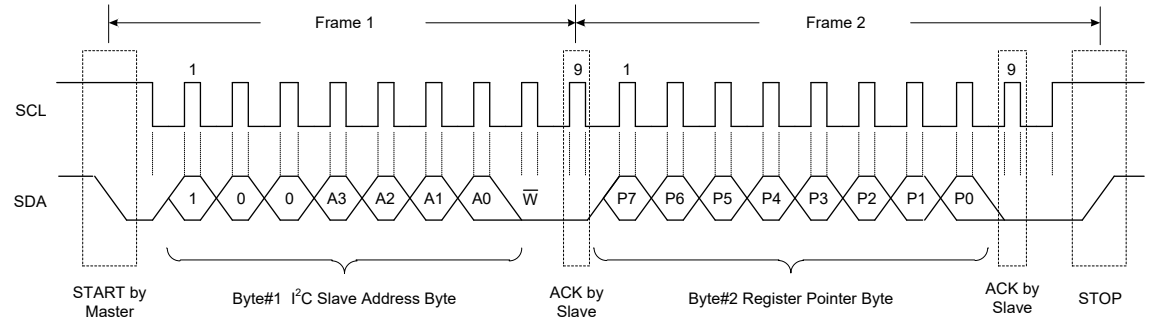
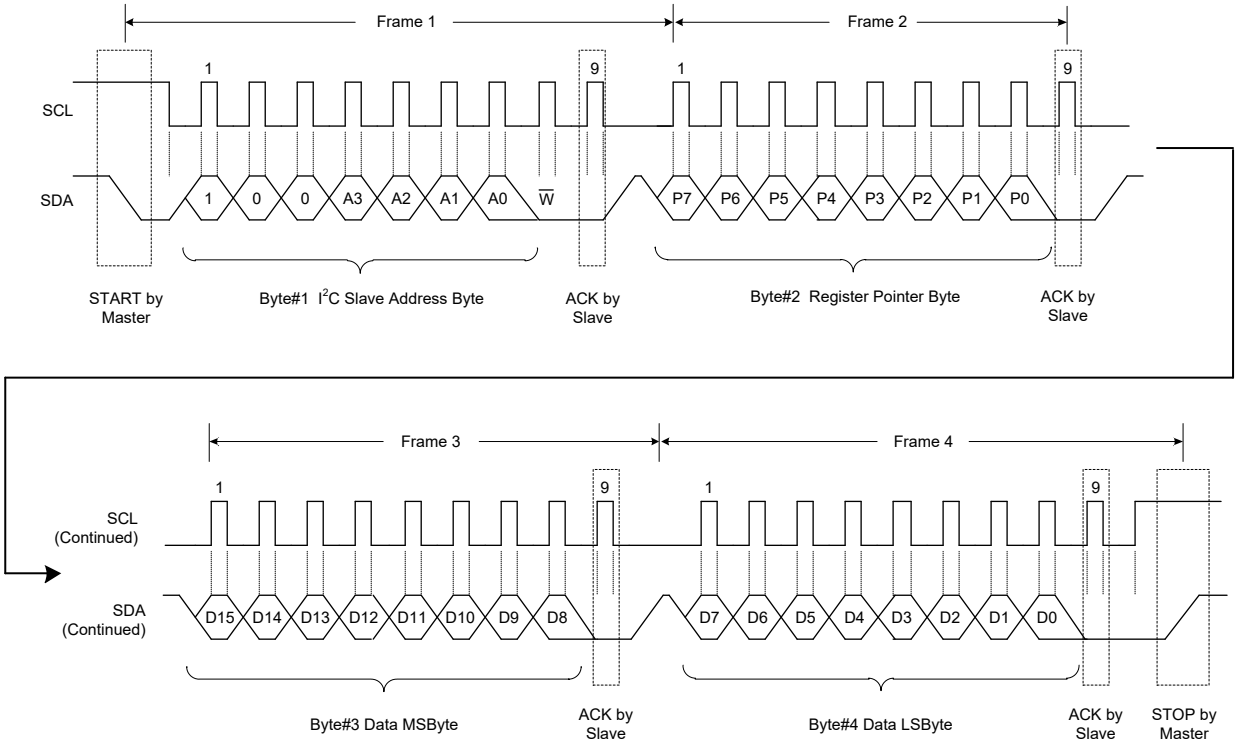
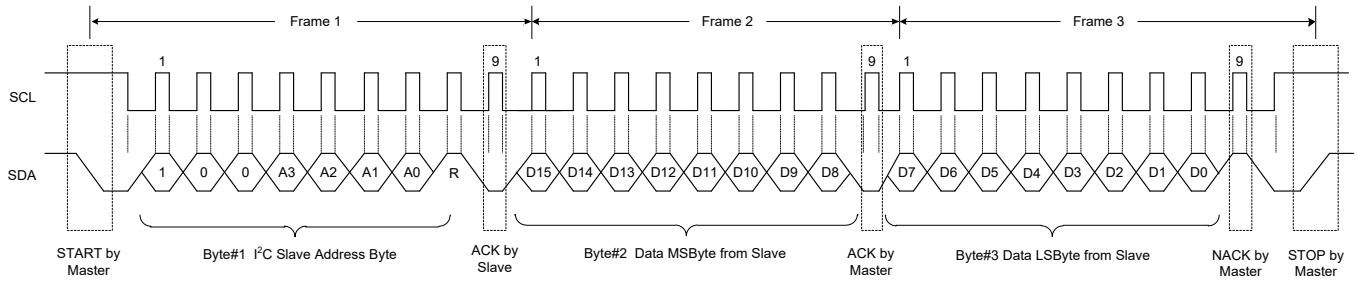


Figure 7. Typical Register Pointer Set



NOTE: The device does not support packet error checking (PEC) or perform clock stretching.

Figure 8. Register Write Word Format



NOTE: The device does not support packet error checking (PEC) or perform clock stretching.

Figure 9. Register Read Word Format

DETAILED DESCRIPTION (continued)

High-Speed (HS) I²C Mode

The SGM843 also supports high-speed (HS) I²C mode whose data rate reaches up to 3.4MHz. To enable this mode, the master device sends a START condition. After the START, a master code is transmitted '00001XXX', followed by a mandatory Not Acknowledge (NACK) condition. Note that the master code is sent in Fast mode or Standard mode, which is at most 400kHz.

The three lowest bits of the master code are used to identify different I²C masters on the same bus. The user should guarantee that each master device has its unique identifier.

After the NACK condition, the high-speed transfer begins. At the master device side, the master device sends a REPEATED START condition followed by the slave address and the remaining data, the same as the frame in Fast mode or Standard mode, but operates at a higher speed. At the slave device side, the SGM843 switches the internal circuit to support HS mode. To keep the bus in HS mode, the user should avoid using the STOP condition and use the REPEATED START condition instead. A STOP condition makes the SGM843 switch back to support Fast mode or Standard mode.

General Call Reset Operation

A reset operation for multiple slaves can be implemented through general call by using the general call address 0000 000, where the final R/$\overline{W}$ bit is set to 0. Subsequently, the data byte 0000 0110 (06h) is sent. Upon receiving this two-byte sequence, every SGM843 device which responds to the address will perform a soft reset and revert to the initial power-up states.

General Call Start Byte

By setting the general call address to 0000 000 and setting the last R/$\overline{W}$ bit to 1, a general call ADC conversion start command can be issued to multiple SGM843 devices without requiring additional data bytes.

Please note that other devices on the bus that use the general call start command will also trigger the start of conversion.

SMBus Alert Response

The SGM843 has the ability to respond to the SMBus alert response that has the ability to identify a quick fault for simple slaves. The master broadcasts the alert response slave address (0001100) and the R/$\overline{W}$ bit is high. The slave that generates the ALERT signal will send its own address through the bus after recognizing the alert response. The host can identify the slave that generates the alert after receiving the slave address.

The alert response is similar to the I²C broadcast call, which may cause multiple slave devices to respond at the same time, and the bus arbitration rules is applied at this time. The losing device will not generate an Acknowledge but continue to pull the alert line low until it is the device's turn to complete the Acknowledge at which point the alert event will be cleared.

REGISTER MAPS

I²C Register Set Summary

The SGM843A uses multiple registers to hold configuration information, test results, threshold settings and status information. All device registers are 16 bits, 2 bytes, and communicate through the I²C interface.

Address	Register Name	Register Size (bits)	Reset Value
00h	Configuration Register	16	41B7h
01h	Shunt Voltage Register	16	0000h
02h	Bus Voltage Register	16	0000h
03h	Power Register	16	0000h
04h	Current Register	16	0000h
05h	Calibration Register	16	0000h
06h	Mask/Enable Register	16	0000h
07h	Alert Limit Register	16	0000h
3Eh	Manufacturer ID Register	16	5449h
3Fh	Device ID Register	16	A480h

NOTE: Type: R = Read-Only, R/$\overline{W}$ = Read/Write.

REGISTER MAPS (continued)

00h: Configuration Register (Reset = 41B7h)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RST	0b	R/W	Reset Bit. When this bit is set to 1, the system will be reset as the power-on reset. It means that all registers are set to their default values. This bit self-clears.
D[14:13]	Reserved	10b	R	Reserved.
D[12]	ADCRANGE	0b	R/W	This bit allows for the configuration of the shunt full-scale input range between IN+ and IN-. 0b = Range is -81.92mV to 81.88mV 1b = Range is -20.48mV to 20.47mV
D[11:9]	AVG[2:0]	000b	R/W	Averaging Mode. Determine the number of samples collected and averaged. 000b = 1 001b = 4 010b = 16 011b = 64 100b = 128 101b = 256 110b = 512 111b = 1024
D[8:6]	VBUSCT[2:0]	110b	R/W	Bus Voltage Conversion Time. Set the conversion time for the bus voltage measurement. 000b = 265μs 001b = 265μs 010b = 265μs 011b = 620μs 100b = 1150μs 101b = 2150μs 110b = 4220μs 111b = 8400μs
D[5:3]	VSHCT[2:0]	110b	R/W	Shunt Voltage Conversion Time. Set the conversion time for the shunt voltage measurement. 000b = 265μs 001b = 265μs 010b = 265μs 011b = 620μs 100b = 1150μs 101b = 2150μs 110b = 4220μs 111b = 8400μs
D[2:0]	MODE[2:0]	111b	R/W	Operating Mode. Select the operation modes, continuous, triggered or shutdown. These bits default to continuous shunt and bus measurement mode. 000b = Shutdown 001b = Shunt voltage triggered, single shot 010b = Bus voltage triggered, single shot 011b = Shunt voltage and bus voltage triggered, single shot 100b = Shutdown 101b = Continuous shunt voltage 110b = Continuous bus voltage 111b = Continuous shunt and bus voltage

REGISTER MAPS (continued)

01h: Shunt Voltage Register (Reset = 0000h)

The Shunt Voltage register is used to store the shunt voltage reading, V_{SHUNT}. Positive numbers are directly displayed in binary format, while negative numbers are displayed in two's complement format. The two's complement of the negative number can be obtained by taking the binary complement of the absolute value of the negative number and adding one. An MSB = 1 indicates that it is a negative number.

For example: assuming V_{SHUNT} = -80mV (ADCRANGE = 0, range = -81.92mV to 81.88mV):

1. Convert the absolute value (80mV) to a decimal integer in LSBs (80mV/40μV) = 2000
2. Convert this number to 12 bits binary = 0111 1101 0000
3. Complement this 12 bits binary = 1000 0010 1111
4. Add 1 to the complement to get the two's complement = 1000 0011 0000 = 830h
5. Left shifting 4 bits to get the register value= 1000 0011 0000 0000= 8300h.

The register will display the averaged value if averaging enabled.

If full-scale range of shunt voltage is configured as -81.92mV to 81.88mV (ADCRANGE = 0), the LSB is 40μV. And if full-scale range of shunt voltage is configured as -20.48mV to 20.47mV (ADCRANGE = 1), the LSB is 10μV.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:4]	VSHUNT[11:0]	000h	R	Shunt-Voltage Data Bits. Two's complement format.
D[3:0]	RESERVED	0h	R	Reserved.

02h: Bus Voltage Register (Reset = 0000h)

The Bus Voltage register is used to store the bus voltage reading, V_{BUS}. The register will display the averaged value if averaging enabled. The LSB is 25.6mV.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RESERVED	0b	R	Reserved.
D[14:4]	VBUS[10:0]	000h	R	Bus-Voltage Data Bits.
D[3:0]	RESERVED	0h	R	Reserved.

03h: Power Register (Reset = 0000h)

The register will display the averaged power value if averaging enabled.

The power is obtained by multiplying the measured bus voltage with the measured current. And the Power Register displays power values in watts.

Set the resolution of the Power Register (03h) to 32 times the programmed Current_LSB internally.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	POWER[15:0]	0000h	R	Power Data Bits. An unsigned value.

04h: Current Register (Reset = 0000h)

The register will display the averaged current value if averaging enabled.

Multiply the decimal value of the Shunt Voltage register (D[15:4]) and the decimal value of the Calibration register (D[14:0]) together, and then divide by 2048 to calculate the decimal value of the Current register (D[15:4]).

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:4]	CURRENT[11:0]	000h	R	Current Data Bits. Two's complement format.
D[3:0]	RESERVED	0h	R	Reserved.

REGISTER MAPS (continued)

05h: Calibration Register (Reset = 0000h)

This register provides the value of the shunt resistor to the device and sets the resolution of the Current register. Then Current_LSB and Power_LSB are also determined. This register can also be used for system current calibration.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	Reserved	0b	R	Reserved.
D[14:0]	SHUNT_CAL[14:0]	0000h	R/W	Programmed Calibration Data Bits.

06h: Mask/Enable Register (Reset = 0000h)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	SOL	0b	R/W	Over-Voltage Alert Function of Shunt Voltage. If the shunt voltage ADC output exceeds the set value in 07h register, set this bit high to assert the ALERT pin.
D[14]	SUL	0b	R/W	Under-Voltage Alert Function of Shunt Voltage. If the shunt voltage ADC output is lower than the set value in 07h register, set this bit high to assert the ALERT pin.
D[13]	BOL	0b	R/W	Over-Voltage Alert Function of Bus Voltage. If the bus voltage ADC output exceeds the set value in 07h register, set this bit high to assert the ALERT pin.
D[12]	BUL	0b	R/W	Under-Voltage Alert Function of Bus Voltage. If the bus voltage ADC output is lower than the set value in 07h register, set this bit high to assert the ALERT pin.
D[11]	POL	0b	R/W	Over-Power Alert Function. If the internal multiplier calculated power ADC output exceeds the set value in 07h register, set this bit high to assert the ALERT pin.
D[10]	CNVR	0b	R/W	Conversion Ready Function. Set it high to assert the ALERT pin when the CVRF bit is asserted high.
D[9:6]	RESERVED	0000b	R	Reserved.
D[5]	Mem Error	0b	R	CRC or ECC error.
D[4]	AFF	0b	R	Alert Function Flag. Assert the alert function flag when any of the enabled limit events is triggered (SOL, SUL, BOL, BUL, POL). In the event that the LEN bit is configured to 1, the AFF bit will be cleared upon reading the 06h register. Besides, when the LEN bit is set to 0, the AFF bit gets cleared after the subsequent conversion that does not trigger an alert condition.
D[3]	CVRF	0b	R	Conversion Ready Flag. Setting it high indicates that all the measurements are finished. The bit can be cleared under two conditions: 1. Configure register writing (except for shutdown mode). 2. Mask/Enable register reading.
D[2]	OVF	0b	R	Math Overflow Flag. Setting it high indicates math overflow error. Output datum is invalid.
D[1]	APOL	0b	R/W	Alert Polarity Bit. Setting it low indicates normal operation: active low output. Setting it high indicates inverted operation: active high output.
D[0]	LEN	0b	R/W	Alert Latch Enable Bit. Latch the ALERT pin and alert flag bits. 1 = Latch enabled 0 = Transparent (default) Setting it low indicates that the ALERT pin and flag bit is reset when the limit state is cleared. When it is set high, the ALERT pin is cleared by either I²C alert response or reading Mask/Enable register, however the AFF bit can only be cleared by reading Mask/Enable register.

REGISTER MAPS (continued)

07h: Alert Limit Register (Reset = 0000h)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	LIMIT[15:0]	0000h	R/W	The Alert Limit register is used to provide a limit threshold for the register selected by the Mask/Enable register to determine whether it exceeds or falls below the threshold. The limit value programmed in this register should be consistent with the format of the corresponding register.

3Eh: Manufacturer ID Register (Reset = 5449h)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:0]	MANUFACTURE_ID[15:0]	5449h	R	Manufacturer ID Bits. Store the manufacturer identification bits.

3Fh: Device ID Register (Reset = A480h)

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15:4]	DIEID[11:0]	A48h	R	Device ID Bits. Store the device identification bits.
D[3:0]	Reserved	0h	R	Reserved.

APPLICATION INFORMATION

The SGM843 is a 12-bit high-precision current, voltage, power monitor with alert function while being compatible with I²C and SMBus interface.

Device Measurement Range and Resolution

The current-sense amplifier features two programmable ranges for shunt voltage measurement, namely -81.92mV to 81.88mV (ADCRANGE = 0) and -20.48mV to 20.47mV (ADCRANGE = 1). Selection between these two ranges is achieved by configuring the ADCRANGE bit within the Configuration register (00h, D[12]), allowing adaptation to diverse current-sensing applications. Besides, built-in monitoring function includes bus voltage measurement over a span of 0V to 52.4V. However, due to the maximum rated voltage limitation of the process, the recommended operating voltage range of V_{BUS} is from 0V to 28V. Comprehensive details regarding measurement ranges and resolution steps are described in Table 2.

Table 2. ADC Full Scale Values

Parameter	Full Scale Value	Resolution
Shunt Voltage	-81.92mV to 81.88mV (ADCRANGE = 0)	40μV/LSB
	-20.48mV to 20.47mV (ADCRANGE = 1)	10μV/LSB
Bus Voltage	0V to 52.4V (Limit usable range to recommended operating voltage)	25.6mV/LSB

The SGM843 provides dedicated read-only 16-bit measurement registers: VSHUNT[11:0] in the Shunt Voltage register (01h) for shunt voltage, and VBUS[10:0] in the Bus Voltage register (02h) for bus voltage. The data in VSHUNT[11:0] may return positive or negative values indicating bidirectional current flow. Positive numbers are directly displayed in binary format, while negative numbers are displayed in two's complement format. Besides, the data in VBUS[10:0] is always positive and the bus voltage can be obtained by multiplying the result of the binary format conversion by resolution step of 25.6mV/LSB.

Current and Power Calculations

The SGM843 does not need to measure current and power directly, it realizes the calculation of current and power by measuring the differential voltage between IN+ and IN- pins and the voltage on IN- pin. Before reading the Current register (04h) and the Power register (03h), SHUNT_CAL[14:0] in Calibration register (05h) should be programmed first. The SHUNT_CAL[14:0] bits serve to provide a calibration coefficient, which facilitates the generation of precise current readings within the Current register. As shown in Equation 1, the value programmed into the SHUNT_CAL[14:0] bits for ADCRANGE = 0 is determined by both the Current_LSB parameter and the external shunt resistor applied in the system.

$$SHUNT\_CAL = \frac{0.08192}{Current\_LSB \times R_{SHUNT}} \quad (1)$$

Where:

0.08192 is an internal fixed constant employed to guarantee appropriate scaling throughout the measurement process.

Current_LSB is the user-defined current resolution step and the unit is A/LSB. Its value should be chosen from Current_LSB(MIN) to 8× Current_LSB(MIN) to reduce resolution loss, while Current_LSB(MIN) is shown in Equation 2.

R_{SHUNT} is the external shunt resistor applied in the system and the unit is Ω.

Note that if ADCRANGE is 1, the value of SHUNT_CAL should be divided by 4, which means the 0.08192 in the Equation 1 should be updated to 0.02048.

$$Current\_LSB(MIN) = \frac{Maximum\ Expected\ Current}{2^{11}} \quad (2)$$

Where:

Maximum Expected Current is the user-estimated maximum current according to the application used.

Besides, if the value in SHUNT_CAL[14:0] bits is zero, the values in the Current register (04h) and the Power register (03h) are also zero.

The device calculates current by applying the calibration coefficient from the Calibration register (05h) to the measured shunt voltage read from the Shunt Voltage register (01h). This calculated current value in Amperes can be obtained from the CURRENT[11:0] in the Current register (04h) and the Current_LSB parameter by using Equation 3:

$$Current\ (A) = Current\_LSB \times CURRENT \quad (3)$$

Where:

CURRENT is the decimal value read from the CURRENT[11:0] in the Current register (04h).

Current_LSB is the user-defined value in Equation1.

APPLICATION INFORMATION (continued)

Moreover, the system power is determined by multiplying the POWER register value by the Current_LSB, then multiplying the product by a fixed scaling factor of 32, which the unit is Watts, as defined by Equation 4:

$$\text{Power (W)} = 32 \times \text{Current\_LSB} \times \text{POWER} \quad (4)$$

Where:

POWER is the decimal value read from the POWER[15:0] in the Power register (03h).

Current_LSB is the user-defined value in Equation1.

ADC Output Data Rate and Noise Performance

The noise performance and effective resolution of the SGM843 are determined by the ADC conversion time and the averaging configuration settings. In practice, inherent trade-offs exist between conversion time and the number of averaging cycles employed. Averaging operations act as a filtering mechanism for the input signal, thereby contributing to a notable improvement in overall measurement accuracy. A higher number of averaging cycles enables more effective suppression of input noise. Similarly, conversion time exerts a direct influence on measurement precision, with extended conversion times yielding superior accuracy. Consequently, the optimal measurement accuracy can be achieved by adopting the maximum available conversion time combined with the highest number of averaging cycles, as long as the timing requirements by the overall system are satisfied.

Table 3 presents the typical effective number of bits (ENOB) for the SGM843 across various conversion time and averaging configurations, where ENOB is calculated from peak-to-peak noise measurements.

Table 3. Noise Performance

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (-81.92mV to 81.88mV) (ADCRANGE = 0)	Noise-Free ENOB (-20.48mV to 20.47mV) (ADCRANGE = 1)
265	1	0.265	9.2	7.1
620		0.62	10.4	8.5
1150		1.15	11	9
2150		2.15	12	9.7
4220		4.22	12	10
8400		8.4	12	10.4
265	4	1.06	10.4	8.2
620		2.48	12	9.7
1150		4.6	12	10
2150		8.6	12	11
4220		16.88	12	11
8400		33.6	12	12
265	16	4.24	12	9.4
620		9.92	12	11
1150		18.4	12	11
2150		34.4	12	11
4220		67.52	12	12
8400		134.4	12	12

APPLICATION INFORMATION (continued)

ADC Conversion Time Period (μs)	Output Sample Averaging (Samples)	Output Sample Period (ms)	Noise-Free ENOB (-81.92mV to 81.88mV) (ADCRANGE = 0)	Noise-Free ENOB (-20.48mV to 20.47mV) (ADCRANGE = 1)
265	64	16.96	12	10.4
620		39.68	12	12
1150		73.6	12	11
2150		137.6	12	12
4220		270.08	12	12
8400		537.6	12	12
265	128	33.92	12	11
620		79.36	12	12
1150		147.2	12	12
2150		275.2	12	12
4220		540.16	12	12
8400		1075.2	12	12
265	256	67.84	12	11
620		158.72	12	12
1150		294.4	12	12
2150		550.4	12	12
4220		1080.32	12	12
8400		2150.4	12	12
265	512	135.68	12	12
620		317.44	12	12
1150		588.8	12	12
2150		1100.8	12	12
4220		2160.64	12	12
8400		4300.8	12	12
265	1024	271.36	12	12
620		634.88	12	12
1150		1177.6	12	12
2150		2201.6	12	12
4220		4321.28	12	12
8400		8601.6	12	12

APPLICATION INFORMATION (continued)

Input Filtering Considerations

In practical applications, current measurement is inevitably affected by unwanted noise components. The SGM843 implements configurable noise suppression mechanisms through independent adjustment of conversion cycles and averaging times via the Configuration register (00h). While the conversion times for shunt voltage and bus voltage can be programmed separately, the averaging operations for both channels share the same configuration parameters.

The ADC of SGM843 is a sigma-delta (Σ-Δ) structure with typical sampling rates of 1MHz (±10%, MAX). The sigma-delta structure has good noise suppression capability. However, if there are transients at or near the sampling frequency (greater than 2MHz), it will affect the measurement accuracy which needs to be handled. By placing low-value resistors in series with a ceramic capacitor at the IN+ and IN- pins, these high-frequency signals can be effectively filtered. Figure 10 shows the filter setup, where the recommended resistor value is less than 100Ω and the recommended capacitor value is between 0.1μF and 1μF. Both resistor values should be consistent to avoid offset due to I_{BIAS}.

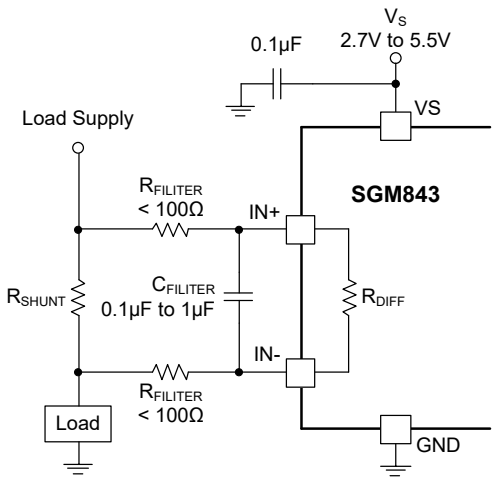


Figure 10. Input Filtering

In addition to transient disturbances, input overload conditions must also be properly considered and managed. The device inputs are capable of withstanding a differential voltage of up to ±26V. Under the load short-circuit condition, a large load current is generated, resulting in a rapid voltage rise across the shunt resistor. Once the short-circuit fault is cleared, parasitic inductance within the power loop may induce kickback voltages at the input terminals that potentially exceed the device's absolute voltage ratings. Such transient kickback voltages can be effectively suppressed through the application of Zener-type protection devices.

In certain applications, over-stress conditions can be triggered by excessive dV/dt transients arising from events such as hard short-circuit faults at the input. Such over-stress conditions arise from the actuation of internal ESD protection circuits under high current conditions. Experimental results demonstrate that the incorporation of 100Ω series resistors at the input terminals provides sufficient protection for the device against faults induced by high dV/dt events.

Typical Application

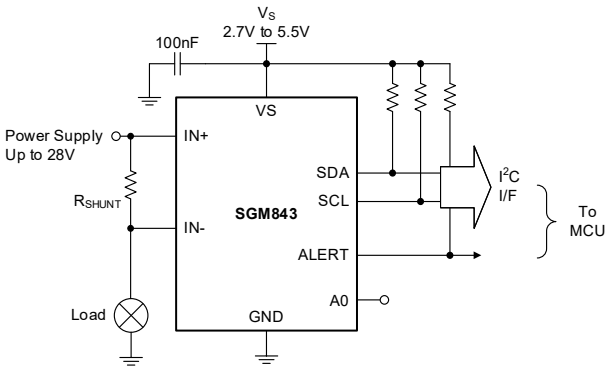


Figure 11. High-Side Sensing Application Diagram

Design Requirements

The SGM843 performs current sensing by the voltage drop across the shunt resistor between IN+ and IN-. The device is also capable of measuring the bus voltage at IN- pin and calculating the corresponding power by programming the Calibration register (05h). It has a programmable alert function, which can respond to user-defined fault or conversion completion events. In addition, users can also customize the specific threshold that triggers alert.

The design specifications and requirements associated with the SGM843 are summarized in Table 4.

APPLICATION INFORMATION (continued)

Table 4. Design Parameters

Design Parameter	SYMBOL	Example Value
Power Supply Voltage	V_S	3.3V
Bus Supply Rail	V_{CM}	12V
Average Current		12A
Over-Current Fault Threshold		18A
Maximum Current Monitored	I_{MAX}	20A
ADC Range Selection	V_{SENSE_MAX}	-81.92mV to 81.88mV

Select the Shunt Resistor

In accordance with the aforementioned design requirements, the ADC is configured to employ its full-scale input range of -81.92mV to 81.88mV (V_{SENSE_MAX}). The selection of the shunt resistor (R_{SHUNT}) requires a comprehensive consideration of both the maximum current monitored (I_{MAX}) and the maximum permissible shunt voltage (V_{SENSE_MAX}). Under full-load operating conditions, the voltage dropped across the shunt resistor must be maintained below the specified full-scale voltage V_{SENSE_MAX}. The maximum allowable value of R_{SHUNT} is derived via Equation 5, resulting in a calculated upper limit of 4.096mΩ. For practical implementation, a standard off-the-shelf resistance of 4mΩ is adopted as the shunt resistor.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (5)$$

Configure the Device

Upon each power-on cycle, the device initializes all registers to their default configurations. Consequently, proper configuration of these registers must be executed during the power-up initialization sequence. Under default operating conditions in Configuration register (Reset = 41B7h), the device automatically performs continuous conversions of the shunt voltage and bus voltage in accordance with the default settings. All registers can be further reprogrammed dynamically based on specific application requirements.

Program the Shunt Calibration Register

To achieve precise current measurement, the LSB for current (Current_LSB) is initially determined using Equation 2. With a maximum expected operating current of 20A, the corresponding Current_LSB is calculated to be 9.765625mA/LSB. As mentioned in Equation 1, Current_LSB should be chosen from Current_LSB(MIN) to 8 × Current_LSB(MIN) to reduce resolution loss. Therefore, 10mA/LSB for current is chosen in this application. Subsequently, SHUNT_CAL[14:0] in the Calibration register (05h) is programmed to a value of 2048d (800h), according to the calculated Current_LSB and the chosen shunt resistance (R_{SHUNT}). And the value in Calibration register (05h) is 2048d (800h), because the highest bit of the register is reserved 0. Remember that the Calibration register (05h) needs to be configured after the power-up initialization sequence, otherwise the current in the Current register (04h) and the power in the Power register (03h) cannot be read correctly.

Set Desired Fault Thresholds

The SGM843 can respond to any of the five selectable alert functions or a conversion ready signal. These alert functions include shunt voltage over-limit (SOL), shunt voltage under-limit (SUL), bus voltage over-limit (BOL), bus voltage under-limit (BUL) and power over-limit (POL). In this application, a SOL (Shunt Over-limit) fault event can be enabled by configuring the SOL bit within the Mask/Enable register (06h) to a logic high state. With the over-current fault threshold specified as 18A and the R_{SHUNT} resistance of 4mΩ, the maximum shunt voltage is calculated as 72mV. This threshold voltage determines the required setting for the Alert Limit register (07h). Based on the LSB of shunt voltage, the value for the desired fault threshold is calculated as: 72mV/40μV = 1800d (708h). Left shifting 4 bits to get the value for the Alert Limit register (07h) is 28800d (7080h). Remember that the Alert Limit register (07h) needs to be configured after the power-up initialization sequence when using ALERT function.

Calculate Returned Values

To obtain the actual parameter value, multiply the register reading from 01h to 04h by its corresponding LSB. Table 5 provides the register return values in decimal format. Prior to being multiplied by the corresponding LSB value, the output codes for shunt voltage (01h), current (04h), and bus voltage (02h) must be right-shifted by 4 bits to recover the valid 12-bit measurement result because the four least significant bits in the raw output data are reserved and fixed at logic 0.

Besides, bus voltage in Bus Voltage (02h) is positive values only and power are represented in an unsigned value with 16 bits.

APPLICATION INFORMATION (continued)

Table 5. Calculate Returned Values

Register Name	Contents	Right Shifted 12-bit Value	LSB Value	Calculated Value
Configuration (00h)	16823d (41B7h)	—	—	—
Calibration (05h)	2048d (800h)	—	—	—
Mask/Enable (06h)	32768d (8000h)	—	—	—
Alert Limit (07h)	28800d (7080h)	1800d (708h)	40μV/LSB	1800 × 40μV = 0.072V
Shunt Voltage (01h)	19200d (4B00h)	1200d (4B0h)	40μV/LSB	1200 × 40μV = 0.048V
Bus Voltage (02h)	7504d (1D50h)	469d (1D5h)	25.6mV/LSB	469 × 25.6mV = 12.0064V
Current (04h)	19200d (4B00h)	1200d (4B0h)	10mA/LSB	1200 × 10mA = 12A
Power (03h)	450d (1C2h)	—	Current LSB × 32 = 320mW/LSB	450 × 320mW =144W

Application Curves

Figure 12 demonstrates the response of the ALERT pin during a shunt over-voltage fault of 72mV when configured with a conversion time of 265μs and averaging setting of 1. Figure 13 demonstrates the response for the same limit but with a conversion time of 1.15ms. To visualize the ALERT pin response time under different conditions, the oscilloscope is set to the persistence mode. Figure 12 and Figure 13 show how the ALERT response time varies depending on when the fault condition occurs relative to the internal ADC clock of the SGM843. For fault conditions that are just exceeding the limit threshold, the response time for the ALERT pin can vary from one to two conversion cycles. This variation primarily results from the relative timing between fault occurrence and ADC sampling instants. It is worth noting that the alert response time has no correlation with the average count because the alert function assesses whether each individual conversion result meets the predefined alert threshold. When the fault conditions exceed the threshold significantly, the alert can respond in less than one conversion cycle.

Since the relationship between alert limit threshold event and ADC conversion is not simple to predict, so that the critical value for the alert response time in shunt or bus voltage only measurement mode should be 2 times of the conversion time when considering the margin.

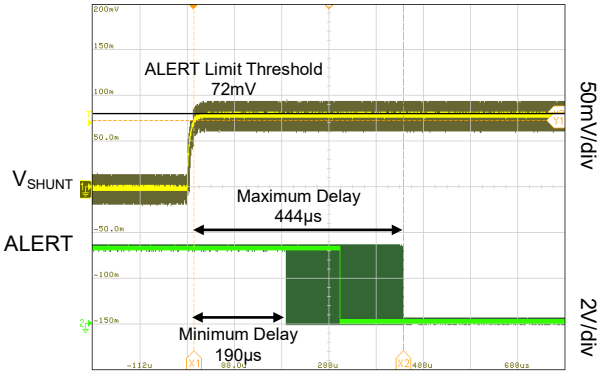


Figure 12. Alert Response Time (t_{CT} = 265μs)

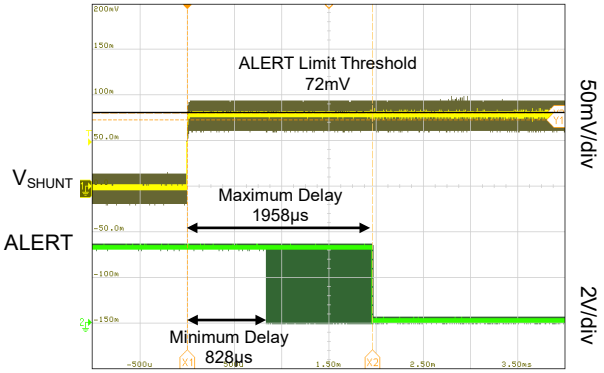


Figure 13. Alert Response Time (t_{CT} = 1.15ms)

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The device is capable of accurately measuring common-mode voltages imposed on the power supply terminals, which may exceed its own supply voltage, V_S. For instance, while the device operates from a 5V supply, the monitored load voltage can reach as high as 28V. The input terminals can sustain a voltage range from 0V to 28V regardless of whether the device is powered or in a shutdown state.

To maintain stable power supply performance, bypass capacitors should be positioned as close as possible to the device's input and GND pins. A 0.1μF bypass capacitor is typically recommended. For applications involving noisy or high-impedance power supplies, additional decoupling capacitors are required to further suppress power supply noise.

Layout

Layout Guidelines

To achieve high-precision current sensing, a Kelvin connection or 4-wire configuration is strongly recommended between the input pins (IN+ and IN-) and the shunt resistor. These connection schemes effectively eliminate the introduction of parasitic impedance across the input terminals. Given the extremely low resistance value of the shunt resistor, any extra series impedance associated with high-current carrying paths would result in considerable measurement errors. Besides, the power-supply bypass capacitor should be placed as close as possible to the power supply and ground pins of the device to optimize noise rejection and supply stability

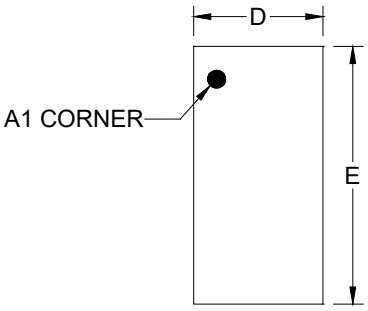
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

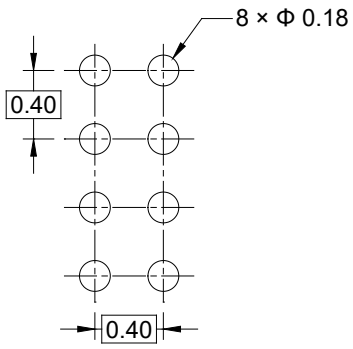
Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

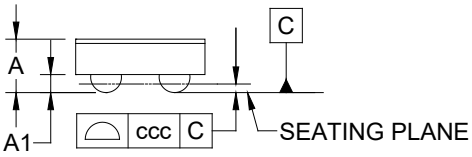
WLCSP-0.75×1.5-8B



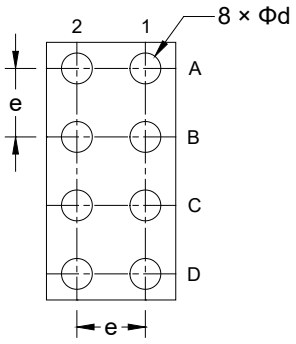
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



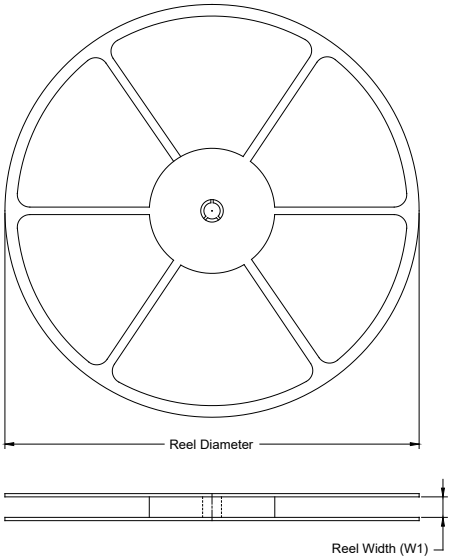
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.350
A1	0.085	-	0.125
D	0.720	-	0.780
E	1.470	-	1.530
d	0.150	-	0.210
e	0.400 BSC		
ccc	0.050		

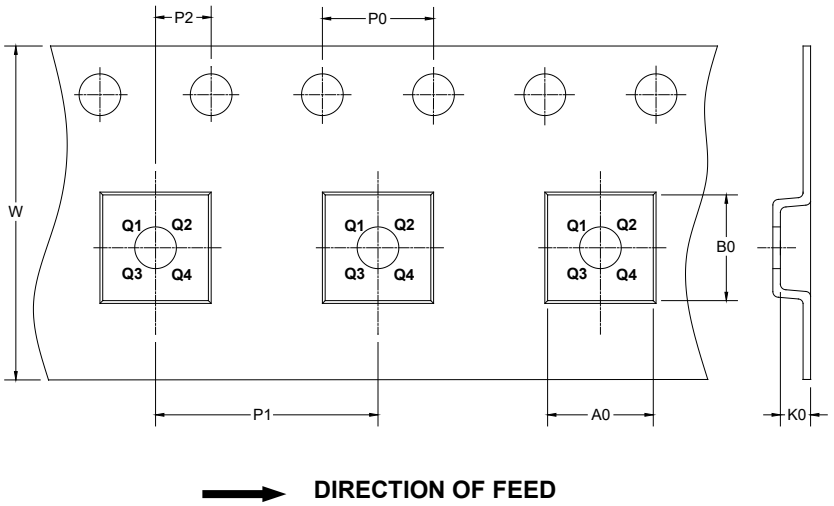
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



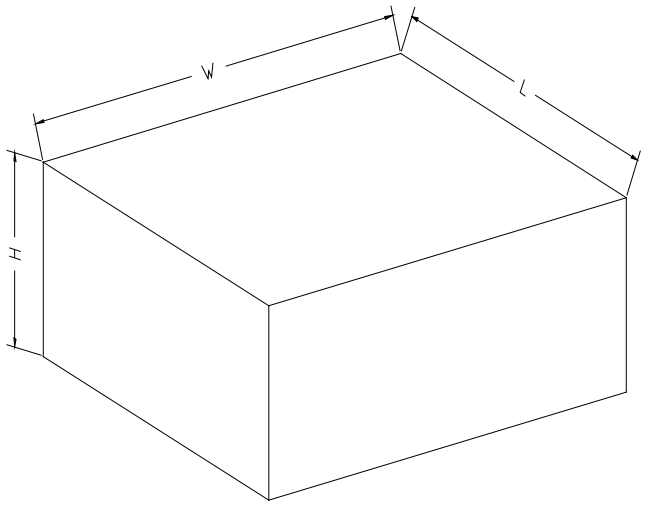
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.75×1.5-8B	7"	9.5	0.84	1.62	0.43	4.0	2.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002