SGM41562S
800mA Single-Cell Li-Ion Battery Charger with Power Path Management

GENERAL DESCRIPTION

The SGM41562S is a highly integrated, I^{2}C programmable, single-cell Li-Ion or Li-polymer battery charger with system power path management. It is specifically designed for portable applications requiring minimum board space and small external components. The charging profile includes pre-charge, constant-current and constant-voltage phases. Several safety and protection features are included, such as built-in safe charge timer to set maximum duration of charge and pre-charge, input voltage and current monitoring, internal (junction) and external (battery) temperature monitoring, input current limiting and load current limiting. The SGM41562S can charge with a wide input voltage range of up to 19V.

The SGM41562S has 3 power ports: input power port (IN), battery port (BAT) and system or load port (SYS). The system is powered from the input whenever it is available. Input is typically a USB power source. If the input source is weak or removed, power source for the system will automatically switch to the battery. The voltage and currents from input and battery as power sources are continuously monitored to prevent battery damage due to excessive currents or over-discharge.

The I^{2}C serial interface is used to program the device functions and parameters or to read its status. 12 read/write or read only 8-bit registers (REG0x00 to REG0x0B) are accessible. A watchdog protection feature is also included. If this feature is enabled and there is no read/write activity or signal from the host in time, the device will reset the charging parameters to their defaults and recycles power to the system (turn off/on) that may reset the host.

The SGM41562S is capable of charging with input voltages as high as 19V but with higher input voltages, the chip temperature can easily rise up and thermal protection may stop charging if proper cooling is not considered. The SGM41562S goes into voltage protection state if V_{IN} > 6V. The input changes are continuously monitored and a system power recycle (SYS) may occur if the system does not respond to the input toggles.

The SGM41562S is available in a Green WLCSP-1.55×1.57-9B package. Device functionality and protection features are assured in the ambient temperature range from -40℃ to +125℃. Charging parameters are guaranteed in 0℃ to +55℃.

FEATURES

- **Fully Autonomous Charger for Single-Cell Li-Ion and Li-Polymer Battery**
- **±0.5% Charging Voltage Accuracy**
- **21V Maximum Input Voltage Rating with Over-Voltage Protection**
- **19V Maximum Operating Voltage**
- **6V Maximum Operating Voltage**
- **I^{2}C Interface for Parameters Setting/Status Reporting**
- **Fully Integrated Power Switches**
- **No External Blocking Diode Required**
- **Built-in Robust Charge Protections Including Battery Temperature Monitor and Programmable Timer**
- **Battery or PCB Over-Temperature Protection**
- **Built-in Battery Disconnection Function**
- **System Reset Function**
- **Thermal Limit Regulation on Chip**
- **Available in a Green WLCSP-1.55×1.57-9B Package**

APPLICATIONS

Wearable Devices
IoT Gadgets

SIMPLIFIED SCHEMATIC

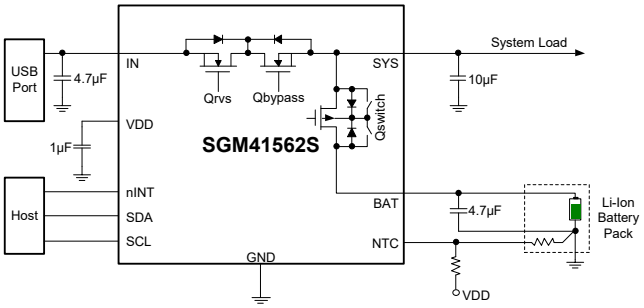


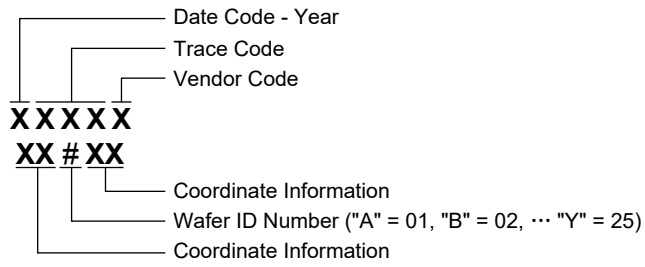
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41562S	WLCSP-1.55×1.57-9B	-40℃ to +125℃	SGM41562SXG/TR	1PH XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN ..... -5V to 21V
SYS ..... -0.3V to 5.3V (5.5V for 500μs)
All Other Pins to GND ..... -0.3V to 6V
$I_{INCLAMP}$ 5mA
Package Thermal Resistance
WLCSP-1.55×1.57-9B, θ_{JA} ..... 94.4℃/W
WLCSP-1.55×1.57-9B, θ_{JB} ..... 15.6℃/W
WLCSP-1.55×1.57-9B, θ_{JC} ..... 27℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 4.35V to 19V (Charging)
..... 4.35V to 5.5V (Charging)
(Over-Voltage Protection State, Continuous) 19V
I_{IN} ..... Up to 800mA
I_{BAT} ..... Up to 3.2A
I_{CHG} ..... Up to 800mA
V_{BAT_REG} ..... 3.5V to 4.77V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

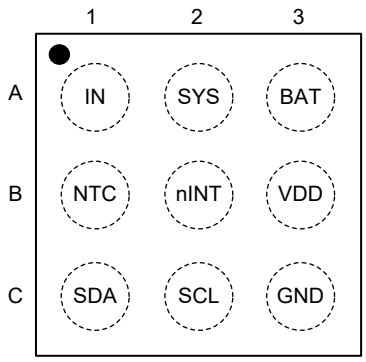
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.55×1.57-9B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	IN	P	Input Power Pin. Place a minimum 2.2μF ceramic capacitor between IN pin and GND pin as close as possible to these pins.
A2	SYS	P	System Power Supply Output. Place a ceramic capacitor between SYS pin and GND pin as close as possible to these pins.
A3	BAT	P	Battery Positive Terminal Connection Pin. Place a ceramic capacitor between BAT pin and GND pin as close as possible to the device. Connect the negative battery terminal to power GND.
B1	NTC	AIO	Battery Temperature Sense Input. Connect a negative temperature coefficient thermistor between this pin and GND pin. NTC is usually placed in touch with battery pack. Hot-cold temperature window can be programmed by a resistor divider network placed between VDD to NTC to GND pins. Charging will suspend if NTC function is enabled and NTC pin voltage goes out of the V_{HOT} and V_{COLD} range.
B2	nINT	DIO	Interrupt Output Pin. This pin can send a charging status and fault interrupt signal to the host. It also has the effect of disconnecting the system from the battery. Pull nINT pin from high to low for > t_{RST_DGL} (16s default). Regardless of the nINT status, The battery FET automatically turns off and turns on again after > t_{RST_DUR} (4s default). Both t_{RST_DGL} and t_{RST_DUR} can be programmed via the I^2C interface. The nINT pin can only be pulled up to BAT.
B3	VDD	P	Internal Power Supply Pin. Connect a minimum 0.1μF decoupling ceramic capacitor from VDD pin to GND. External load current on this pin should not exceed 1mA.
C1	SDA	DIO	I^2C Bus Data. A 10kΩ pull-up to the logic-high rail should be used on SDA line.
C2	SCL	DI	I^2C Bus Clock. A 10kΩ pull-up to the logic-high rail should be used on SCL line.
C3	GND	P	Ground Pin of the Device.

NOTE: AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{IN} = 5V and V_{BAT} = 3.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Source and Battery Protection						
Input Under-Voltage Lockout Threshold	V_{IN_UVLO}	Input falling	3.2	3.6	4	V
V_{IN_UVLO} Threshold Hysteresis	$V_{IN\_UVLO\_HYS}$	Input rising		105		mV
Input Over-Voltage Protection Threshold	V_{IN_OVLO}	Input rising threshold	18.5	19	19.5	V
			5.9	6	6.15	
V_{IN_OVLO} Threshold Hysteresis	$V_{IN\_OVLO\_HYS}$			325		mV
Input vs. Battery Voltage Headroom Threshold	V_{HDRM}	Input rising vs. battery		110		mV
V_{HDRM} Threshold Hysteresis	V_{HDRM_HYS}	Input vs. battery voltage headroom threshold hysteresis		55		mV
BAT Pin Input Voltage	V_{BAT}				4.77	V
Input Power Detection Time	t_{PWD}	Wait time before sending interrupt pulse for reporting input power new status		70		ms
nINT Output Pulse Duration	t_{INT_PULSE}			250		μs
Battery Under-Voltage Lockout Threshold	V_{BAT_UVLO}	V_{BAT} falling, VBAT_UVLO[2:0] = 000	2.2	2.40	2.6	V
		V_{BAT} falling, VBAT_UVLO[2:0] = 100	2.53	2.76	2.95	
		V_{BAT} falling, VBAT_UVLO[2:0] = 111	2.78	3.00	3.22	
Battery Under-Voltage Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$	V_{BAT_UVLO} = 2.76V		180		mV
Battery Over-Voltage Protection Threshold	V_{BAT_OVP}	Rising, higher than V_{BAT_REG}		100		mV
Power Path Management						
Regulated System Output Voltage Accuracy	$V_{SYS\_REG\_ACC}$	V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{CHG} = 0A, VSYS_REG[4:0] = 0 1100, V_{SYS_REG} = 4.2V	4.18	4.20	4.22	V
		V_{IN} = 5.5V, R_{SYS} = 100Ω, I_{CHG} = 0A, VSYS_REG[4:0] = 1 0101, V_{SYS_REG} = 4.65V	4.63	4.65	4.67	
Input Current Limit	I_{IN_LIM}	IIN_LIM[4:0] = 0 0000, I_{IN_LIM} = 50mA	30	47	65	mA
		IIN_LIM[4:0] = 0 0010, I_{IN_LIM} = 110mA	70	105	130	
		IIN_LIM[4:0] = 0 1000, I_{IN_LIM} = 290mA	240	270	300	
		IIN_LIM[4:0] = 0 1111, I_{IN_LIM} = 500mA	440	470	500	
		IIN_LIM[4:0] = 1 1001, I_{IN_LIM} = 800mA	690	750	810	
Input Minimum Voltage Regulation	V_{IN_MIN}	VIN_MIN[3:0] = 0000, V_{IN_MIN} = 3.88V	3.84	3.88	3.91	V
		VIN_MIN[3:0] = 1001, V_{IN_MIN} = 4.60V	4.57	4.60	4.63	
		VIN_MIN[3:0] = 1111, V_{IN_MIN} = 5.08V	5.05	5.08	5.12	
IN to SYS Switch On-Resistance	R_{ON_Q1}	V_{IN} = 4.5V, I_{SYS} = 100mA		155		mΩ
Input Quiescent Current	I_{IN_Q}	V_{IN} = 5.5V, EN_HIZ = 0, CEB = 0, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		0.85	1.1	mA
		V_{IN} = 5.5V, EN_HIZ = 0, CEB = 1, charge disabled		0.85	1.1	
Input Suspend Current	I_{IN_SUSP}	V_{IN} = 5.5V, EN_HIZ = 1, CEB = 0, charge enable		11	16	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_{IN} = 5V and V_{BAT} = 3.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Quiescent Current	I_{BAT_Q}	V_{IN} = 5V, CEB = 0, I_{SYS} = 0A, V_{BAT} = 4.3V, charge complete		14	18	μA
		V_{IN} = 0, CEB = 1, VDD_DIS = 1, FET_DIS = 0, I_{SYS} = 0A, V_{BAT} = 4.35V, disable external NTC circuit driving		7	11	
		V_{IN} = 0, CEB = 1, I_{SYS} = 0A, V_{BAT} = 4.35V, enable PCB OTP function, excluding the external NTC bias		9	13	
		V_{IN} = 0, CEB = 1, I_{SYS} = 0A, V_{BAT} = 4.35V, enable PCB OTP function and watchdog, excluding the NTC bias		9	13	
		V_{BAT} = 4.5V, no input, shipping mode, nINT pulled up to V_{BAT}, VDD_DIS = 1, EN_NTC = 0		0.35	0.6	
Battery FET On-Resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BAT} = 3.5V, I_{SYS} = 100mA		70		mΩ
Battery FET Discharge Current Limit (Refer to Histogram)	I_{DSCHG}	IDSCHG[3:0] = 0001, I_{DSCHG} = 400mA		400		mA
		IDSCHG[3:0] = 1001, I_{DSCHG} = 2000mA		2000		
Delay before Discharge Over-Current Cut	t_{DSCHG_CUT}	Delay after discharge OC detection and before turning switch off		64		μs
Delay before Retry after Cut	t_{RETRY}	Turn on retry delay after OC turn off		800		μs
Ideal Diode Forward Voltage in Supplement Mode (BAT to SYS)	V_{FWD}	50mA discharge current		38		mV
Shipping Mode						
Enter to Shipping Mode Deglitch Delay Time after Programming the Shipping Mode	t_{SMEN_DGL}	FET_DIS bit is set from 0 to 1, EN_SHIP_DGL[1:0] = 00		1		s
Exit Shipping Mode Delay (Initiated by nINT Pin or V_{IN} Plug-In)	t_{SMEX_DGL}	nINT pin is pulled low, REG0x00[2:1] = 00		2		s
		nINT pin is pulled low, REG0x00[2:1] = 11		100		ms
Auto-Reset Mode						
Reset and Power Recycle by nINT Pin is Pull Down	t_{RST_DGL}	tRST_DGL[1:0] = 00		8		s
		tRST_DGL[1:0] = 10		16		
Battery FET Off-Time Duration after Reset	t_{RST_DUR}	tRST_DUR = 0		2		s
		tRST_DUR = 1		4		
Battery Charger						
Battery Charge Regulation Voltage	V_{BAT_REG}	VBAT_REG[6:0] = 000 1010, V_{BAT_REG} = 3.6V	3.58	3.60	3.62	V
		VBAT_REG[6:0] = 100 0110, V_{BAT_REG} = 4.2V	4.18	4.20	4.22	
		VBAT_REG[6:0] = 101 1000, V_{BAT_REG} = 4.38V	4.36	4.38	4.4	
		VBAT_REG[6:0] = 110 1000, V_{BAT_REG} = 4.54V	4.52	4.54	4.56	
Charge Current	I_{CC}	ICC[6:0] = 000 0000, I_{CC} = 8mA	6.5	8	9.5	mA
		ICC[6:0] = 000 1011, I_{CC} = 96mA	86	96	106	
		ICC[6:0] = 010 0000, I_{CC} = 264mA	251	264	277	
		ICC[6:0] = 011 1000, I_{CC} = 456mA	440	456	470	
		ICC[6:0] = 110 0011, I_{CC} = 800mA	760	800	840	
Junction Temperature Regulation	T_{J_REG}	I^2C programmable range	60		120	℃
		TJ_REG[1:0] = 11, T_{J_REG} = 120℃		120		
Pre-Charge Current	I_{PRE}	ITERM[3:0] = 0101, I_{TERM} = I_{PRE} = 11mA		11		mA
		ITERM[3:0] = 1111, I_{TERM} = I_{PRE} = 31mA		31		

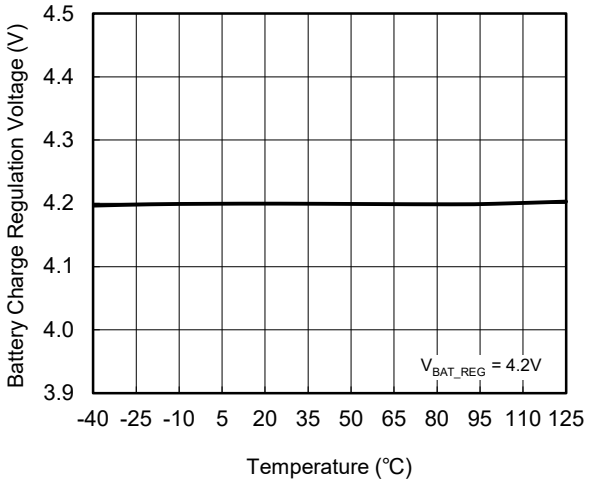
ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_{IN} = 5V and V_{BAT} = 3.5V, unless otherwise noted.)

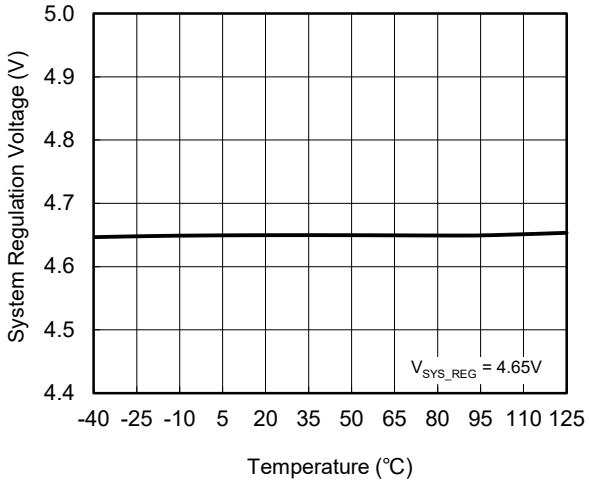
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Termination Current Threshold	I_{TERM}	ITERM[3:0] = 0000, I_{TERM} = 1mA	0.5	1	1.6	mA
		ITERM[3:0] = 0001, I_{TERM} = 3mA	2	3	4	
		ITERM[3:0] = 0101, I_{TERM} = 11mA	9	11	13	
		ITERM[3:0] = 1111, I_{TERM} = 31mA	26	31	38	
Termination Deglitch Time	t_{TERM_DGL}	ITERM_TIMER = 0		200		ms
		ITERM_TIMER = 1		40		
Pre-Charge to Fast Charge Threshold	V_{BAT_PRE}	V_{BAT} rising, VBAT_PRE = 1, V_{BAT_PRE} = 3V	2.9	3	3.1	V
Pre-Charge to Fast Charge Threshold Hysteresis	$V_{BAT\_PRE\_HYS}$			90		mV
Battery Auto-Recharge Voltage Drop Threshold	V_{RECH}	Below V_{BAT_REG}, VRECH = 0		100		mV
		Below V_{BAT_REG}, VRECH = 1		200		
Battery Auto-Recharge Deglitch Time	t_{RECH_DGL}			200		ms
Thermal Protection						
Thermal Shutdown Threshold	T_{J_SHDN}			150		℃
Thermal Shutdown Hysteresis				20		℃
NTC Pin Output Current	I_{NTC}	CEB = 0, V_{NTC} = 3V	-200		200	nA
NTC Cold Temperature Rising Threshold	V_{COLD}	As percentage of V_{DD}	63	65	67	%
NTC Cold Temperature Rising Threshold Hysteresis				0.7		%
NTC Hot Temperature Falling Threshold	V_{HOT}	As percentage of V_{DD}	31	33	35	%
NTC Hot Temperature Falling Threshold Hysteresis				1.5		%
NTC Hot Temperature Falling Threshold for PCB OTP	V_{HOT_PCB}	As percentage of V_{DD}	30	32	34	%
NTC Hot Temperature Falling Threshold Hysteresis for PCB OTP				1.7		%
Logic IO Pin Characteristics						
Low Logic Voltage Threshold	V_L				0.4	V
High Logic Voltage Threshold	V_H		0.9			V
I^2C Interface (SDA, SCL)						
Input Low Logic Voltage Threshold	V_{IL}				0.4	V
Input High Logic Voltage Threshold	V_{IH}		0.9			V
Output Low Threshold Level	V_{OL}	I_{SINK} = 5mA			0.2	V
I^2C Clock Frequency	f_{SCL}				1	MHz
Clock Frequency and Watchdog Timer						
Watchdog Timer	t_{WDT}	WATCHDOG[1:0] = 11		256		s

TYPICAL PERFORMANCE CHARACTERISTICS

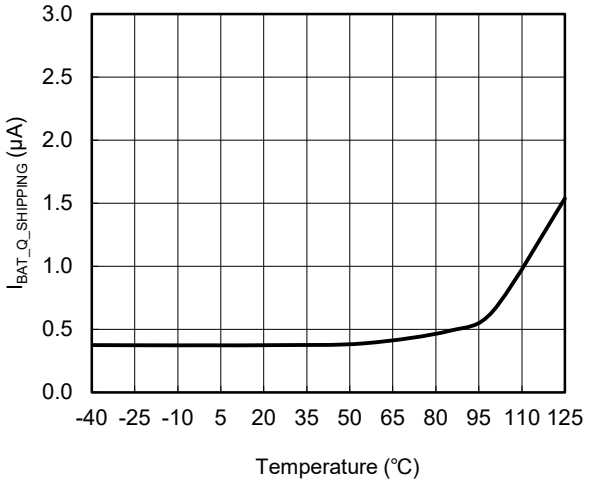
Battery Charge Regulation Voltage vs. Temperature



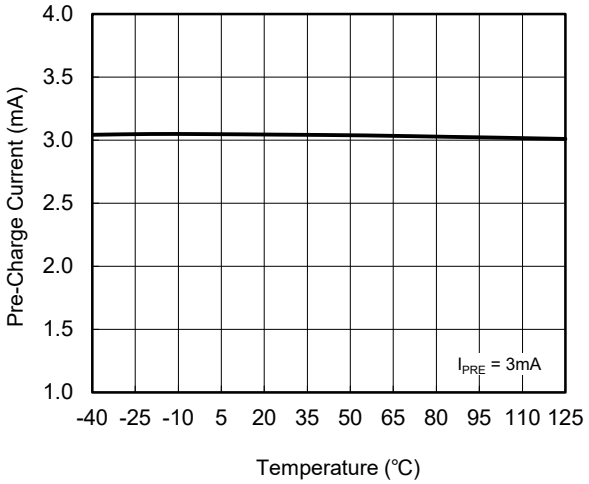
System Regulation Voltage vs. Temperature



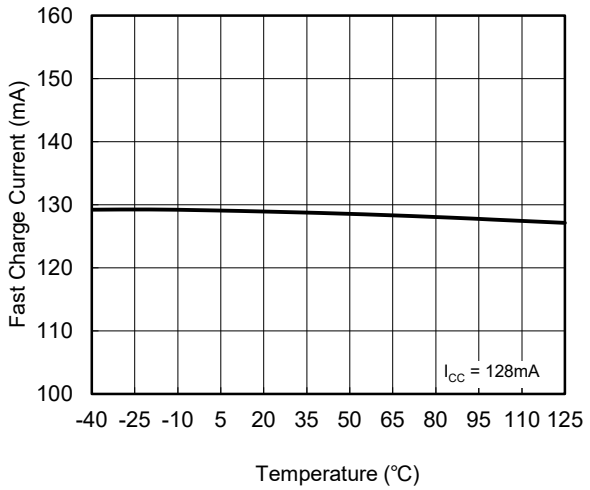
Battery Current under Shipping Mode vs. Temperature



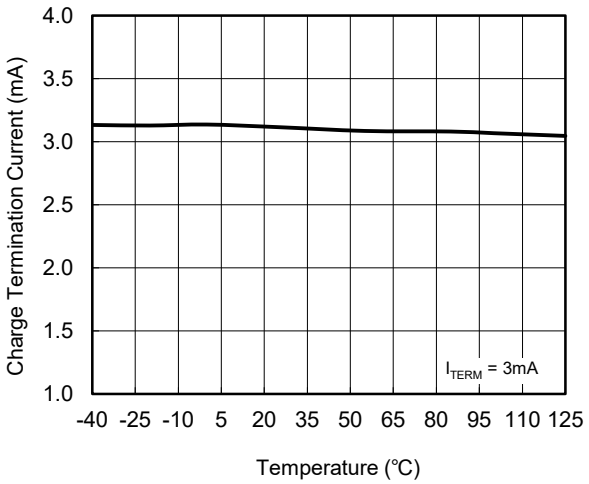
Pre-Charge Current vs. Temperature



Fast Charge Current vs. Temperature

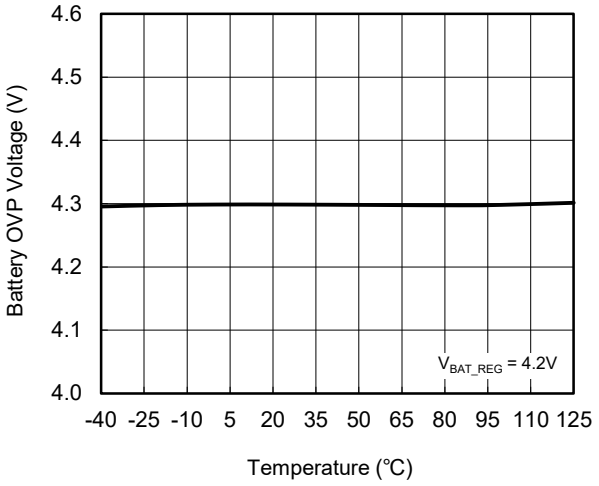


Charge Termination Current vs. Temperature

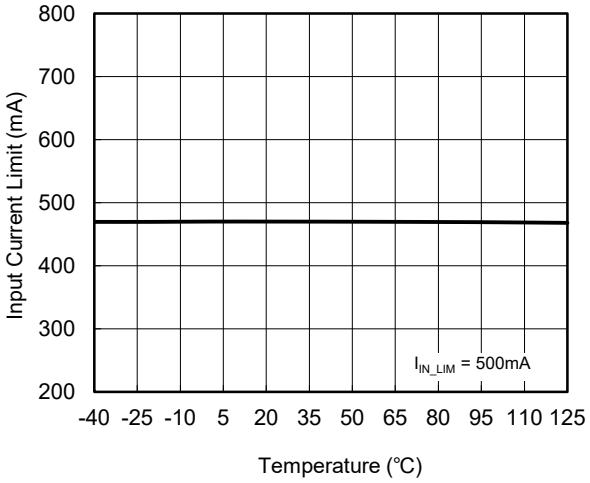


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

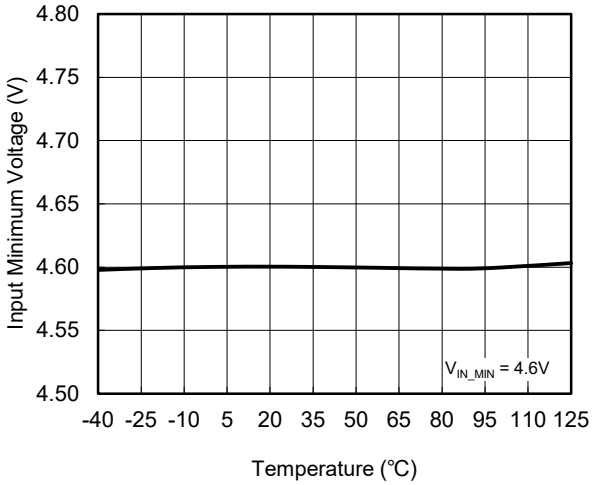
Battery OVP Voltage vs. Temperature



Input Current Limit vs. Temperature



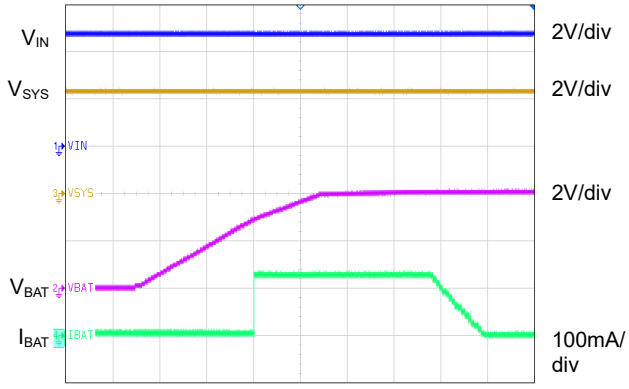
Input Minimum Voltage vs. Temperature



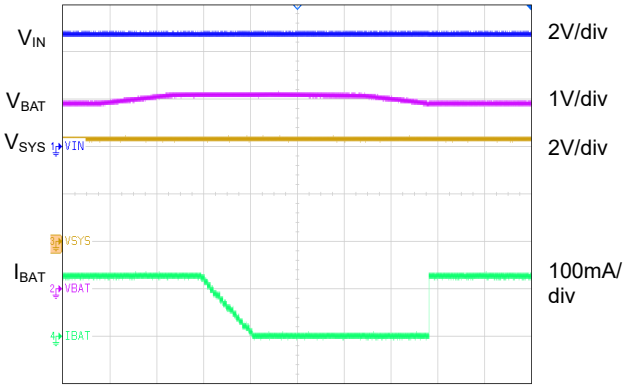
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, I_{IN} = 500mA, I_{CC} = 128mA and V_{IN_MIN} = 4.6V, unless otherwise noted.

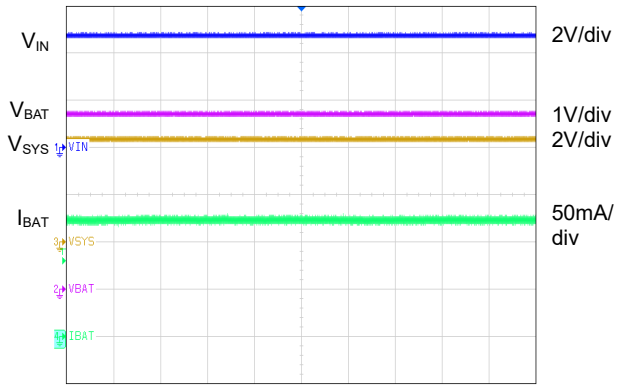
Battery Charge Curve



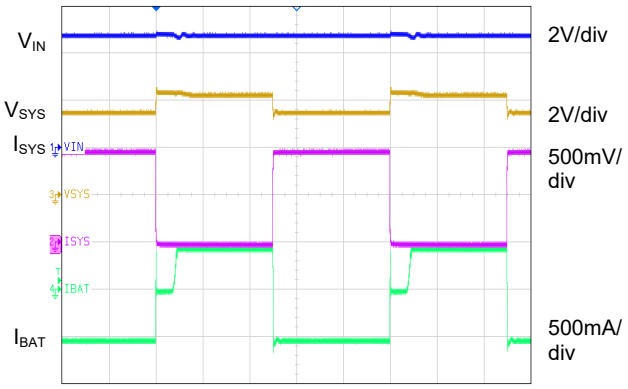
Auto-Recharge Curve



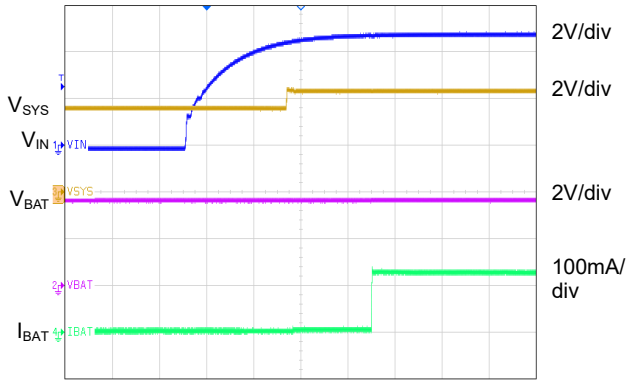
CC Charge Steady State



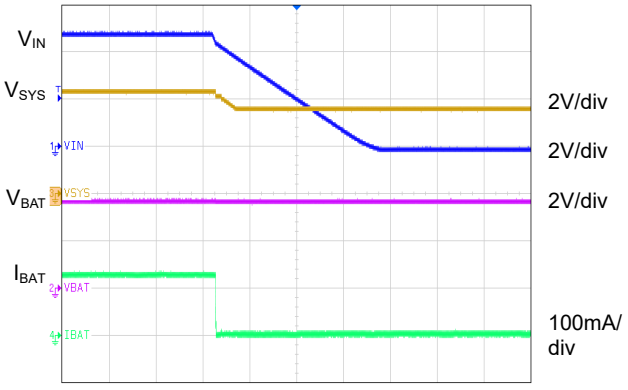
SYS Load Transient



Power-On



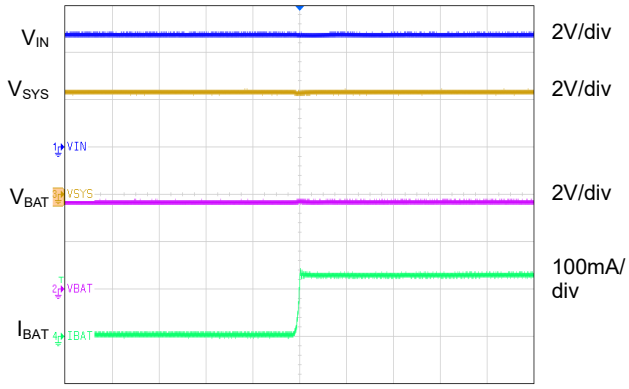
Power-Off



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

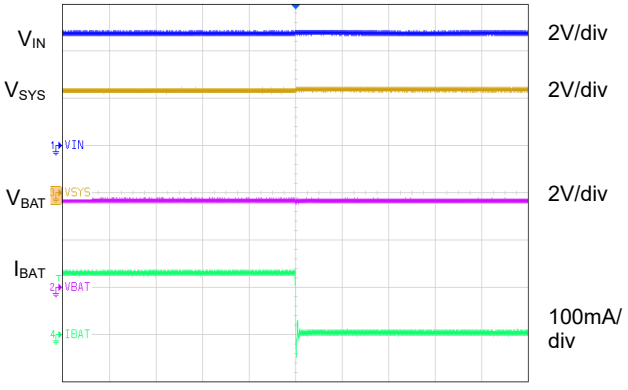
T_A = +25℃, V_{IN} = 5V, I_{IN} = 500mA, I_{CC} = 128mA and V_{IN_MIN} = 4.6V, unless otherwise noted.

Charge Enable



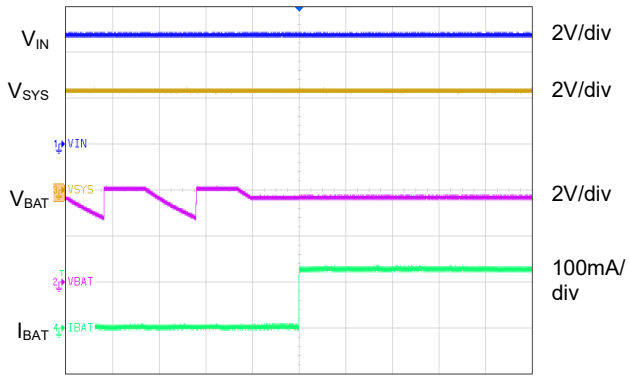
Time (200μs/div)

Charge Disable



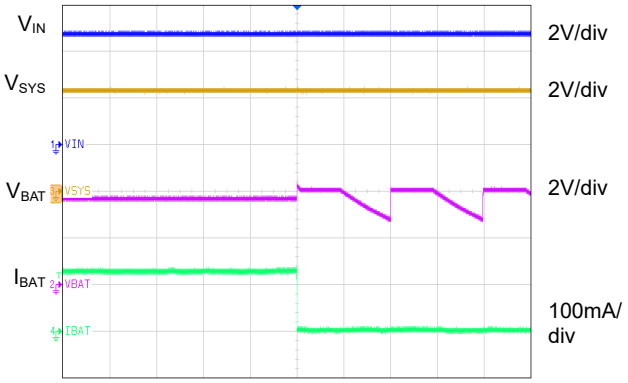
Time (200μs/div)

Battery Insertion



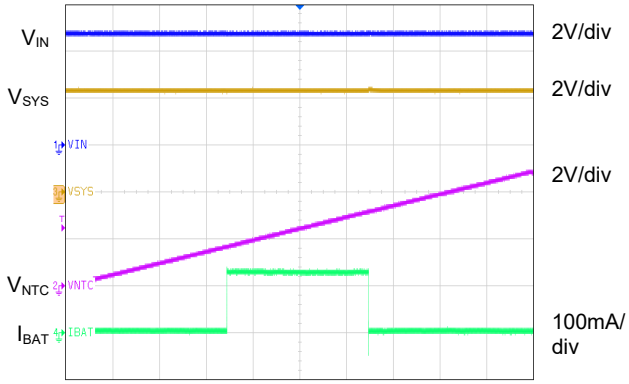
Time (200ms/div)

Battery Removal



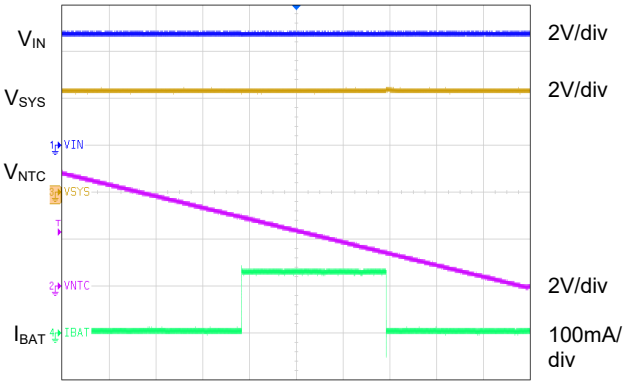
Time (200ms/div)

NTC Rising



Time (20ms/div)

NTC Falling

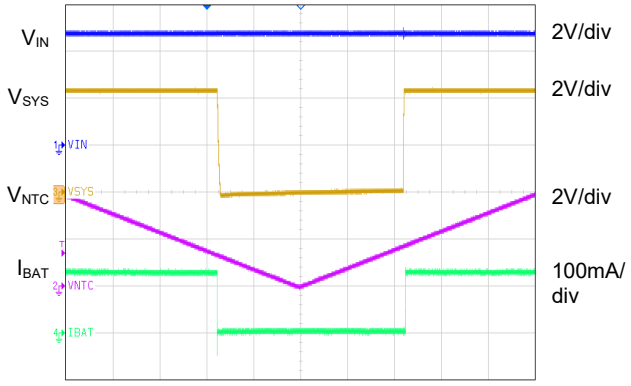


Time (20ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

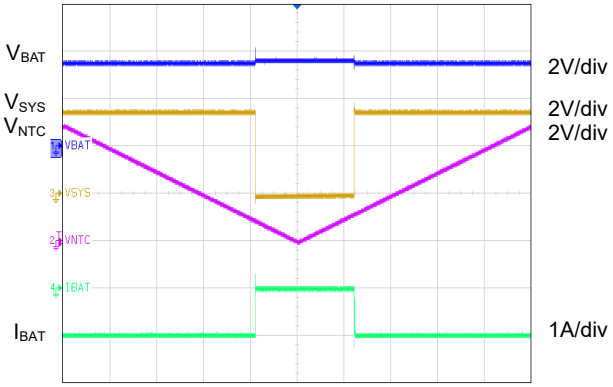
T_A = +25℃, V_{IN} = 5V, I_{IN} = 500mA, I_{CC} = 128mA and V_{IN_MIN} = 4.6V, unless otherwise noted.

PCB_OTP at Charge Mode



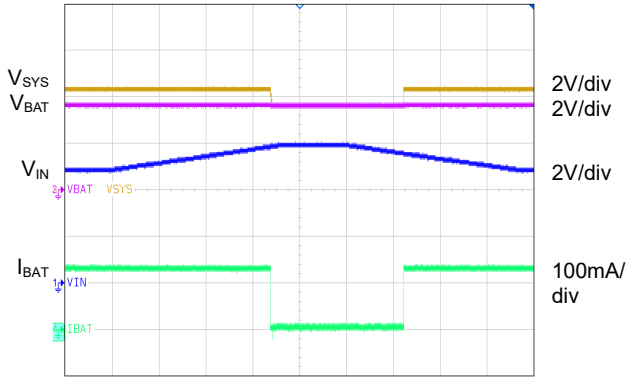
Time (20ms/div)

PCB_OTP at Discharge Mode



Time (50ms/div)

V_{IN} OVP Operation



Time (2s/div)

FUNCTIONAL BLOCK DIAGRAM

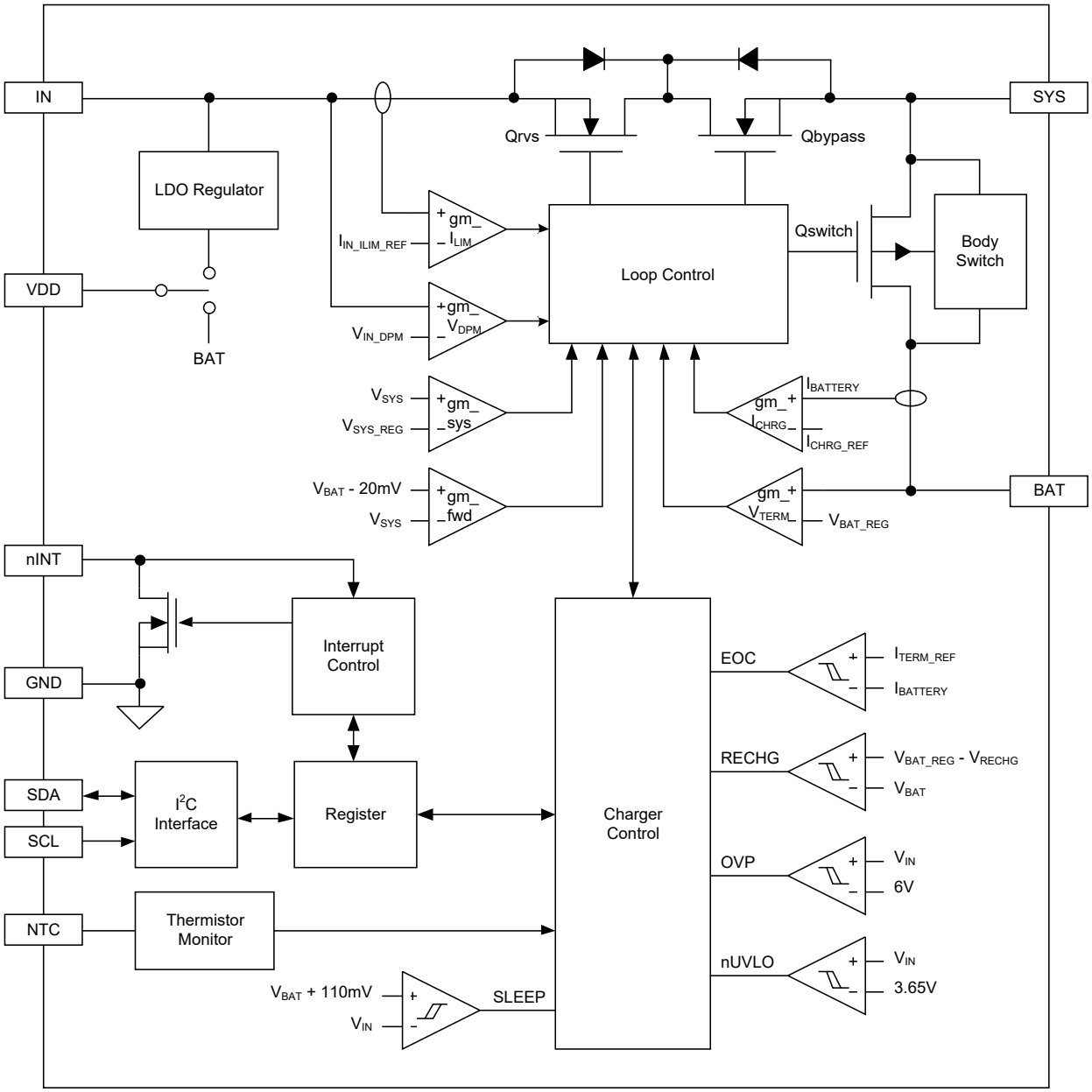


Figure 2. Block Diagram

DETAILED DESCRIPTION

Introduction

The SGM41562S is a single-cell battery charger with power path management function for Li-Ion and Li-polymer batteries. The charge features include pre-charge, fast charge including constant-current mode (CCM) and constant-voltage mode (CVM), end-of-charge termination, auto-recharge, and a built-in safe charge timer. The safe charge timer is used to prevent over-charging or other issues if the host runs out of control.

A bypass switch between IN and SYS pins, and a battery switch between SYS and BAT pins are integrated to provide complete power path management (PPM). The switches have low on-resistances to minimize loss and heat. System load is primarily powered from the input when it is available, and the remaining input power is used to charge the battery if needed. When the input source is weak, the load is powered partially from the battery. This mode in which the battery provides the power deficit is called supplement mode. Battery will provide the full load power if input is removed or if V_{IN} is out of range. For battery charging, the power to the battery is regulated by the battery switch. To prevent faulty charge conditions, input voltage, input current, system voltage, chip temperature and external temperature (sensed by NTC) are continuously monitored during charge.

Figure 3 shows the power paths and key internal blocks of the device. The Qbypass switch regulates the voltage of the system and the internal charge circuit. The Qrvs switch acts as a near ideal blocking diode to prevent reverse power (or leakage) from the load (SYS pin) back to the input (IN pin). The Qswitch switch is responsible for battery charging regulation and connecting or disconnecting the battery (BAT pin) to the system (SYS pin). The charge and discharge circuits in the Figure 3 that are connected to the IN and BAT pins have their own independent UVLO and power supply. The rest of the chip is powered by either IN or BAT pin, whichever has the higher voltage. The I/F interface (I^2C communication and nINT) block is active whenever any of the power sources (IN or BAT pin) are available.

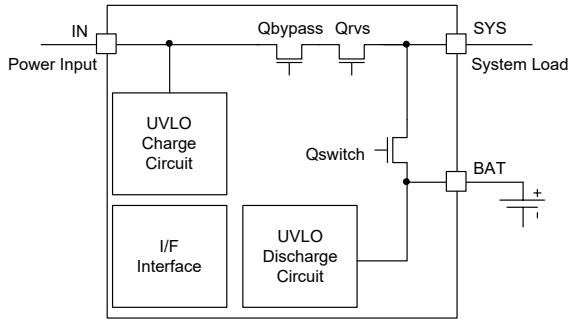


Figure 3. Power Path Management Structure

The chip has a watchdog timer as a protective feature against unexpected host malfunctions. When watchdog timer is enabled, it must be reset by host regularly to prevent watchdog timer overflow that results in a chip reset and power recycle. Watchdog reset is by writing into the watchdog register through I^2C interface (I/F). If the watchdog is not reset on time, the power to the host will recycle.

The power fed to the SYS pin is recycled when watchdog times out, the host does not respond to IN power input (when watchdog is forced on) or COLD_RESET bit is set to 1, to clear the running environment before system program upgrade or release from locked situations.

Input Detection

Figure 4 shows how the input voltage status is detected and affects the device function along with the relevant timings and nINT output signal updates. The device continuously monitors the input voltage at the IN node. The SYS node and charge circuit are only started and connected to the input when for a duration of t_{INI}, V_{IN} is within its normal range (above V_{IN_UVLO} and below V_{IN_OVLO}). Qbypass and Qrvs switches will turn off as soon as an input UVLO or OVLO is detected.

As shown in Figure 4, any input state is considered stable if it continuously stays in the same condition for a duration of t_{PWD} after which the device sends out a negative pulse to the nINT pin with a pulse width of t_{INT_PULSE} to inform the host about the input state change.

The watchdog timer WATCHDOG[1:0] register is set to 01 once the valid input is detected and when an INT pulse is asserted, which resumes its original setting when any writing to this device occurs. If the host does not clear the watchdog, power to the host is recycled for reset when watchdog runs time out.

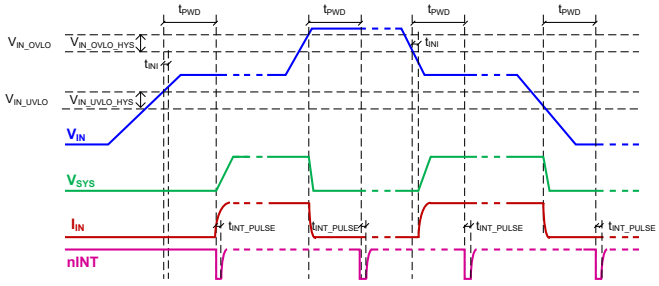


Figure 4. Input Power Detection and nINT Signaling Timings

DETAILED DESCRIPTION (continued)

Power Path Management

When the input voltage is normal and has enough headroom for powering the system (V_{IN} > V_{IN_UVLO} and V_{IN} - V_{BAT} > V_{HDRM}), the input power path will conduct and the device starts to power the system from input by setting the system voltage to V_{SYS_REG}. V_{SYS_REG} is selected by programming VSYS_REG[4:0] register, the lower 5 bits of REG0x07 (also called system voltage register or VSYS_REG[4:0] register). However, the actual system voltage (V_{SYS}) can be affected by the input voltage level, input current limit and battery voltage.

I^2C commands can directly control the power paths. Input path will be disconnected (high-impedance) by turning off Qbypass switch if the EN_HIZ bit is set to 1. If the battery is getting charged and Qswitch switch is on, it can also be disconnected by setting charge enable bit, set the CEB bit to 1 (turn off Qswitch switch in charge direction). The power path control bits are explained in Table 1. When these bits are clear, they have no effect.

Table 1. Switch Control by I^2C Interface

FETs	EN_HIZ = 1	CEB = 1
Qbypass	Off	X
Qswitch (Charging)	X	Off
Qswitch (Discharging)	X	X

NOTE: X = Don't care.

Battery Charge Profile

Figure 5 shows the battery charge profile used in this device. The charge phases are explained below. Depending on the I^2C settings and the battery state of charge (SOC), some or all of the phases may be skipped or used to finish a complete charge cycle as explained below:

Pre-Charge: If the battery voltage is less than the pre-charge threshold (V_{BAT_PRE}), the battery is charged with the small pre-charge current (I_{PRE}). The pre-charge current value is the same as the termination current (I_{TERM}) that is programmed via bits D[3:0] of the REG0x03, also called ITERM[3:0].

Constant-Current Charge: When battery voltage is higher than V_{BAT_PRE}, and less than V_{BAT_REG}, it will be charged with a constant current. The constant-current value is determined by bits D[6:0] of the REG0x02 that is called ICC[6:0] and a single scaling bit that if set, multiplies it by ¼. This bit is used for finer CC adjustment (CC_FINE bit in REG0x0A).

Constant-Voltage Charge: When the battery voltage reaches to the V_{BAT_REG}, the voltage is kept constant and the charge current drown by battery will start to fall. The V_{BAT_REG} value is determined by bits D[7:1] of the REG0x04 that is also called VBAT_REG[6:0].

Charge Termination: A charge termination is recognized when the charge current drops to a small value represented by I_{TERM}. If the termination detection is enabled by setting the EN_TERM bit in REG0x05 D[4] to 1, then if the charge current (I_{CHG}) stays equal or lower than I_{TERM} for a period of t_{TERM_DGL} (termination deglitching time) the charge cycle is considered complete and charging current will be turned off and drop to zero. With no termination, the charge current will continue to drop. Note that a charge cycle is also considered complete and charging will be turned off, if the safe timer function runs out of time provided that the safe timer function is already enabled by setting EN_TIMER bit in REG0x05 D[3] to 1.

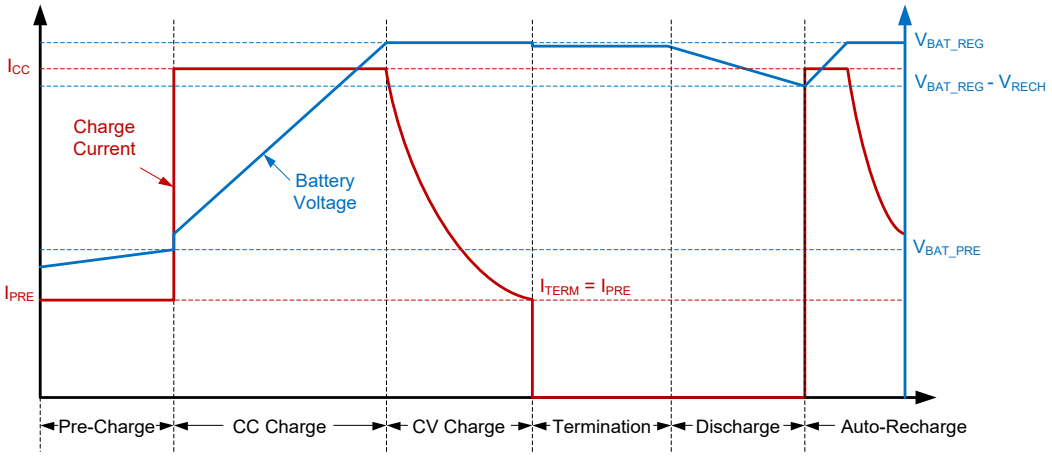


Figure 5. Battery Charge Profile

DETAILED DESCRIPTION (continued)

The charge status is updated to "charge complete" once the termination condition is detected. The charge current will be terminated when termination conditions are met and if the TERM_TMR bit is set to 0 (REG0x05 D[0] = 0). The charge will not terminate and current keeps decreasing if TERM_TMR bit is set to 1.

During the whole charging process, the actual charge current may fall below the set values due to other regulations or controls such as dynamic power management (DPM) regulation caused by insufficient input voltage or current or due to thermal regulation. In thermal regulation the device reduces the power path currents to keep junction temperature below the programmed limit.

If one of the following conditions is satisfied, a new charge cycle starts:

- The input power recycles (input on/off).
- Battery charging is enabled by I^2C command.
- Auto-recharge kicks in due to battery charge state.

If all the following conditions are satisfied:

- No NTC thermistor temperature fault.
- No safety (charge) timer fault.
- No battery over-voltage event.
- The Qswitch switch is not forced to turn off (e.g. CEB = 1).

Battery Over-Voltage Protection

The SGM41562S has a built-in battery over-voltage protection limit. A battery over-voltage event is detected when battery voltage is higher than V_{BAT_OVP} + V_{BAT_REG}. When this event occurs, the charging is immediately suspended and a fault is asserted. The discharging path will be turned on if battery over-voltage condition does not clear and continue.

Input Current and Input Voltage Based Power Management

Usually the input source (typically USB) is not strong enough for all system power demands and a power management scheme is needed to keep the system voltage at desired level without overloading the source. Figure 6 shows the power management profile and explains how it is implemented in SGM41562S including the battery assist operation (supplement) when input source is not able to provide required power.

The input current is continuously monitored to make sure the input source maximum current limit specification is met. The total input current limit is programmable by I^2C and is used to prevent overloading of the input source.

If the input source is weak and the programmed input current limit is higher than the effective capability of the source (like in a dynamic loading condition) the back-up power management will come in effect to prevent overloading of the input source. The back-up power management is based on limiting the input voltage drop to V_{IN_MIN} value (programmable). When the load is higher than the input current capacity, the voltage based dynamic power management (DPM) will adjust the input voltage to V_{IN_MIN}. If input current and voltage limit are both reached, then the Qbypass switch (between IN and SYS pins) will regulate and limit the total power taken from the input. With the power limiting, if the system voltage drops to the minimum value of (V_{SYS_REG} - 90mV) or the input voltage falls below (V_{IN} - 160mV), the device will finally reduce the charge current to prevent further voltage drops.

The programmed V_{IN_MIN} must be at least 250mV higher than V_{BAT_REG} to assure stable operation of the regulator.

DETAILED DESCRIPTION (continued)

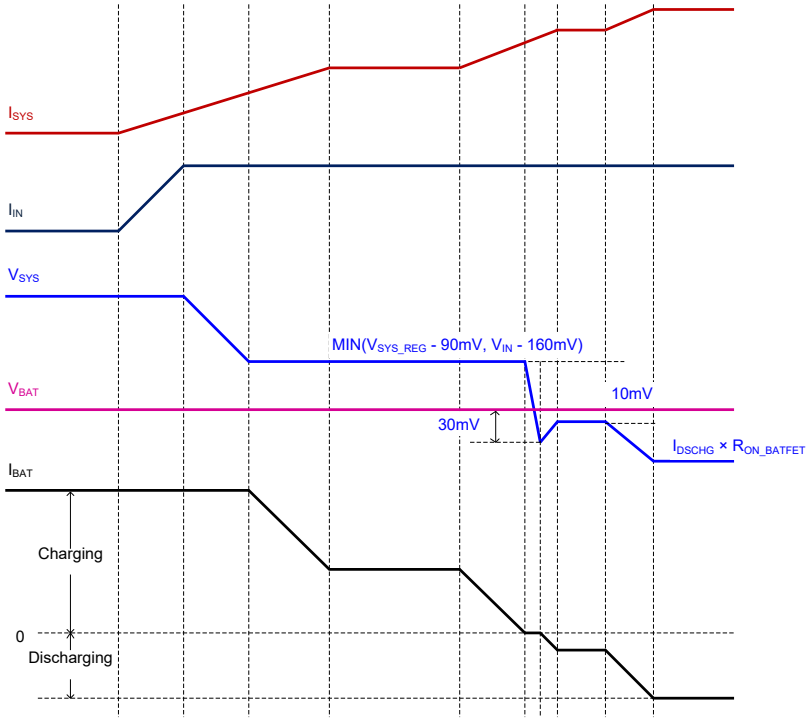


Figure 6. Dynamic Power Management and Battery Supplement Operation Profile

Battery Supplement Mode

As mentioned above, the DPM will reduce the charge current to keep the input current or voltage in regulation when source power is not sufficient for system demand. If the charge current is reduced to zero but still due to heavy system load, the input source is overloaded and V_{SYS} continues to drop, then the battery will supply the deficit to assist the input source. This mode is called battery supplement mode in which the battery provides I_{DSCHG} as supplement current to the load. This mode starts when the system drop reaches to 30mV below the battery voltage. In this mode the Qswitch switch acts as a near ideal diode from battery to the system. The Qswitch switch is controlled to regulate and maintain the V_{BAT} - V_{SYS} drop to a fixed 10mV value when I_{DSCHG} × R_{ON_BATFET} is less than 10mV. If I_{DSCHG} × R_{ON_BATFET} is larger than 10mV, the Qswitch switch is fully turned on to pass battery voltage to the system with minimum drop.

In the battery supplement mode, the ideal diode mode will be disabled as soon as the system load decreases and V_{SYS} exceeds the V_{BAT} + 20mV value.

When V_{IN} source is not available, the device operates in discharge mode (battery power) in which the Qswitch switch is always fully on to reduce the losses.

Battery Regulation Voltage

The battery voltage for the constant-voltage regulation phase (CV) is represented by V_{BAT_REG}.

Thermal Regulation and Shutdown

The SGM41562S continuously monitors the internal junction temperature to avoid junction overheating while keeping the power delivery at its maximum. When the internal junction temperature reaches its programmable limit (T_{J_REG}), the device starts to reduce the charge current to prevent higher power dissipation. The thermal regulation limit is programmable to help adjust the design for the thermal requirements in different applications. 4 different junction temperature regulation thresholds (default 120℃) can be chosen by programming the TJ_REG[1:0] register. In particular, it is recommended that the junction temperature be set not lower than the ambient temperature at which the device charging behavior may occur.

The device fixed thermal shutdown limit (T_{J_SHDN}) is slightly higher than the highest programmable T_{J_REG}. If T_J rises above this limit, both Qbypass and Qswitch switches will turn off.

DETAILED DESCRIPTION (continued)

NTC Function and VDD Gating

The NTC pin is provided to sense the battery temperature using an NTC thermistor. Thermistors are usually included in the rechargeable battery packs to ensure safe operation by monitoring the battery temperature and making sure it is between hot and cold limits. To adjust the temperature limits for the device, two resistors (R_{T1} and R_{T2} in Figure 12) should be connected to NTC pin as a divider between VDD and GND pins. The thermistor itself is connected between NTC pin and GND. The voltage on the NTC pin is determined by all three resistors. This resistor divider along with the hot and cold limit voltages defined in the Electrical Characteristics table determines the hot-cold operating window. Note that due to the negative temperature coefficient of NTC, when its voltage drops below V_{HOT}, it means the battery temperature is exceeding the hot limit. The NTC protection function can be disabled by clearing the EN_NTC bit to 0. The default settings for NTC function are the PCB OTP levels specified in Electrical Characteristics table that can be change by I^2C as explained in Table 2.

Table 2. NTC Function Selection

I^2C Control		Function
EN_NTC	PCB_OTP_DIS	
0	Don't care	Disable
1	1	NTC
1	0	PCB OTP

NTC function only works in charge mode. When NTC pin voltage falls out of the hot-cold window, it means that the temperature is outside the safe operating range and results in a pause in charging and sets the fault bits. The charging will resume when the temperature falls back into the safe range.

If VDD_DIS bit is disabled and V_{IN} is removed, V_{DD} power turns off and becomes high-impedance leaving only R_{T2} in parallel with the NTC thermistor. If VDD_DIS bit is enabled, V_{DD} remains active. V_{DD} uses battery power if V_{IN} is removed.

With PCB OTP selected, if the NTC pin voltage is lower than the NTC hot threshold, Qbypass and Qswitch switches will turn off. The PCB OTP fault will also set the NTC_FAULT status bit to 1. The operation will resume when the NTC pin voltage goes back above the NTC hot threshold.

Safety Timer

Using an internal safety timer, the SGM41562S is capable to limit the maximum duration of the pre-charge and charge periods to avoid extended charging cycles that may happen due to abnormal battery conditions. This protection can be disabled by I^2C. The safety timer starts counting if one of the following occurs. A new charge cycle is started.

- Write in REG0x01 D[3] (CEB) bit: from 1 to 0 (charge enable)
- Write in REG0x05 D[3] (EN_TIMER) bit: from 0 to 1 (safety timer enable)
- Write in REG0x02 D[7] (REG_RST) bit: from 0 to 1 (software reset)
- Write in REG0x0A D[4] (COLD_RESET) bit: from 0 to 1 (software power recycle)

The safety time limit is 1 hour for pre-charge condition in which the battery voltage stays lower than V_{BAT_PRE} and cannot go higher. For the charge phase the time limit is programmable through I^2C and the safety timer starts counting when the battery enters in constant-current charge mode or constant-voltage charge mode.

Host Mode and Default Mode

The SGM41562S can operate in either default mode (with default parameters) or host mode (parameters programmed by host). It will go to the default mode if one of the following occurs:

- Input refresh with no battery connected.
- Re-insert battery with no input source connected.
- Device registers reset by writing 1 to REG_RST bit.
- Watchdog timer expiry.

Upon a power-on reset, the device starts in default mode and in the same state as if watchdog timer expiration has occurred. In this mode, all registers take their default values, including EN_HIZ = 0 and CEB = 1, that means the input power path is enabled and device is set to battery discharge mode. Note that by default the battery will not be charged after a reset.

When the device is in the host mode, watchdog function can be activated and works in both charge and discharge modes (watchdog timer is independent of the charge safety timer). Watchdog timer can be enabled by programming a non-zero expiry time in its register, that is WATCHDOG[1:0] ≠ 00. If watchdog timer is enabled, it must be reset regularly before it runs out of time by writing 1 to WD_RST bit in REG0x02. Otherwise, the watchdog timer will expire and this will result in a power recycle to the system. Therefore, resetting the watchdog timer by host must happen in the intervals shorter than watchdog time limit. The power recycle is performed by turning off Qswitch and Qbypass for a duration of t_{RST_DUR} and then turning them on again. After watchdog timer expiration, all registers will reset to their default values and the device goes to the default mode.

To reduce the quiescent current during discharge mode, the watchdog timer can be turned off by setting the EN_WD_DISCHG bit to 0. If the WATCHDOG[1:0] register is set to 00, the watchdog timer is disabled under charge and discharge modes independent of the EN_WD_DISCHG bit value.

DETAILED DESCRIPTION (continued)

Battery Discharge Function

If the battery is connected (V_{BAT} is above the V_{BAT_UVLO} threshold) and the input source is missing, the Qswitch turns fully on. The low on-resistance of the Qswitch minimizes the conduction loss during discharge. The quiescent current is as low as 9μA in this mode. By setting SWITCH_MODE bit (REG0x0A D[3]) to 1, the Qswitch will stay on even if the rest of the internal blocks are turned off, to reduce the quiescent current to less than 1μA. The low on-resistance and low quiescent current of the device extend the run time.

Over-Discharge Current Protection

The over-discharge current protection is effective in discharge mode and supplement mode. If the I_{BAT} exceeds discharge current limit value programmed in the REG0x03 D[7:4] (IDSCHG[3:0] bits), the Qswitch turns off after a wait delay (t_{DSCHG_CUT}) and then resumes conducting after a retry delay time (t_{RETRY}).

When the battery voltage falls below the V_{BAT_UVLO} limit that is programmed in the REG0x01 D[2:0] (VBAT_UVLO[2:0] bits), the Qswitch turns off to prevent over-discharging the battery.

If SWITCH_MODE bit (REG0x0A D[3]) is set to 1, the Qswitch is forced to remain on like a simple switch and the over-discharge is ignored during battery discharge. This bit will reset if power is re-applied to the input. It will also reset if the battery is connected or disconnected while power is applied to the input.

System Short-Circuit Protection

If the short-circuit (to GND) occurs on the load connected to SYS pin, the Qswitch disconnects the BAT to SYS path and the Qbypass limits the current flowing in the IN to SYS path. If the short-circuit persists, the die temperature goes high and causes a thermal shutdown.

Interrupt to Host (nINT Pin)

The nINT output signal is provided to alert the host on power events. The SGM41562S sends out a negative pulse (width = t_{INT_PULSE}) to nINT if any of the following events occurs:

- A good input source is detected (UVLO < V_{IN} < OVLO).
- UVLO or OVLO is detected (input).
- Charge completed.
- A charging status change.
- A fault record in REG0x09 occurs (input fault, thermal fault, safety timer fault, battery OVP fault or NTC fault).
- Watchdog expiration (WTD_FAULT bit in REG0x08 D[7]).

When one of the mentioned faults occurs, the relevant fault bit will latch in the register except for NTC fault bit that always reports the current status of the thermistor. A fault status bit is unlatched if the device quits that fault state. It will reset to 0 after the host reads the register if the bit is unlatched.

The assertion of nINT signal pulse can be masked for some of the events listed above when the corresponding mask control bits are set in REG0x06 D[4:0]. If a mask bit is set, and the event occurs, the nINT signals stay high.

The nINT pin is also used as an input to initiate a power recycle on the SYS output, for example, when a turn-off/turn-on is needed on the system when battery is not removable. This input is also used to exit the shipping mode that keeps the battery disconnected.

Battery Disconnection Function

When the battery is not removable, it is essential to disconnect the battery from the system to allow system power recycling or to put that in the shipping mode. It is performed by forcing the Qswitch to remain off by setting FET_DIS bit to 1. Table 3 explains how the SGM41562S can be programmed in shipping mode (or to do a power recycle on SYS) and how to exit the shipping mode. To exit shipping mode, either the input power should be applied to IN port, or a low voltage (ground) should be applied to nINT pin for a short time (for example by holding a push bottom).

Table 3. Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	FET_DIS = 1	nINT Pin H to L for 2s	V_{IN} Plug-In
Qbypass	Don't care	Don't care	On
Qswitch (Charging)	Off	On	On (100ms later)
Qswitch (Discharging)	Off	On	On (100ms later)

The FET_DIS bit is used for battery disconnection control. When the bit is set to 1, the device enters the shipping mode after a delay time, which is dependent on EN_SHIP_DGL[1:0] register. After the delay, the Qswitch turns off and the FET_DIS bit resets to 0. The device wakes up from shipping mode by pulling down nINT pin or detecting an acceptable voltage on the IN pin. The device exits from shipping mode 2 seconds after pulling nINT pin down or 100ms after detecting an acceptable V_{IN}. For the application of nINT pulled down to a low voltage in the shipping mode, the EN_SHIP_DGL[1:0] register must keep its default value.

DETAILED DESCRIPTION (continued)

The system power can be recycled by turning off the Qswitch and Qbypass if nINT pin is pulled low for a duration of more than t_{RST_DGL}. It is the time delay to avoid noise and glitches or to hold a push bottom. The t_{RST_DGL} time is programmed by tRST_DGL[1:0] bits in REG0x01. The off state lasts for a duration of t_{RST_DUR} which can be programmed via tRST_DUR bit in REG0x01. After this time the Qswitch and/or Qbypass will be automatically turned on and the system is powered again. During the off period, the nINT pin is biased to a lower voltage.

If nINT pin is shorted to GND or left floating before entering the shipping mode, the INT_DIS bit (REG0x0C D[2]) must be written to 1 to avoid bad shipping mode operation. In this case, the only method of exiting shipping mode is plugging-in the V_{IN}.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address: 03H

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

PORV: Power-On Reset Value

n: Parameter code formed by the bits as an unsigned binary number.

REG0x00: [Reset = 0x90]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	VIN_MIN[3:0]	1	R/W	VIN_MIN[3] 1 = 640mV	Minimum Input Voltage Limit (n: 4 bits): = 3.88 + 0.08n (V) Offset: 3.88V Range: 3.88V (0000) - 5.08V (1111) Default: 4.60V (1001)	REG_RST
		0	R/W	VIN_MIN[2] 1 = 320mV		REG_RST
		0	R/W	VIN_MIN[1] 1 = 160mV		REG_RST
		1	R/W	VIN_MIN[0] 1 = 80mV		REG_RST
D[3]	PRECHARGE-TO	0	R/W	Pre-Charge Safe Time 0 = 1h (default) 1 = 2h		REG_RST
D[2]	INT EXIT-SHIP	0	R/W	INT Exit Shipping Mode 0 = 2s (default) 1 = 100ms		REG_RST
D[1]	VIN EXIT-SHIP	0	R/W	VIN Plug Exit Shipping Mode 0 = 2s (default) 1 = 100ms		REG_RST
D[0]	ITERM_TIMER	0	R/W	ITERM Deglitch Timer Setting 0 = 200ms (default) 1 = 40ms		REG_RST

REG0x01: [Reset = 0xAC]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:6]	tRST_DGL[1:0]	10	R/W	nINT Pull-Down Period to Disconnect the Battery (n: 2 bits): = 8s + 4n (seconds) 00 = 8s 01 = 12s 10 = 16s (default) 11 = 20s		REG_RST or Watchdog
D[5]	tRST_DUR	1	R/W	Battery FET Off-Time Duration after Reset The Qbypass and Qswitch off-time before auto turn-on. 0 = 2s 1 = 4s (default)		REG_RST or Watchdog
D[4]	EN_HIZ	0	R/W	HIZ Mode Enable 0 = Disable (default) 1 = Enable Control Qbypass Switch Default: disable (0) or switch on Note: The EN_HIZ bit only controls the on and off of the Qbypass.		REG_RST or Watchdog
D[3]	CEB	1	R/W	Setting Charge Enable 0 = Charge enable 1 = Charge disabled (default) Charge Enable/Disable Qswitch Configuration Default: charge disabled (1) or Qswitch off		REG_RST or Watchdog
D[2:0]	VBAT_UVLO[2:0]	1	R/W	VBAT_UVLO[2] 1 = 360mV	Battery UVLO Threshold Value (n: 3 bits): = 2.4V + 0.09n (V) Offset: 2.4V Range: 2.4V (000) - 3.03V (111) Default: 2.76V (100)	REG_RST or Watchdog
		0	R/W	VBAT_UVLO[1] 1 = 180mV		REG_RST or Watchdog
		0	R/W	VBAT_UVLO[0] 1 = 90mV		REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x02: [Reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	REG_RST	0	R/W	Software Reset 0 = Keep current setting (default) 1 = Reset If set, will reset most parameters to default. (as explained in the last column of register map tables)		REG_RST
D[6:0]	ICC[6:0]	0	R/W	ICC[6] 1= 512mA	Fast Charge Current Value (CC Mode) (n: 6 bits): = 8mA + 8n (mA) Offset: 8mA Range: 8mA (000 0000) - 1024mA (111 1111) Default: 128mA (000 1111)	REG_RST or Watchdog
		0	R/W	ICC[5] 1= 256mA		REG_RST or Watchdog
		0	R/W	ICC[4] 1 = 128mA		REG_RST or Watchdog
		1	R/W	ICC[3] 1 = 64mA		REG_RST or Watchdog
		1	R/W	ICC[2] 1 = 32mA		REG_RST or Watchdog
		1	R/W	ICC[1] 1 = 16mA		REG_RST or Watchdog
		1	R/W	ICC[0] 1 = 8mA		REG_RST or Watchdog

REG0x03: [Reset = 0x91]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	IDSCHG[3:0]	1	R/W	IDSCHG[3] 1 = 1600mA	BAT to SYS Discharge Current Limit Value (n: 4 bits): = 200mA + 200n (mA), n ≠ 0 Offset: 200mA Valid Range: 400mA (0001) - 3.2A (1111) Default: 2000mA (1001)	REG_RST or Watchdog
		0	R/W	IDSCHG[2] 1 = 800mA		REG_RST or Watchdog
		0	R/W	IDSCHG[1] 1 = 400mA		REG_RST or Watchdog
		1	R/W	IDSCHG[0] 1 = 200mA		REG_RST or Watchdog
D[3:0]	ITERM[3:0]	0	R/W	ITERM[3] 1 = 16mA	Charge Termination Current Value (n: 4 bits): = 1mA + 2n (mA) Offset: 1mA Range: 1mA (0000) - 31mA (1111) Default: 3mA (0001)	REG_RST or Watchdog
		0	R/W	ITERM[2] 1 = 8mA		REG_RST or Watchdog
		0	R/W	ITERM[1] 1 = 4mA		REG_RST or Watchdog
		1	R/W	ITERM[0] 1 = 2mA		REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x04: [Reset = 0x8D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:1]	VBAT_REG[6:0]	1	R/W	VBAT_REG[6] 1 = 640mV	Charge Voltage Limit (n: 7 bits): = 3500 + 10n (mV) Offset: 3.5V Range: 3500mV - 4770mV Default: 4.200V (100 0110) Clamped Low Clamped High Bit Step: 10mV	REG_RST or Watchdog
		0	R/W	VBAT_REG[5] 1 = 320mV		REG_RST or Watchdog
		0	R/W	VBAT_REG[4] 1 = 160mV		REG_RST or Watchdog
		0	R/W	VBAT_REG[3] 1 = 80mV		REG_RST or Watchdog
		1	R/W	VBAT_REG[2] 1 = 40mV		REG_RST or Watchdog
		1	R/W	VBAT_REG[1] 1 = 20mV		REG_RST or Watchdog
		0	R/W	VBAT_REG[0] 1 = 10mV		REG_RST or Watchdog
D[0]	VRECH	1	R/W	Battery Recharge Threshold 0 = 100mV 1 = 200mV (default) Offset below V_{BAT_REG}.		REG_RST or Watchdog

REG0x05: [Reset = 0x7A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_WD_DISCHG	0	R/W	Watchdog Control 0 = Disable (default) 1 = Enable Watchdog control in discharge mode.	REG_RST
D[6:5]	WATCHDOG[1:0]	11	R/W	Watchdog Timer 00 = Disable timer 01 = 64s 10 = 128s 11 = 256s (default) If WATCHDOG[1:0] = 00, the watchdog timer is disabled regardless of whether EN_WD_DISCHG bit is set.	REG_RST
D[4]	EN_TERM	1	R/W	Termination Control 0 = Disable 1 = Enable (default) Use termination or not.	REG_RST or Watchdog
D[3]	EN_TIMER	1	R/W	Safety Timer Control 0 = Disable 1 = Enable (default) Charge safety timer enable/disable setting.	REG_RST or Watchdog
D[2:1]	CHG_TMR[1:0]	01	R/W	Charge Timer 00 = 3h 01 = 5h (default) 10 = 8h 11 = 12h	REG_RST or Watchdog
D[0]	TERM_TMR	0	R/W	Termination Timer Control 0 = Disable (default) 1 = Enable When TERM_TMR bit is enabled, the device will not suspend the charge current after charge termination.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x06: [Reset = 0xC0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_NTC	1	R/W	NTC Control 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[6]	EN_TMR2X	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Enable 2× extended safety timer during PPM (default)	REG_RST or Watchdog
D[5]	FET_DIS	0	R/W	0 = Enable (default) 1 = Disable Qswitch control for shipping mode and system power recycle. Note: The FET_DIS bit controls the on and off of the Qswitch in both charging and discharging.	REG_RST
D[4]	PG_INT_CTL	0	R/W	0 = On (default) 1 = Off	REG_RST or Watchdog
D[3]	EOC_INT_CTL	0	R/W	Charge Completed INT Mask Control 0 = On (default) 1 = Off	REG_RST or Watchdog
D[2]	CHG_STATUS_ INT_CTL	0	R/W	Charging Status Change INT Mask Control 0 = On (default) 1 = Off Charging statuses are: not charging, pre-charge and charge.	REG_RST or Watchdog
D[1]	NTC_INT_CTL	0	R/W	0 = On (default) 1 = Off	REG_RST or Watchdog
D[0]	BATOVP_INT_CTL	0	R/W	0 = On (default) 1 = Off	REG_RST or Watchdog

REG0x07: [Reset = 0x73]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	VINLOOP_DIS	0	R/W	0 = Enable (default) 1 = Disable		REG_RST or Watchdog
D[6:5]	TJ_REG[1:0]	11	R/W	Thermal Regulation Threshold 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)		REG_RST or Watchdog
D[4:0]	VSYS_REG[4:0]	1	R/W	VSYS_REG[4] 1 = 800mV	System Regulation Voltage Value (n: 5 bits): = 3.6V + 0.05n (V) Offset: 3.6V Range: 3.6V (0 0000) - 5.15V (1 1111) Default: 4.55V (1 0011)	REG_RST
		0	R/W	VSYS_REG[3] 1 = 400mV		REG_RST
		0	R/W	VSYS_REG[2] 1 = 200mV		REG_RST
		1	R/W	VSYS_REG[1] 1 = 100mV		REG_RST
		1	R/W	VSYS_REG[0] 1 = 50mV		REG_RST

REGISTER MAPS (continued)

REG0x08: [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WTD_FAULT	0	R	Watchdog Expiration 0 = Normal (default) 1 = Watchdog timer expiration	N/A
D[6]	PCB_OTP_DIS	0	R/W	PCB OTP Enable 0 = Enable (default) 1 = Disable	REG_RST or Watchdog
D[5]	VIN_OVP_SEL	0	R/W	0 = 6V (default) 1 = 19V	REG_RST
D[4:3]	CHG_STAT[1:0]	00	R	Charging Status 00 = Not charging (default) 01 = Pre-charge 10 = Charge 11 = Charge done	N/A
D[2]	PPM_STAT	0	R	Device in Power Path Management Mode (PPM) 0 = No PPM (default) 1 = In PPM	N/A
D[1]	PG_STAT	0	R	Input Power (IN) Status 0 = Power fail (default) 1 = Power good	N/A
D[0]	THERM_STAT	0	R	Thermal Regulation Status 0 = No thermal regulation (default) 1 = In thermal regulation	N/A

REG0x09: [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	EN_SHIP_DGL[1:0]	00	R/W	Enter Shipping Mode Deglitch Time 00 = 1s (default) 01 = 2s 10 = 4s 11 = 8s	REG_RST
D[5]	VIN_FAULT	0	R	Input VIN Fault Status 0 = Normal (default) 1 = Input fault (OVP or bad source)	N/A
D[4]	THEM_SD	0	R	Thermal Shutdown Fault Status 0 = Normal (default) 1 = Thermal shutdown	N/A
D[3]	BAT_FAULT	0	R	Battery Over-Voltage Fault Status 0 = Normal (default) 1 = Battery OVP	N/A
D[2]	STMR_FAULT	0	R	Safety Timer Expiration Fault Status 0 = Normal (default) 1 = Safety timer expiration	N/A
D[1]	NTC_FAULT[1]	0	R	NTC Exceeding Hot Level 0 = Normal (default) 1 = NTC hot	N/A
D[0]	NTC_FAULT[0]	0	R	NTC Exceeding Cold Level 0 = Normal (default) 1 = NTC cold	N/A

REGISTER MAPS (continued)

REG0x0A: [Reset = 0x60]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	ADDR[2:0]	011	R	Slave Address 001 = 01H 010 = 02H 011 = 03H (default) 100 = 04H 101 = 05H 110 = 06H 111 = 07H	N/A
D[4]	COLD_RESET	0	R/W	Software Power Recycle 0 = No action (default) 1 = Power recycle reset Cause a system power recycles if set to 1. Automatically clear after power recycle.	N/A
D[3]	SWITCH_MODE	0	R/W	0 = Normal power path (default) 1 = Qswitch forced on Effective in battery discharge mode only. When Qswitch is forced on, there is no current and voltage limit because the internal circuits are shut down for lower consumption.	N/A
D[2]	VDD_DIS	0	R/W	0 = Enable battery power (default) 1 = Disable battery power If set to 1, V_{DD} becomes high-impedance when V_{IN} is removed. If the PCB OTP of NTC function is be selected, the VDD_DIS bit setting is invalid.	N/A
D[1]	VINOVP_DIS	0	R/W	0 = Enable (default) 1 = Disable Disable over-voltage lockout detection of V_{IN} if set to 1.	N/A
D[0]	CC_FINE	0	R/W	0 = Normal scale (default) 1 = Fine scale If set to 1, the programmed charge current in ICC[6:0] is weighted to ¼.	N/A

REG0x0B: [Reset = 0x09]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	ID[7:0]	0000 1001	R	Device ID 0000 1001 = SGM41562S	N/A

REG0x0C: [Reset = 0x7A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:3]	IIN_LIM[4:0]	0	R/W	IIN_LIM[4] 1 = 480mA	Input Current Limit (n: 5 bits): = 50 + 30n (mA) Offset: 50mA Range: 50mA (0 0000) - 980mA (1 1111) Default: 500mA (0 1111)	REG_RST
		1	R/W	IIN_LIM[3] 1 = 240mA		REG_RST
		1	R/W	IIN_LIM[2] 1 = 120mA		REG_RST
		1	R/W	IIN_LIM[1] 1= 60mA		REG_RST
		1	R/W	IIN_LIM[0] 1 = 30mA		REG_RST or Watchdog
D[2]	INT_DIS	0	R/W	Disable INT Function during Shipping Mode 0 = INT function (default) 1 = Disable INT function during shipping mode		REG_RST or Watchdog
D[1]	VBAT_PRE	1	R/W	Pre-Charge to Fast Charge Threshold 0 = 2.8V 1 = 3.0V (default)		REG_RST or Watchdog
D[0]	WD_RST	0	R/W	I^2C Watchdog Timer Reset 0 = Normal (default) 1 = Reset If set, watchdog timer will be reset.		REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0D: [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	IPRECHG[3:0]	0	R/W	IIN_LIM[3] 1 = 16mA	Pre-charge Current Value (n: 4 bits): = 1 + 2n (mA) Offset: 1mA Range: 1mA (0000) - 31mA (1111) Default: 3mA (0001)	REG_RST or Watchdog
		0	R/W	IIN_LIM[2] 1 = 8mA		
		0	R/W	IIN_LIM[1] 1 = 4mA		
		1	R/W	IIN_LIM[0] 1= 2mA		
D[3]	IPRECHG6	0	R/W	IPRECHG Range Select in Charge Mode 0 = IPRECHG[3:0] (default) 1 = IPRECHG[3:0] × 6		REG_RST or Watchdog
D[2]	ITERM6	0	R/W	ITERM Range Select in Charge Mode 0 = ITERM[3:0] (default) 1 = ITERM[3:0] × 6		REG_RST or Watchdog
D[1:0]	Reserved	00	R/W	Reserved		REG_RST or Watchdog

STATE CONVERSION CHART

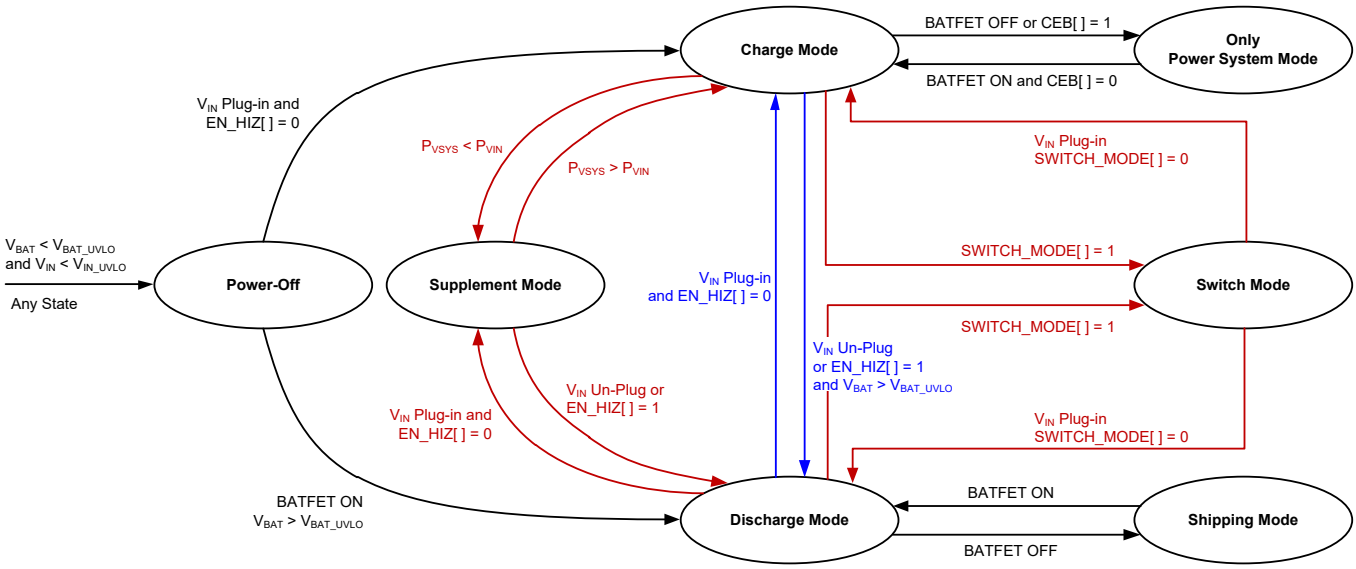


Figure 7. State Machine Conversion

CONTROL FLOW CHART

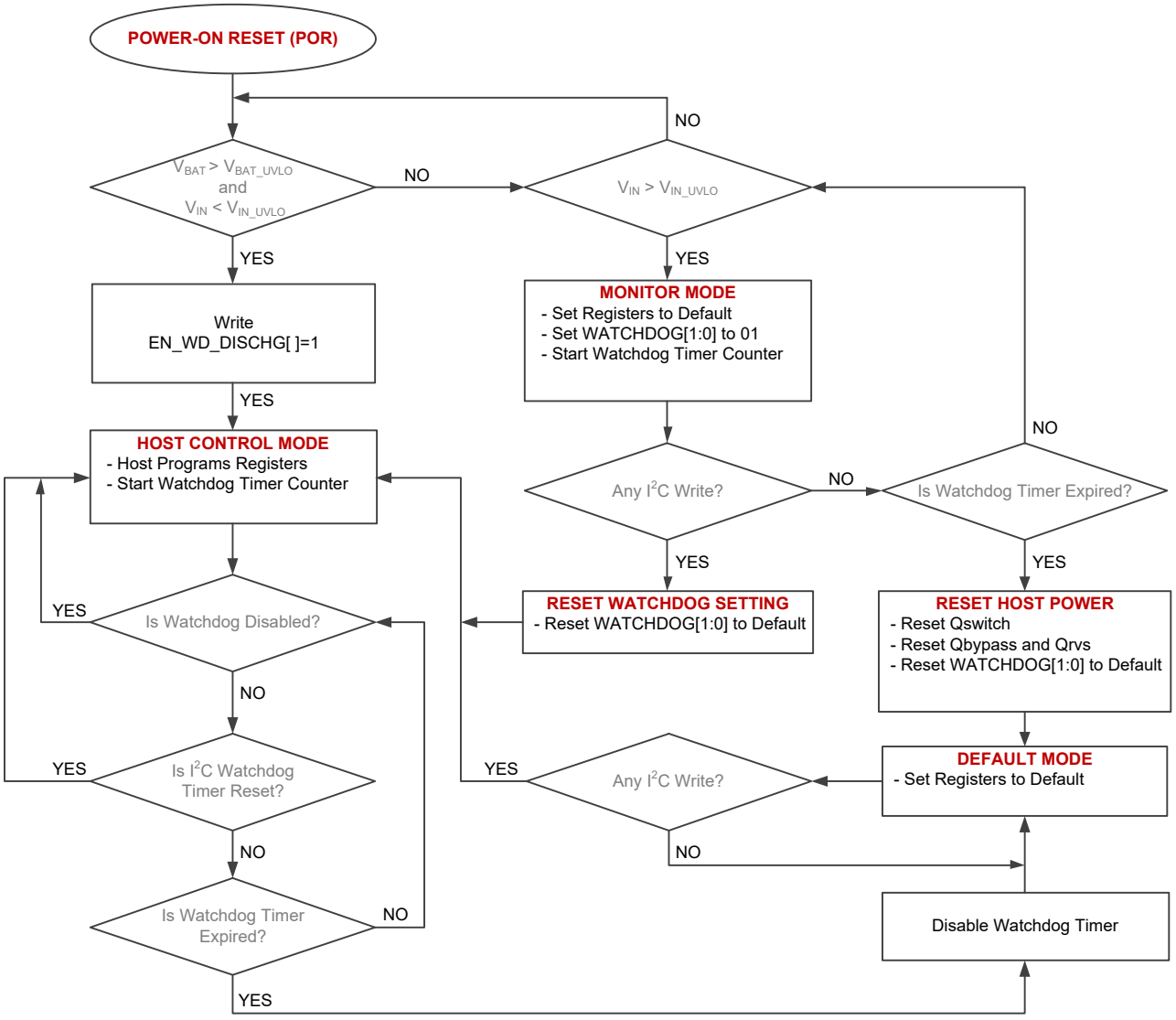


Figure 8. Startup, Host Mode, Default Mode and Host Power Reset

CONTROL FLOW CHART (continued)

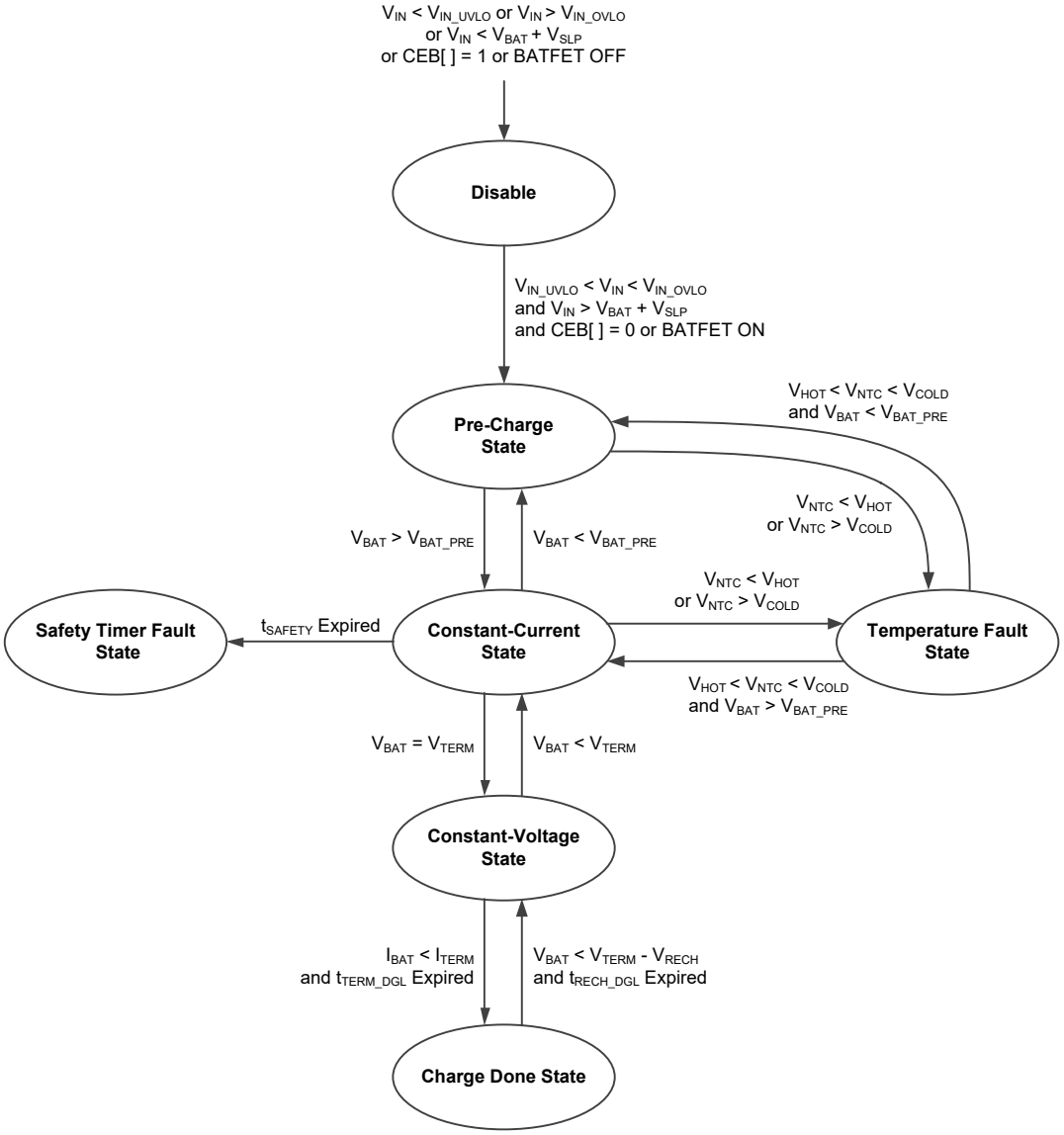


Figure 9. Charging Process

CONTROL FLOW CHART (continued)

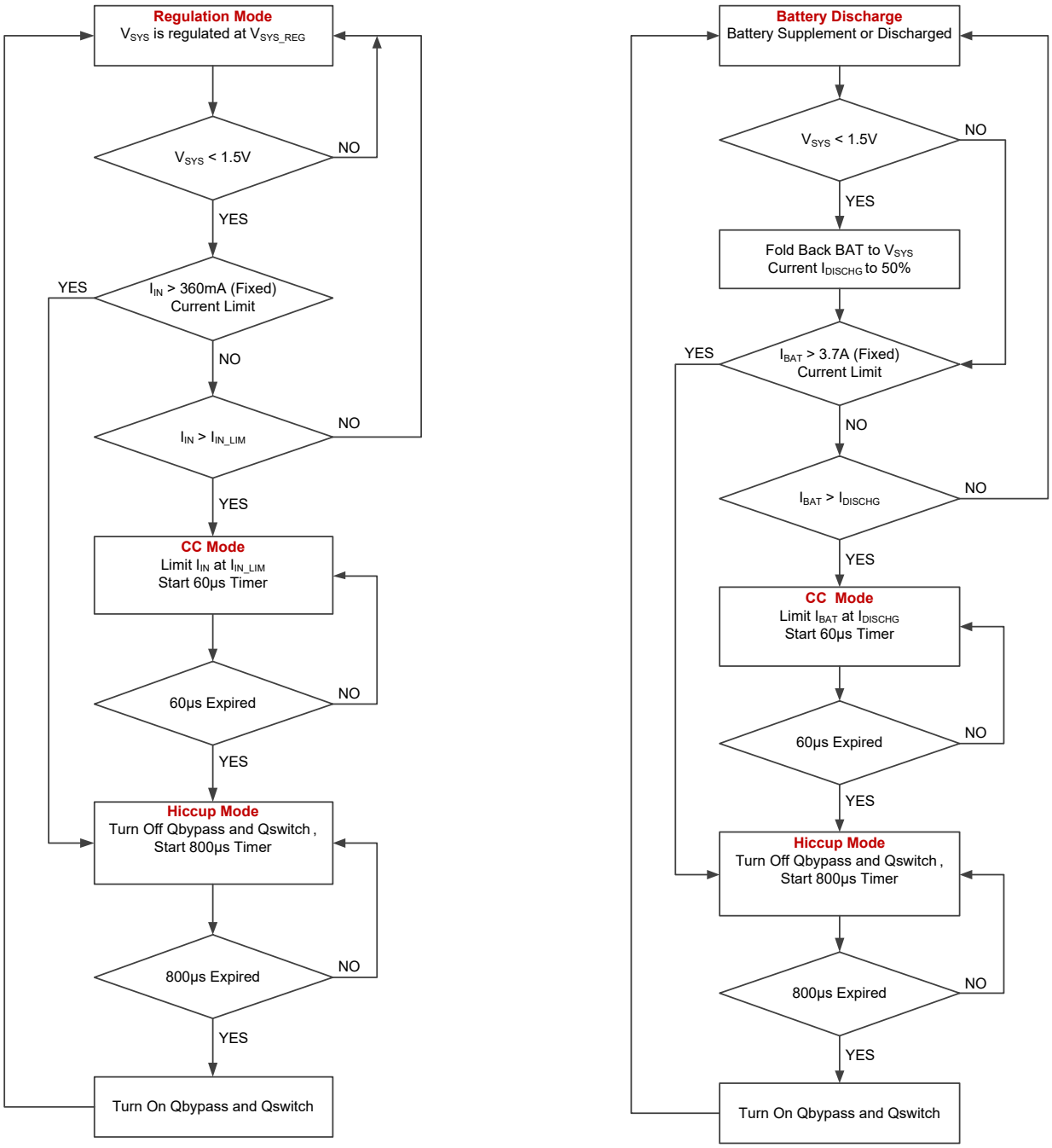


Figure 10. System Short-Circuit Protection

APPLICATION INFORMATION

Resistor Divider for NTC Sensor

A resistor divider between VDD and GND pins can be used to adjust the battery temperature limits sensed by the NTC sensor. The R_{T1} and R_{T2} resistors (see Figure 11) allow independent programming of the high and low temperature limits for any type of NTC temperature characteristics.

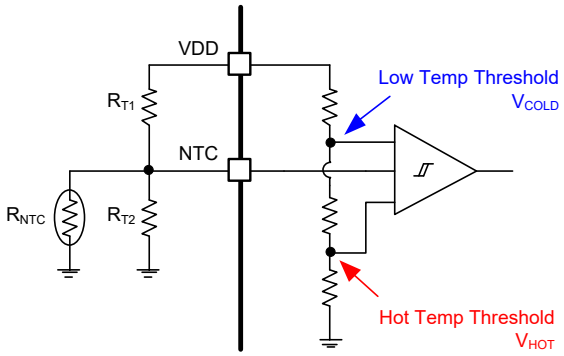


Figure 11. NTC Function Block

For a given NTC thermistor, if the NTC resistances at the desired high and low temperatures are R_{NTCH} and R_{NTCL} respectively, R_{T1} and R_{T2} values can be calculated by:

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1 - V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

where V_{COLD} and V_{HOT} thresholds values are voltage levels on the NTC pin given in the Electrical Characteristics table for the hot and cold detection.

For example, for a thermistor with $R_{25℃}$ = 10kΩ and β = 3260, R_{NTCL} is 27.2kΩ at T_{COLD} = 0℃, and R_{NTCH} is 4.29kΩ at T_{HOT} = 50℃. Assuming that the NTC window is between 0℃ and 50℃, and using the values of V_{COLD} and V_{HOT} in Electrical Characteristics table, R_{T1} = 7.6kΩ and R_{T2} = 29.33kΩ are calculated by Equation 1 and Equation 2 (recalculation is needed, when mean values are characterized in the Electrical Characteristics table).

External Capacitor Selection

Like many low-dropout regulators, the SGM41562S requires external capacitors on its power ports for stability and noise or spike voltage immunity. These capacitors must be properly selected and placed near the device.

Input Capacitor (IN to GND)

A minimum 2.2μF input capacitor must be connected between IN and GND pins for stable operation over full load range. In general an output capacitance larger than the input capacitor is acceptable if the input capacitor is at least 2.2μF.

Output Capacitor (SYS to GND)

The SGM41562S is designed specifically to operate with small ceramic output capacitance. A ceramic capacitor (X5R or X7R) larger than 2.2μF is suitable for the SGM41562S applications. The output capacitor should be connected close to the device between SYS and GND pins with thick traces and small loop area.

BAT to GND Capacitor

A capacitor is needed between BAT and GND pins. Use a ceramic capacitor (X5R or X7R) that is at least 2.2μF.

VDD to GND Capacitor

VDD voltage powers the internal control and logic circuit. It is critical to use a 0.1μF decoupling ceramic capacitor between VDD pin and GND close to the device with thick PCB traces to decouple noise and stabilize VDD voltage.

PCB Layout Guide

1. Place external capacitors as close as possible to the device to minimize stray inductances and connection impedance.
2. The GND for the I^2C signals should be clean and directly connected to GND pin, without sharing its route with GND returns that carry high current or switching currents.
3. Due to relatively slow rise/fall times, it is able to route the I^2C wires in parallel on the same PCB layer.

TYPICAL APPLICATION CIRCUIT

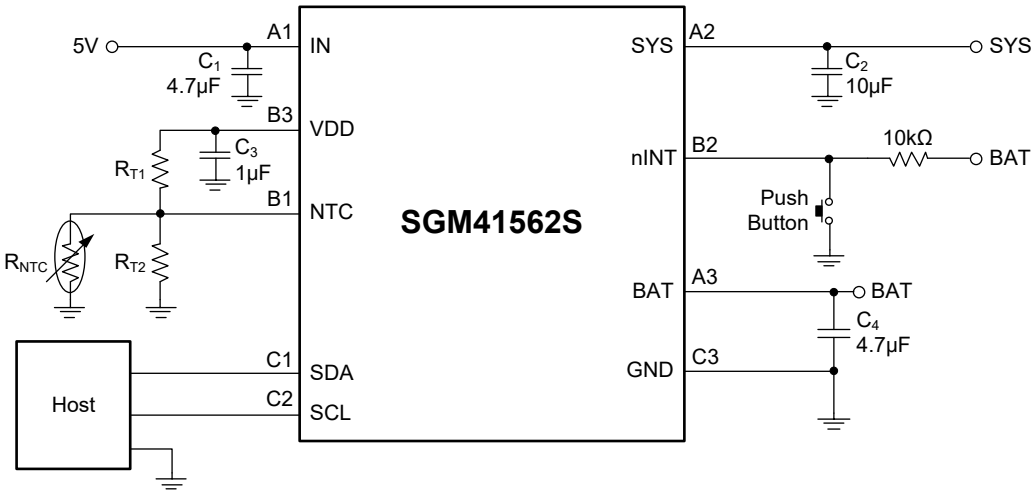


Figure 12. SGM41562S Typical Application Circuit with 5V Input

REVISION HISTORY

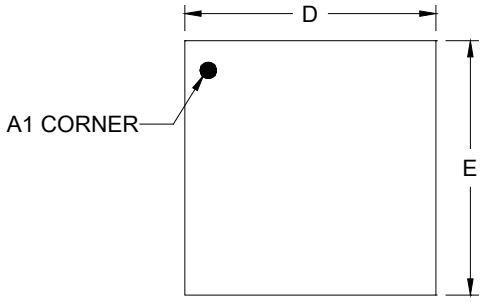
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2026 – REV.A to REV.A.1	**Page**
Updated Electrical Characteristics section	5

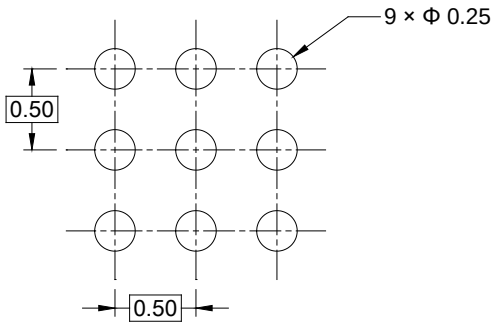
Changes from Original to REV.A (DECEMBER 2025)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

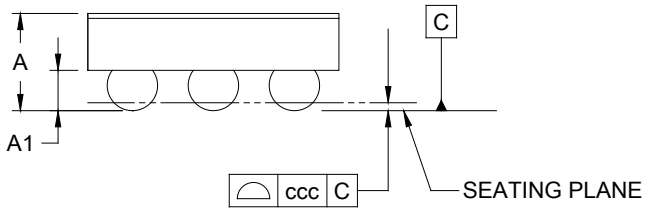
WLCSP-1.55×1.57-9B



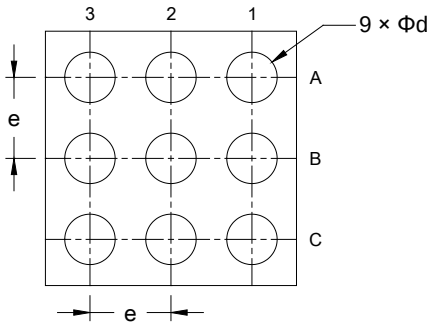
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



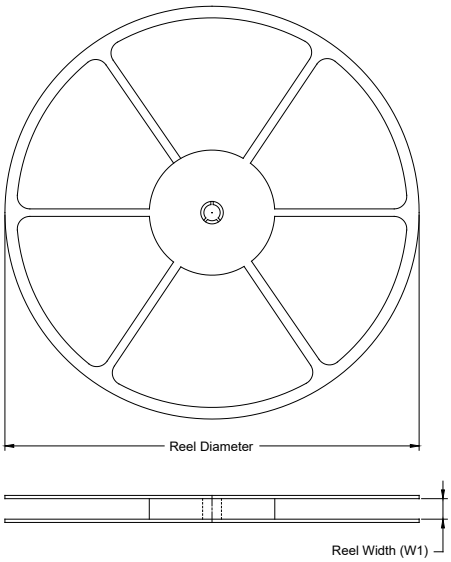
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.638
A1	0.229	-	0.269
D	1.520	-	1.580
E	1.540	-	1.600
d	0.281	-	0.341
e	0.500 BSC		
ccc	0.050		

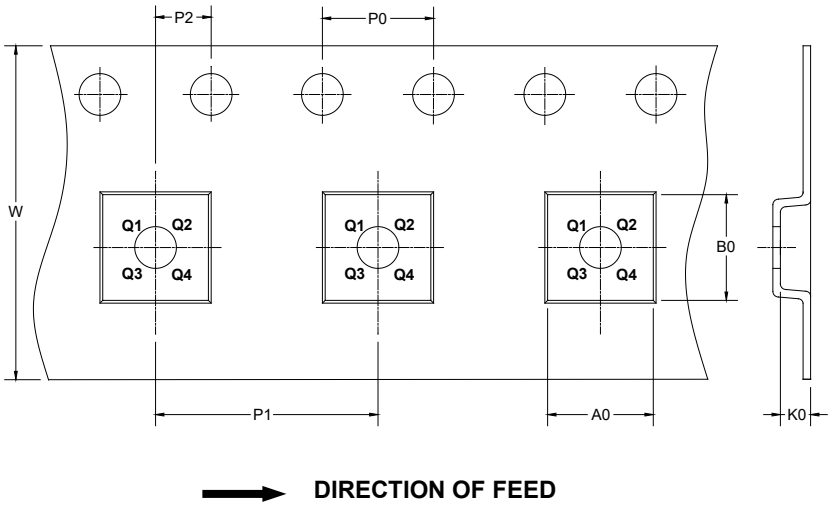
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



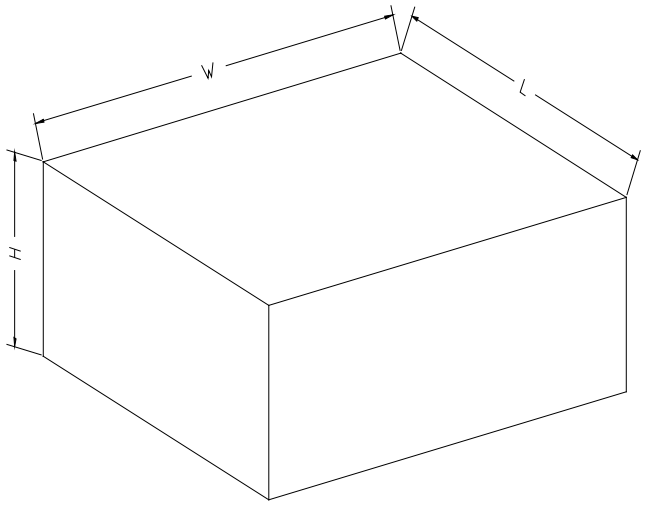
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.55×1.57-9B	7″	9.5	1.65	1.70	0.71	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002