74LVC2T45
2-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation

GENERAL DESCRIPTION

The 74LVC2T45 is a 2-bit, dual-supply bus transceiver with configurable voltage translation. The device has two separate configurable power-supply rails. The A and B ports track the V_{CCA} supply and V_{CCB} supply respectively. The supply voltage pins accept voltage range from 1.65V to 5.5V, which makes the device suitable for low voltage bidirectional translation voltage nodes of 1.8V, 2.5V, 3.3V and 5V.

The 74LVC2T45 features that two data buses can communicate asynchronously. Either the A port outputs or the B port outputs can be activated by DIR logic levels. The DIR input circuit is supplied by V_{CCA}. When B port outputs are activated, the device allows the data to transmit from A bus to B bus. On the contrary, when A port outputs are activated, the device allows the data to transmit from B bus to A bus. The input circuit is always active on the two ports. A logic level of high or low must be set to avoid excessive supply current.

The 74LVC2T45 is available in Green MSOP-8, XTDFN-1.35×1-8L and VSSOP-8 packages. It operates over a temperature range of -40℃ to +125℃.

FEATURES

- **V_{CCA} Supply Voltage Range: 1.65V to 5.5V**
- **V_{CCB} Supply Voltage Range: 1.65V to 5.5V**
- **DIR Input Circuit Referenced to V_{CCA}**
- **Typical Data Rates:**
  - **420Mbps (3.3V to 5V Translation)**
  - **210Mbps (Translate to 3.3V)**
  - **140Mbps (Translate to 2.5V)**
  - **75Mbps (Translate to 1.8V)**
- **Outputs in High-Impedance State when V_{CCA} or V_{CCB} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green MSOP-8, XTDFN-1.35×1-8L and VSSOP-8 Packages**

APPLICATIONS

Personal Electronic Devices
Industrial and Enterprise Devices
Telecommunications

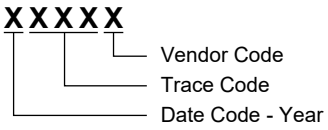
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC2T45	MSOP-8	-40℃ to +125℃	74LVC2T45XMS8G/TR	GJX XMS8 XXXXX	Tape and Reel, 4000
	XTDFN-1.35×1-8L	-40℃ to +125℃	74LVC2T45XXET8G/TR	4PX	Tape and Reel, 5000
	VSSOP-8	-40℃ to +125℃	74LVC2T45XVS8G/TR	2FQ XXXX	Tape and Reel, 3000

MARKING INFORMATION

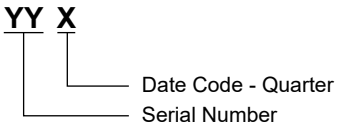
MSOP-8

(1) XXXXX = Date Code, Trace Code and Vendor Code.



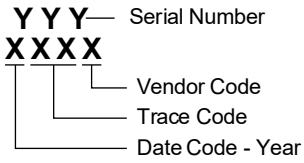
XTDFN-1.35×1-8L

(2) X = Date Code.



VSSOP-8

(3) XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CCA} ..... -0.5V to 6.5V
Supply Voltage Range, V_{CCB} ..... -0.5V to 6.5V
Input Voltage Range, V_I (1) ..... -0.5V to 6.5V
Output Voltage Range, V_O (1)
High-Impedance State ..... -0.5V to 6.5V
High-State or Low-State
A Ports ..... -0.5V to MIN(6.5V, V_{CCA} + 0.5V)
B Ports ..... -0.5V to MIN(6.5V, V_{CCB} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V) ..... -50mA
Output Clamp Current, I_{OK} (V_O < 0V) ..... -50mA
Continuous Output Current, I_O ..... ±50mA
Continuous Current through $V_{CCA/B}$ or GND ..... ±100mA
Junction Temperature (2) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CCA} ..... 1.65V to 5.5V
Supply Voltage Range, V_{CCB} ..... 1.65V to 5.5V
Input Voltage Range, V_I ..... 0V to 5.5V
Output Voltage Range, V_O
High-Impedance State ..... 0V to 5.5V
High-State or Low-State
A Ports ..... 0V to V_{CCA}
B Ports ..... 0V to V_{CCB}
Input Transition Rise or Fall Rate, Δt/ΔV
Data Inputs
V_{CCI} = 1.65V to 1.95V ..... 20ns/V (MAX)
V_{CCI} = 2.3V to 2.7V ..... 20ns/V (MAX)
V_{CCI} = 3.0V to 3.6V ..... 10ns/V (MAX)
V_{CCI} = 4.5V to 5.5V ..... 5ns/V (MAX)
Control Input
V_{CCI} = 1.65V to 5.5V ..... 5ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

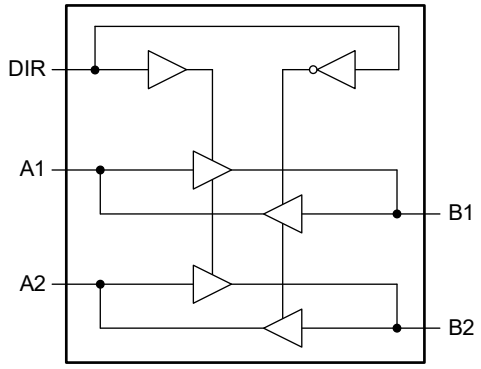
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

LOGIC DIAGRAM



FUNCTION TABLE

SUPPLY VOLTAGE	CONTROL INPUT	INPUT/OUTPUT (1)	
V_{CCA}, V_{CCB}	DIR (2)	An	Bn
1.65V to 5.5V	L	An = Bn	Input
1.65V to 5.5V	H	Input	Bn = An
GND (3)	*X*	Z	Z

H = High Voltage Level

L = Low Voltage Level

Z = High-Impedance State

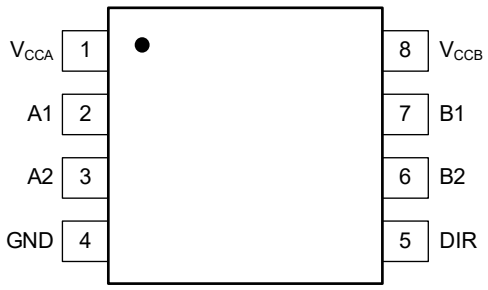
X = Don't Care

NOTES:

1. The input circuit of the data I/O is always active.
2. The DIR input circuit is referenced to $V_{CCA.}$
3. If at least one of V_{CCA} or V_{CCB} is at GND level, the outputs in high-impedance state.

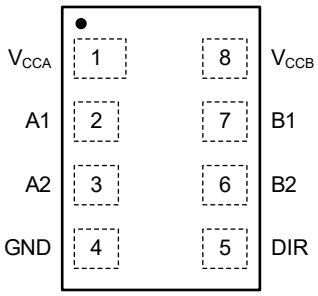
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-8/VSSOP-8

(TOP VIEW)



XTDFN-1.35×1-8L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{CCA}	Supply Voltage on A Ports.
2	A1	Input/Output. It tracks the V_{CCA} supply.
3	A2	Input/Output. It tracks the V_{CCA} supply.
4	GND	Ground.
5	DIR	Direction Control Input. It tracks the V_{CCA} supply.
6	B2	Input/Output. It tracks the V_{CCB} supply.
7	B1	Input/Output. It tracks the V_{CCB} supply.
8	V_{CCB}	Supply Voltage on B Ports.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃. V_{CCI} is the supply voltage associated with the data input ports. V_{CCO} is the supply voltage associated with the data output ports, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CCA}			Full	1.65		5.5	V
	V_{CCB}			Full	1.65		5.5	
High-Level Input Voltage	V_{IH}	Data and DIR inputs	V_{CCI} = 1.65V to 1.95V	Full	0.65 × V_{CCI}			V
			V_{CCI} = 2.3V to 2.7V	Full	1.7			
			V_{CCI} = 3.0V to 3.6V	Full	2.0			
			V_{CCI} = 4.5V to 5.5V	Full	0.7 × V_{CCI}			
Low-Level Input Voltage	V_{IL}	Data and DIR inputs	V_{CCI} = 1.65V to 1.95V	Full			0.35 × V_{CCI}	V
			V_{CCI} = 2.3V to 2.7V	Full			0.7	
			V_{CCI} = 3.0V to 3.6V	Full			0.8	
			V_{CCI} = 4.5V to 5.5V	Full			0.3 × V_{CCI}	
High-Level Output Voltage	V_{OH}	V_I = V_{IH}	V_{CCO} = 1.65V to 4.5V, I_{OH} = -100μA	Full	V_{CCO} - 0.03	V_{CCO} - 0.01		V
			V_{CCO} = 1.65V, I_{OH} = -4mA	Full	1.37	1.53		
			V_{CCO} = 2.3V, I_{OH} = -8mA	Full	2.00	2.17		
			V_{CCO} = 3.0V, I_{OH} = -24mA	Full	2.44	2.69		
			V_{CCO} = 4.5V, I_{OH} = -32mA	Full	3.98	4.20		
			V_{CCO} = 5.5V, I_{OH} = -32mA	Full	5.04	5.23		
Low-Level Output Voltage	V_{OL}	V_I = V_{IL}	V_{CCO} = 1.65V to 4.5V, I_{OL} = 100μA	Full		0.01	0.03	V
			V_{CCO} = 1.65V, I_{OL} = 4mA	Full		0.07	0.24	
			V_{CCO} = 2.3V, I_{OL} = 8mA	Full		0.10	0.25	
			V_{CCO} = 3.0V, I_{OL} = 24mA	Full		0.25	0.45	
			V_{CCO} = 4.5V, I_{OL} = 32mA	Full		0.28	0.50	
			V_{CCO} = 5.5V, I_{OL} = 32mA	Full		0.27	0.47	
Input Leakage Current	I_I	V_I = V_{CCA} or GND, V_{CCA} = V_{CCB} = 1.65V to 5.5V		Full		±0.01	±1	μA
Power-Off Leakage Current	I_{OFF}	V_I or V_O = 0V to 5.5V	A ports, V_{CCA} = 0V, V_{CCB} = 0V to 5.5V	Full		±0.01	±1	μA
			B ports, V_{CCB} = 0V, V_{CCA} = 0V to 5.5V	Full		±0.01	±1	
Off-State Output Current (1)	I_{OZ}	V_{CCA} = V_{CCB} = 1.65V to 5.5V, V_O = V_{CCO} or GND		Full		±0.01	±1	μA
Supply Current	I_{CCA}	V_I = V_{CCI} or GND, I_O = 0A	V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	2	μA
			V_{CCA} = 5V, V_{CCB} = 0V	Full		0.01	2	
			V_{CCA} = 0V, V_{CCB} = 5V	Full	-2	-0.01		
	I_{CCB}	V_I = V_{CCI} or GND, I_O = 0A	V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	2	
			V_{CCA} = 5V, V_{CCB} = 0V	Full	-2	-0.01		
			V_{CCA} = 0V, V_{CCB} = 5V	Full		0.01	2	
	I_{CCA} + I_{CCB}	V_I = V_{CCI} or GND, I_O = 0A	V_{CCA} = V_{CCB} = 1.65V to 5.5V	Full		0.4	4	
Additional Supply Current	ΔI_{CCA}	A ports at V_{CCA} - 0.6V, DIR at V_{CCA}, B ports = open, V_{CCA} = V_{CCB} = 3.0V to 5.5V		Full		0.2	10	μA
		DIR at V_{CCA} - 0.6V, A ports at V_{CCA} or GND, B ports = open, V_{CCA} = V_{CCB} = 3.0V to 5.5V		Full		0.2	10	
	ΔI_{CCB}	B ports at V_{CCB} - 0.6V, DIR at GND, A ports = open, V_{CCA} = V_{CCB} = 3.0V to 5.5V		Full		0.2	10	
Input Capacitance	C_I	DIR input, V_{CCA} = V_{CCB} = 3.3V, V_I = V_{CCA} or GND		+25℃		4		pF
Input/Output Capacitance	$C_{I/O}$	A or B ports, V_{CCA} = V_{CCB} = 3.3V, V_O = $V_{CCA/B}$ or GND		+25℃		5		pF

NOTE: 1. For I/O ports, the parameter I_{OZ} includes the input leakage current.

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	V_{CCB}												UNITS
			1.8V ± 0.15V			2.5V ± 0.2V			3.3V ± 0.3V			5V ± 0.5V			
			MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	
V_{CCA} = 1.8V ± 0.15V															
Propagation Delay	t_{PLH}	An to Bn	1.5	6	13	1	4.5	9	1	4	7.5	1	4	7	ns
	t_{PHL}		1.5	6	13	1	4.5	8.5	1	4	7.5	1	4	7	
	t_{PLH}	Bn to An	1.5	6	13	1	5	12	1	5	11.5	1	5	11	
	t_{PHL}		1.5	6	13	1	5	12	1	5	11.5	1	5	11.5	
Disable Time	t_{PHZ}	DIR to An	3	10.5	16	3	10.5	16	3	10.5	16	3	10.5	16	ns
	t_{PLZ}		2.5	7	11.5	2.5	7.5	11.5	2.5	7	12	2.5	8.5	13	
	t_{PHZ}	DIR to Bn	3	14	22	2.5	9	14	2.5	6	11	2.5	5.5	9	
	t_{PLZ}		3	10	17	2	6	11	2.5	6.5	10	2	5	8	
Enable Time (2)	t_{PZH}	DIR to An		16	30		11	23		11.5	21.5		10	19	ns
	t_{PZL}			20	35		14	26		11	22.5		10.5	20.5	
	t_{PZH}	DIR to Bn		13	24.5		12	20.5		11	19.5		12.5	20	
	t_{PZL}			16.5	29		15	24.5		14.5	23.5		14.5	23	
V_{CCA} = 2.5V ± 0.2V															
Propagation Delay	t_{PLH}	An to Bn	1	5	12	1	3.5	7.5	1	3	6	0.7	3	5.5	ns
	t_{PHL}		1	5	12	1	3.5	7.5	1	3	6	0.7	3	5.5	
	t_{PLH}	Bn to An	1	4.5	9	1	3.5	7.5	1	3.5	7	1	3.5	7	
	t_{PHL}		1	4.5	8.5	1	3.5	7.5	1	3.5	7	0.9	3.5	7	
Disable Time	t_{PHZ}	DIR to An	2	7	10	2	7	10	2	7	10	2	7.5	11	ns
	t_{PLZ}		1.5	3.5	8	1.5	3.5	8	1.5	3.5	8	1.5	4	8	
	t_{PHZ}	DIR to Bn	3.5	12.5	20.5	2.5	7.5	12	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	9	16	2	5	10	2.5	5.5	9	2	4	7	
Enable Time (2)	t_{PZH}	DIR to An		13.5	25		8.5	17.5		9	16		7.5	14	ns
	t_{PZL}			17	29		11	19.5		8.5	17		7.5	14.5	
	t_{PZH}	DIR to Bn		8.5	20		7	15.5		6.5	14		7	13.5	
	t_{PZL}			12	22		10.5	17.5		10	16		10.5	16.5	

NOTES:

1. Specified by design and characterization, not production tested.

2. The enable time value is calculated. Calculate the enable times for the 74LVC2T45 using the following formulas:

• t_{PZH} (DIR to An) = t_{PLZ} (DIR to Bn) + t_{PLH} (Bn to An)

• t_{PZL} (DIR to An) = t_{PHZ} (DIR to Bn) + t_{PHL} (Bn to An)

• t_{PZH} (DIR to Bn) = t_{PLZ} (DIR to An) + t_{PLH} (An to Bn)

• t_{PZL} (DIR to Bn) = t_{PHZ} (DIR to An) + t_{PHL} (An to Bn)

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	V_{CCB}												UNITS
			1.8V ± 0.15V			2.5V ± 0.2V			3.3V ± 0.3V			5V ± 0.5V			
			MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	MIN (1)	TYP	MAX (1)	
V_{CCA} = 3.3V ± 0.3V															
Propagation Delay	t_{PLH}	An to Bn	1	5	11.5	1	3.5	7	0.7	3	5.5	0.7	2.5	5	ns
	t_{PHL}		1	5	11.5	1	3.5	7	0.8	3	5.5	0.7	2.5	5	
	t_{PLH}	Bn to An	1	4	7.5	1	3	6	0.7	3	5.5	0.6	3	5.5	
	t_{PHL}		1	4	7.5	1	3	6	0.8	3	5.5	0.7	3	5.5	
Disable Time	t_{PHZ}	DIR to An	2	4	8.5	2	4	8.5	2	4	8.5	2	4	8.5	ns
	t_{PLZ}		1.5	3.5	8	1.5	3.5	8	1.5	4	8	1.5	4	8	
	t_{PHZ}	DIR to Bn	3.5	12.5	20	2.5	8	12	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	8	15.5	2	4.5	10	2	5.5	8.5	1.5	3.5	7.5	
Enable Time (2)	t_{PZH}	DIR to An		12	23		7.5	16		8.5	14		6.5	13	ns
	t_{PZL}			16.5	27.5		11	18		8	15.5		7	13	
	t_{PZH}	DIR to Bn		8.5	19.5		7	15		7	13.5		6.5	13	
	t_{PZL}			9	20		7.5	15.5		7	14		6.5	13.5	
V_{CCA} = 5V ± 0.5V															
Propagation Delay	t_{PLH}	An to Bn	1	5	11	1	3.5	7	0.6	3	5.5	0.5	2.5	5	ns
	t_{PHL}		1	5	11.5	0.9	3.5	7	0.7	3	5.5	0.5	2.5	4.5	
	t_{PLH}	Bn to An	1	4	7	0.7	3	5.5	0.7	2.5	5	0.5	2.5	5	
	t_{PHL}		1	4	7	0.7	3	5.5	0.7	2.5	5	0.5	2.5	4.5	
Disable Time	t_{PHZ}	DIR to An	1.5	4	6.5	1.5	4	6.5	1.5	4	6.5	1.5	4	7	ns
	t_{PLZ}		1	3	5.5	1	3	5.5	1	3	5.5	1	3	5.5	
	t_{PHZ}	DIR to Bn	3.5	12	19.5	2.5	8	12.5	2.5	5	10	2	4	7.5	
	t_{PLZ}		3	9.5	16	2	5.5	9	2	5.5	8.5	1.5	3.5	6	
Enable Time (2)	t_{PZH}	DIR to An		13.5	23		8.5	14.5		8	13.5		6	11	ns
	t_{PZL}			16	26.5		11	18		7.5	15		6.5	12	
	t_{PZH}	DIR to Bn		8	16.5		6.5	12.5		6	11		5.5	10.5	
	t_{PZL}			9	18		7.5	13.5		7	12		6.5	11.5	

NOTES:

1. Specified by design and characterization, not production tested.

2. The enable time value is calculated. Calculate the enable times for the 74LVC2T45 using the following formulas:

• t_{PZH} (DIR to An) = t_{PLZ} (DIR to Bn) + t_{PLH} (Bn to An)

• t_{PZL} (DIR to An) = t_{PHZ} (DIR to Bn) + t_{PHL} (Bn to An)

• t_{PZH} (DIR to Bn) = t_{PLZ} (DIR to An) + t_{PLH} (An to Bn)

• t_{PZL} (DIR to Bn) = t_{PHZ} (DIR to An) + t_{PHL} (An to Bn)

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	V_{CCA} = V_{CCB} = 5V	UNITS
				TYP	TYP	TYP	TYP	
Power Dissipation Capacitance (1)	C_{PDA}	C_L = 0pF, f = 10MHz, t_R = t_F = 1ns	A port inputs, B port outputs	3	3	4	5	pF
			B port inputs, A port outputs	19	20	21	22	
	C_{PDB}	C_L = 0pF, f = 10MHz, t_R = t_F = 1ns	A port inputs, B port outputs	19	20	21	22	pF
			B port inputs, A port outputs	3	3	4	5	

NOTE:

1. Power dissipation capacitance per transceiver. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$

   where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

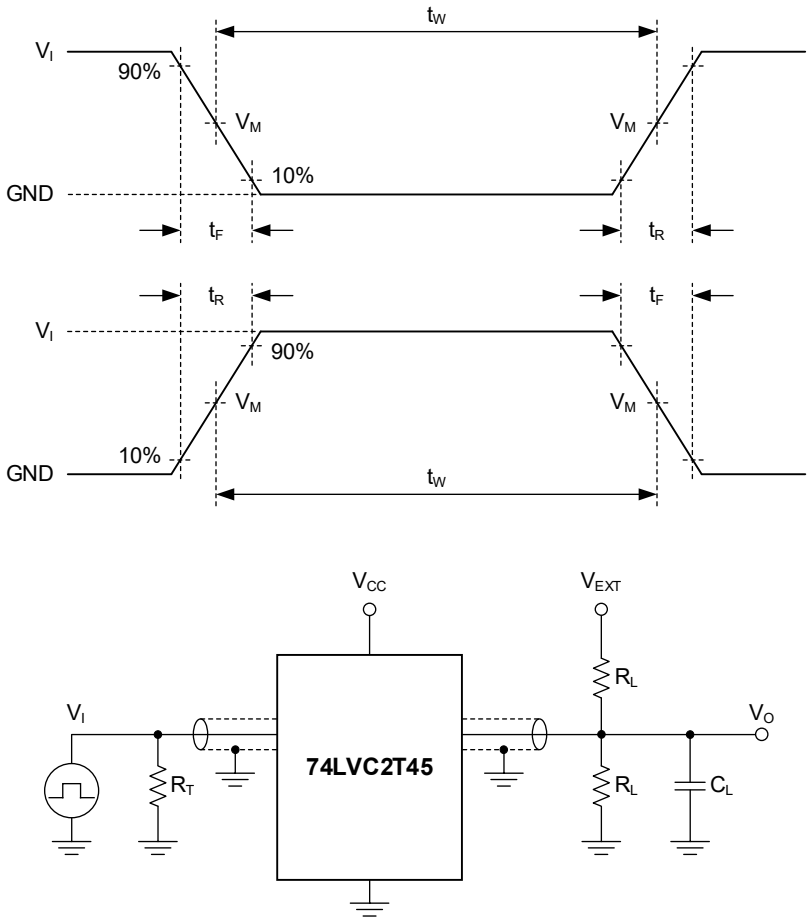
   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in Volts.

   N = number of inputs switching.

   $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

V_{EXT}: External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

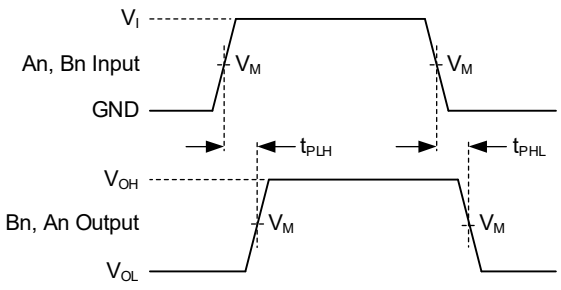
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CCA}, V_{CCB}	V_I (1)	t_R, t_F	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL} (2)	t_{PLH}, t_{PHL}
1.65V to 5.5V	V_{CCI}	≤ 2.5ns	15pF	2kΩ	GND	2 × V_{CCO}	Open

NOTES:

1. V_{CCI} is the supply voltage related to the data input ports.

2. V_{CCO} is the supply voltage related to the data output ports.

WAVEFORMS

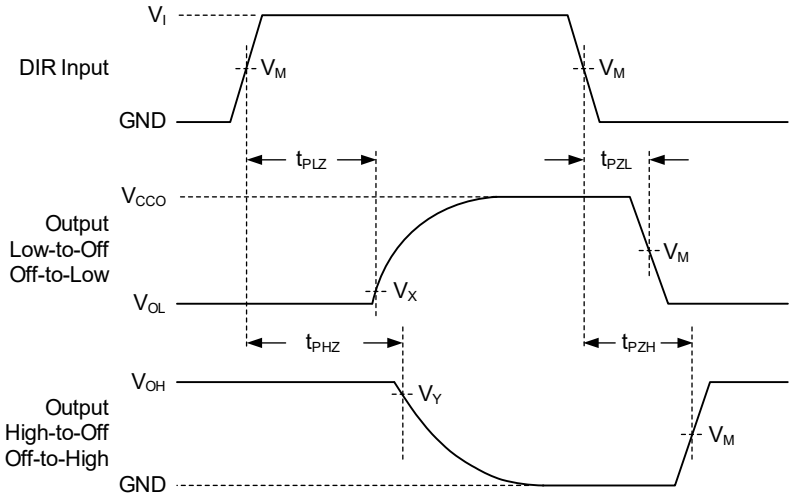


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (An, Bn) to Output (Bn, An) Propagation Delay Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CCA}, V_{CCB}	V_I (1)	V_M (2)	V_M (3)	V_X	V_Y
1.65V to 2.7V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15V	V_{OH} - 0.15V
3.0V to 5.5V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTES:

1. V_{CCI} is the supply voltage related to the data input ports.

2. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

3. V_{CCO} is the supply voltage related to the data output ports.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

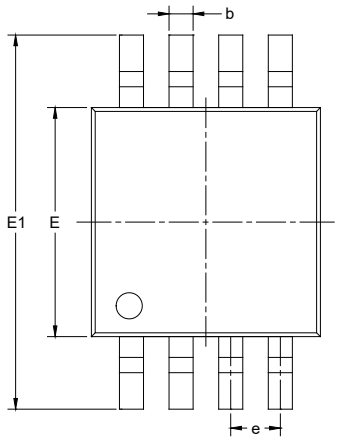
MARCH 2026 – REV.A.1 to REV.A.2	Page
Updated Features section	1
Added VSSOP-8 package	All
Updated Package Outline Dimensions	12

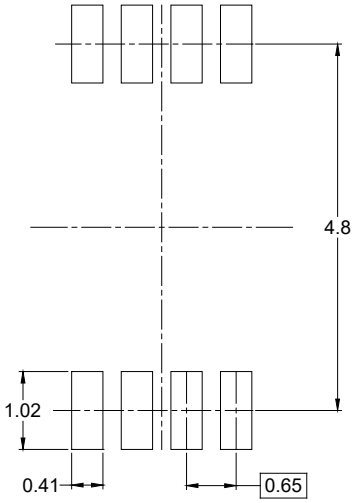
JANUARY 2023 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	5

Changes from Original (JUNE 2022) to REV.A	Page
Changed from product preview to production data	All

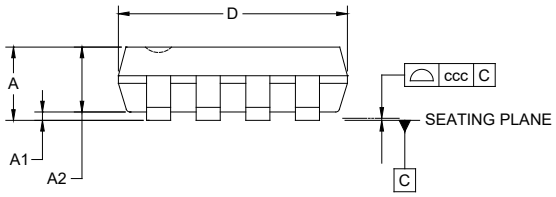
PACKAGE OUTLINE DIMENSIONS

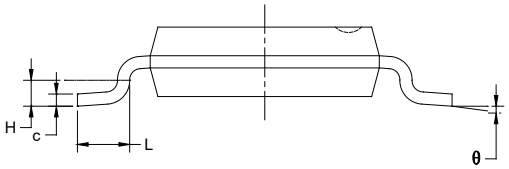
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



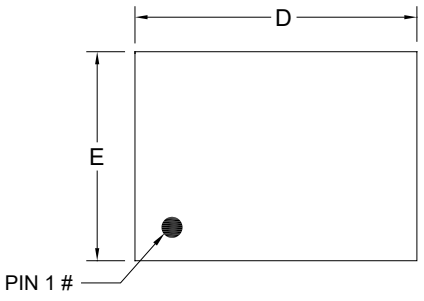


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.220	-	0.380
c	0.080	-	0.230
D	2.800	-	3.200
E	2.800	-	3.200
E1	4.650	-	5.150
e	0.650 BSC		
L	0.400	-	0.800
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

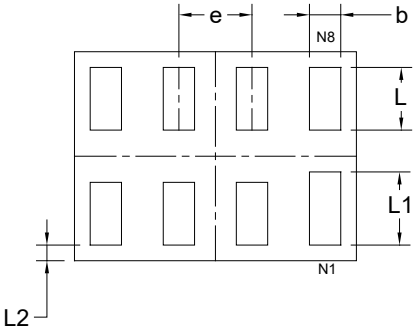
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

PACKAGE OUTLINE DIMENSIONS

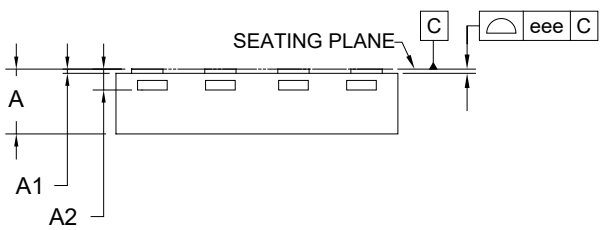
XTDFN-1.35×1-8L



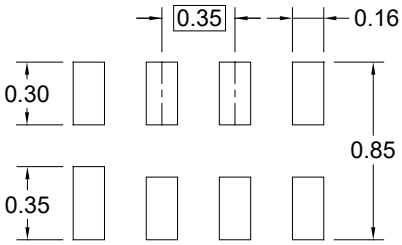
TOP VIEW



BOTTOM VIEW



SIDE VIEW



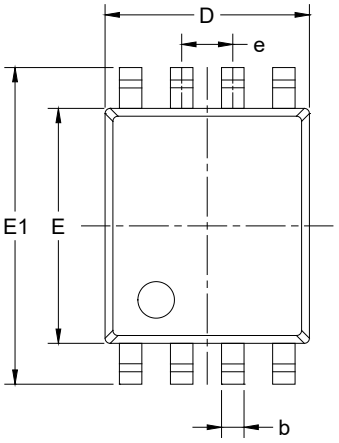
RECOMMENDED LAND PATTERN (Unit: mm)

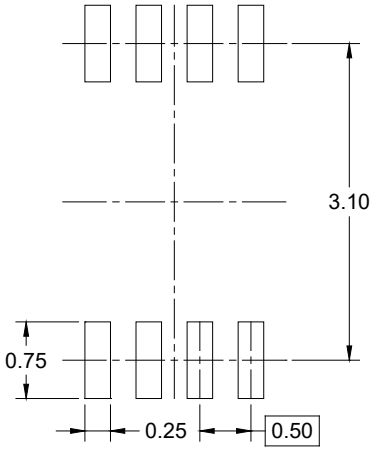
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	0.310	0.330
A1	0.000	-	0.050
A2	0.100 REF		
D	1.250	1.350	1.450
E	0.900	1.000	1.100
b	0.110	0.160	0.210
e	0.350 BSC		
L	0.250	0.300	0.350
L1	0.300	0.350	0.400
L2	0.075 REF		
eee	-	0.050	-

NOTE: This drawing is subject to change without notice.

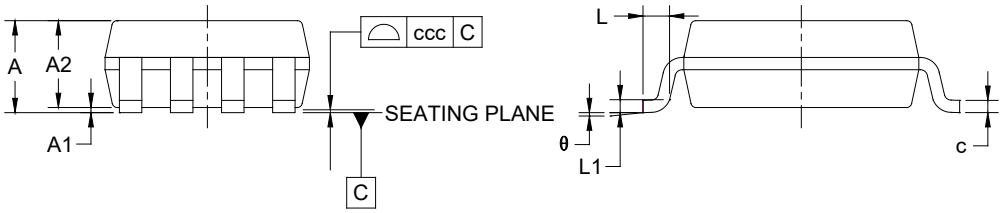
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

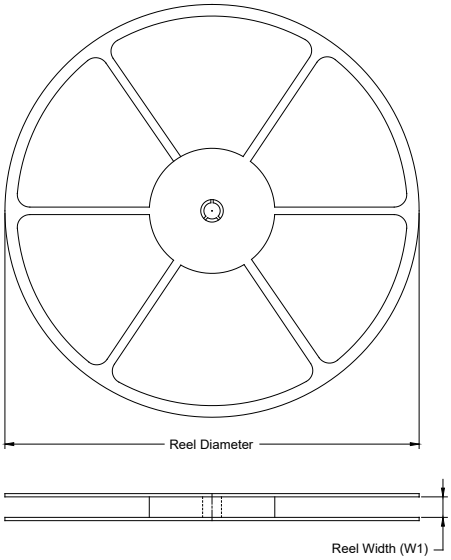


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

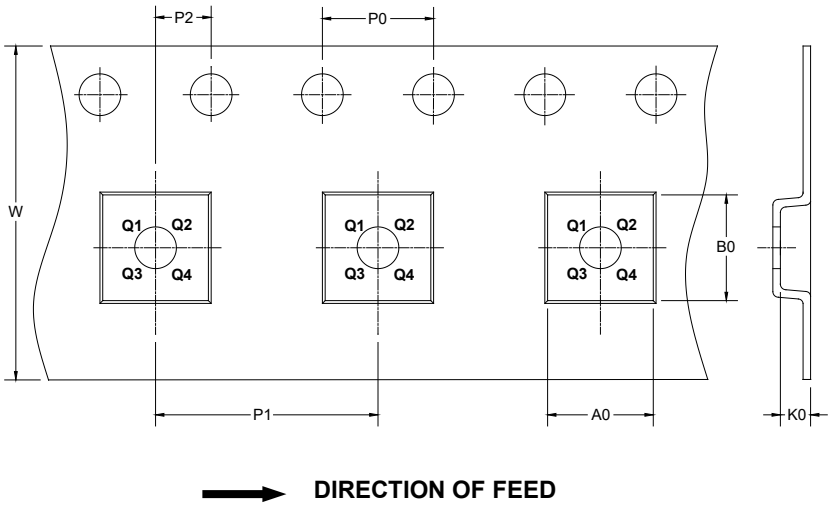
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



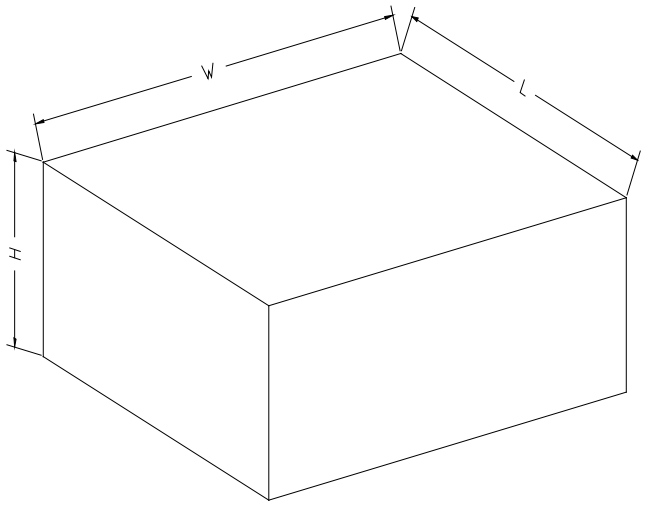
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
XTDFN-1.35×1-8L	7″	9.5	1.21	1.51	0.39	4.0	4.0	2.0	8.0	Q1
VSSOP-8	7"	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002