SGM40571
1A, Single-Input, Single-Cell Li-Ion and Li-Poly Battery Charger

GENERAL DESCRIPTION

The SGM40571 is a 1A linear battery charger that it can charge single-cell Li-Ion or Li-polymer battery in a wide input voltage range from smart wall adapter or USB device. The high input voltage range with input over-voltage protection supports charging by an unregulated adapter.

This chip indeed allows the simultaneous connection of the system and battery to the output port. To ensure that the battery is fully charged within the 12-hour safety timer, the average system load must be carefully managed.

The charging process involves three stages:

1. Pre-charge stage: A small pre-charge current activates the low-voltage battery to enable constant-current fast charging.
2. Constant-current stage: the battery is charged at a constant-current.
3. Constant-voltage stage: the battery is charged at a constant-voltage until it reaches full-charge.

Additionally, the SGM40571 includes the internal thermal regulation and the over-temperature protection (OTP) to ensure safe charging.

The SGM40571 allows the charging process to be customized with the external resistors:

- Fast charge current: set by an external resistor.
- Pre-charge current and termination current: adjustable by changing external resistor.

Additionally, the SGM40571 integrates JEITA control to optimize charging based on the battery temperature, which can be monitored by using an NTC resistor.

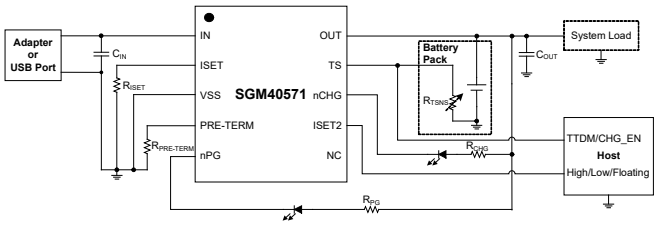
FEATURES

- **Multi-Chemistry Voltage Support: 4.2V, 4.35V and 4.4V**
- **0.8% Charge Voltage Accuracy and 10% Charge Current Accuracy**
- **USB Input Current Limit: 100mA and 500mA**
- **Programmable Termination and Pre-Charge Threshold**
- **Input Rating Voltage: 30V**
- **Input Over-Voltage Protection Threshold: 6.6V or 7.1V**
- **Input Voltage Dynamic Power Management**
- **Thermal Shutdown Protection: 155℃**
- **Thermal Regulation: 125℃**
- **Support ISET Short Detection and OUT Short-Circuit Protection**
- **Safety Timer: 12h**
- **Support Power Good and Charge Status Indication**
- **Automatic Termination and Timer Disable Mode (TTDM)**
- **Available in a Green TDFN-2×2-10L Package**

APPLICATIONS

Smart Watch and Wristband
Wireless Speaker
TWS Headset and Headphone
Portable Medical Equipment
Mobile POS

SIMPLIFIED SCHEMATIC

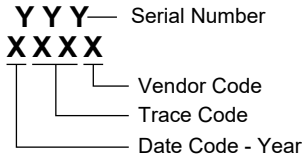


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40571-426AEJMF	TDFN-2×2-10L	-40℃ to +85℃	SGM40571-426AEJMFYTHN10G/TR	2C8 XXXX	Tape and Reel, 3000
SGM40571-436AEJMF	TDFN-2×2-10L	-40℃ to +85℃	SGM40571-436AEJMFYTHN10G/TR	2C9 XXXX	Tape and Reel, 3000
SGM40571-446AEJNF	TDFN-2×2-10L	-40℃ to +85℃	SGM40571-446AEJNFYTHN10G/TR	2CA XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with Respect to V_{SS})
- IN ..... -0.3V to 30V
- OUT ..... -0.3V to 6V
- PRE-TERM, ISET, ISET2, TS, nCHG, nPG..... -0.3V to 6V

Input Current, IN ..... 1.25A (MAX)
Output Current (Continuous), OUT ..... 1.25A (MAX)
Output Sink Current, nCHG, nPG ..... 15mA (MAX)
Package Thermal Resistance
- TDFN-2×2-10L, θ_{JA} ..... 68.6℃/W
- TDFN-2×2-10L, θ_{JB} ..... 31.6℃/W
- TDFN-2×2-10L, $\theta_{JC\ (TOP)}$ ..... 69.5℃/W
- TDFN-2×2-10L, $\theta_{JC\ (BOT)}$ ..... 5℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±2000V

NOTES:
1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS (1)

IN Voltage Range, V_{IN} ..... 3.5V to 28V
IN Operating Voltage Range, Restricted by V_{DPM} and V_{OVP} ..... 4.45V to 6.45V
Input Current, IN Terminal, I_{IN} ..... 1A (MAX)
Current, OUT Terminal, I_{OUT} ..... 1A (MAX)
Programming Pre-Charge and Termination Current Thresholds, $R_{PRE-TERM}$ ..... 1kΩ to 10kΩ
Fast-Charge Current Programming Resistor, R_{ISET} ..... 0.54kΩ to 10.8kΩ
NTC Thermistor Range without Entering TTDM, R_{TS} ..... 1.66kΩ to 258kΩ
NTC Pin Capacitance ..... 120pF (MAX)
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:
1. Operation when the V_{IN} is below 4.5V or in the drop-out condition may lead to a reduction in performance.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

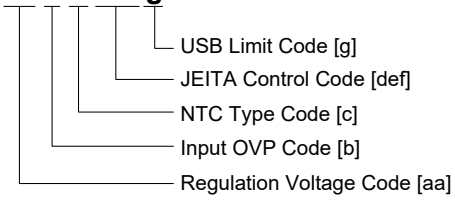
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SUFFIX CODE

Surfix: SGM40571-aa b c def g



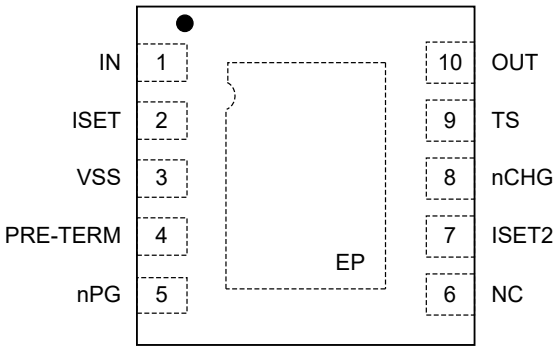
Model: SGM40571-aabcdefg				
Regulation Voltage				
Option Code "**aa**"	**42**	**43**	**44**	
$V_{OUT(REG)}$ (V)	4.2	4.35	4.4	
Input OVP				
Option Code "**b**"	**6**	**7**		
$V_{IN(OVP)}$ (V)	6.6	7.1		
NTC Type				
Option Code "**c**"	**A**	**B**		
NTC Type (kΩ)	10	100		
JEITA Control				
JEITA Enable				
Option Code "**d**"	**D**	**E**		
JEITA Function	Disabled (Codes "e" and "f" are inoperative)	Enabled		
Charge Current Percentage in Cold Operation				
Option Code "**e**"	**H**	**J**	**K**	**L**
Current (%)	20	50	100	N/A
Charge Voltage in Hot Operation				
Option Code "**f**"	**M**	**N**		
Voltage	$V_{OUT(REG)}$ - 150mV	Charge forbidden		
USB Limit				
Option Code "**g**"	**F**	**G**		
USB Input Current Limit When ISET2 = "H" (mA)	500	380		

PRODUCT LIST

Part Number	Package	$V_{OUT(REG)}$ (V)	$V_{IN(OVP)}$ (V)	NTC Type	JEITA Control			USB Limit in ISET2 = "H" (mA)
					JEITA Enable	Cold Operation	Hot Operation	
SGM40571-426AEJMF	TDFN-2×2-10L	4.2	6.6	10kΩ	Enable	50%	$V_{OUT(REG)}$ - 150mV	500
SGM40571-436AEJMF	TDFN-2×2-10L	4.35	6.6	10kΩ	Enable	50%	$V_{OUT(REG)}$ - 150mV	500
SGM40571-446AEJNF	TDFN-2×2-10L	4.4	6.6	10kΩ	Enable	50%	Charge forbidden	500
SGM40572-426AEJMF	MSOP-10 (Exposed Pad)	4.2	6.6	10kΩ	Enable	50%	$V_{OUT(REG)}$ - 150mV	500
SGM40572-426ADKNF	MSOP-10 (Exposed Pad)	4.2	6.6	10kΩ	Disable	100%	Charge forbidden	500
SGM40572-426BEJMF	MSOP-10 (Exposed Pad)	4.2	6.6	100kΩ	Enable	50%	$V_{OUT(REG)}$ - 150mV	500
SGM40572-426BDKNF	MSOP-10 (Exposed Pad)	4.2	6.6	100kΩ	Disable	100%	Charge forbidden	500
SGM40572-436ADKNF	MSOP-10 (Exposed Pad)	4.35	6.6	10kΩ	Disable	100%	Charge forbidden	500
SGM40572-446AEJMF	MSOP-10 (Exposed Pad)	4.4	6.6	10kΩ	Enable	50%	$V_{OUT(REG)}$ - 150mV	500

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	IN	P	Charge Power Input, for Powering this Device and Feeding to the Charge Output. The capacitor capacitance in the range of 1μF to 10μF is recommended. It should be placed close to this pin for decoupling.
2	ISET	AI	Fast-Charge Current Setting Pin.
3	VSS	–	Ground Pin of the Device.
4	PRE-TERM	AI	Program Current Termination Threshold and Pre-Charge Current. Set the ratio of pre-charge and termination current to the fast-charge current.
5	nPG	DO	Active low. Indicates V_{IN} status, V_{IN} > $V_{UVLO(RISE)}$, exit sleep mode and no input over-voltage occurs.
6	NC	–	No Connection.
7	ISET2	AI	Input/Output Current Limit Setting Pin for USB or Adaptor Source.
8	nCHG	DO	During charging: low (FET on). Charge completed or no charging: open-drain (FET off).
9	TS	AI	Battery Pack Temperature Sense Terminal. If the battery pack temperature sense function is not expected, a 10kΩ resistor may need to be externally connected to the TS pin.
10	OUT	P	Battery Connection Pin. The battery connection pin supports direct attachment of system loads. External bypass capacitors within the 1μF to 10μF range are required for stable operation.
Exposed Pad	EP	–	Thermal Pad and Ground Reference. Connect the exposed thermal pad to both the VSS pin and the main ground plane. Ensure the thermal pad shares the same electrical potential as VSS. Note that the thermal pad must not serve as the primary ground input.

NOTE: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input							
Under-Voltage Lockout Exit	$V_{UVLO(RISE)}$	V_{IN}: 0V → 4V		3.15	3.27	3.4	V
Under-Voltage Lockout Hysteresis	$V_{HYS(UVLO)}$	V_{IN}: 4V → 0V, $V_{UVLO(FALL)} = V_{UVLO(RISE)} - V_{HYS(UVLO)}$		195	250	305	mV
Input Power Good Detection Threshold is $V_{OUT} + V_{IN(DT)}$	$V_{IN(DT)}$	Input power good if $V_{IN} > V_{OUT} + V_{IN(DT)}$, V_{OUT} = 3.6V, V_{IN}: 3.5V → 4V			90		mV
Hysteresis on $V_{IN(DT)}$ Falling	$V_{HYS(INDT)}$	V_{OUT} = 3.6V, V_{IN}: 4V → 3.5V			30		mV
Input Over-Voltage Protection Threshold	V_{OVP}	V_{IN}: 5V → 12V	SGM40571-xx6xxxx	6.40	6.56	6.72	V
			SGM40571-xx7xxxx	6.89	7.06	7.24	
Hysteresis on OVP	$V_{HYS(OVP)}$	V_{IN}: 11V → 5V			130		mV
USB/Adaptor Low Input Voltage Protection (Restricts I_{OUT} at V_{IN-DPM})	V_{IN-DPM}	Feature active in USB mode, limit input source current to 50mA, V_{OUT} = 3.5V, R_{ISET} = 825Ω,	$V_{OUT(REG\_TYP)}$ = 4.35V\4.4V	4.37	4.50	4.63	V
			$V_{OUT(REG\_TYP)}$ = 4.2V	4.20	4.34	4.47	
		Feature active in adaptor mode, limit input source current to 50mA, V_{OUT} = 3.5V, R_{ISET} = 825Ω	$V_{OUT(REG\_TYP)}$ = 4.35V\4.4V	4.37	4.50	4.63	
			$V_{OUT(REG\_TYP)}$ = 4.2V	4.12	4.24	4.37	
USB Input I-Limit 100mA	$I_{IN-USB-CL}$	ISET2 = floating, R_{ISET} = 825Ω, 0℃ < T_J < +85℃		77	90	100	mA
USB Input I-Limit 500mA		ISET2 = high, R_{ISET} = 825Ω		425	454	500	
USB input I-Limit 380mA		ISET2 = high, R_{ISET} = 825Ω		330	369	405	
ISET Short-Circuit Test							
Highest Resistor Value Considered a Fault (Short), Monitored for I_{OUT} > 90mA	$R_{ISET(SHORT)}$	R_{ISET}: 540Ω → 250Ω, I_{OUT} latches off cycle power to reset		289		490	Ω
Maximum OUT Current Limit Regulation (Clamp)	$I_{OUT(CL)}$	V_{IN} = 5V, V_{OUT} = 3.6V, V_{ISET2} = low, R_{ISET}: 540Ω → 250Ω, I_{OUT} latches off after t_{DGL_SHORT}		1.07		1.55	A
Battery Short Protection							
OUT Terminal Short-Circuit Detection Threshold	$V_{OUT(SC)}$	V_{OUT}: 3V → 0.5V, no deglitch		0.77	0.8	0.82	V
OUT Terminal Short Hysteresis	$V_{OUT(SC-HYS)}$	Recovery ≥ $V_{OUT(SC)} + V_{OUT(SC-HYS)}$, rising, no deglitch			69		mV
Source Current to OUT Terminal during Short-Circuit Detection	$I_{OUT(SC)}$	V_{OUT} < 0.8V			13		mA
Quiescent Current							
Battery Current into OUT Terminal	$I_{OUT(PDWN)}$	V_{IN} = 0V				1	μA
OUT Terminal Current, Charging Terminated	$I_{OUT(DONE)}$	V_{IN} = 6V, V_{OUT} > $V_{OUT(REG)}$				6	μA
Standby Current into IN Terminal	$I_{IN(STDBY)}$	TS = low, V_{IN} ≤ 6V				310	μA
Active Supply Current, IN Terminal	I_{CC}	TS = open, V_{IN} = 6V, TTDM - no load on OUT terminal, V_{OUT} > $V_{OUT(REG)}$, IC enabled			0.7	1	mA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Battery Charger Fast-Charge								
Battery Regulation Voltage	$V_{OUT(REG)}$	V_{IN} = 5.5V	SGM40571-42xxxxxx	T_J = -40℃ to +125℃	4170	4200	4233	mV
				T_J = +25℃	4184	4200	4221	
			SGM40571-43xxxxxx	T_J = -40℃ to +125℃	4317	4348	4382	
				T_J = +25℃	4330	4348	4370	
			SGM40571-44xxxxxx	T_J = -40℃ to +125℃	4366	4397	4427	
				T_J = +25℃	4380	4397	4418	
Battery Hot Regulation Voltage	$V_{O\_HT(REG)}$	V_{IN} = 5.5V	SGM40571-42xxxxxx	T_J = -40℃ to +125℃	4032	4060	4092	mV
				T_J = +25℃	4045	4060	4081	
			SGM40571-43xxxxxx	T_J = -40℃ to +125℃	4173	4203	4236	
				T_J = +25℃	4185	4203	4225	
			SGM40571-44xxxxxx	T_J = -40℃ to +125℃	4222	4250	4279	
				T_J = +25℃	4235	4250	4270	
Drop-Out, V_{IN} - V_{OUT}	$V_{DO(IN-OUT)}$	Adjust V_{IN} down until I_{OUT} = 0.5A, V_{OUT} = $V_{OUT(REG\_TYP)}$ - 50mV, R_{ISET} = 540Ω, ISET2 = low (adaptor mode)				175	360	mV
Output "Fast Charge" Formula	I_{OUT}	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, ISET2 = low			K_{ISET}/R_{ISET}			A
Fast Charge Current Factor	K_{ISET}	200mA ≤ I_{OUT} < 1000mA			500	540	582	AΩ
		50mA ≤ I_{OUT} < 200mA			380	540	710	
		25mA ≤ I_{OUT} < 50mA			310	544	783	
		10mA < I_{OUT} < 25mA				540		
Pre-Charge - Set by PRE-TERM Terminal for SGM40571								
Pre-Charge to Fast-Charge Transition Threshold	V_{LOWV}				2.4	2.5	2.6	V
	$I_{PRE-TERM}$				See the Termination section			
Pre-Charge Current (Default Setting)	$\%_{PRE-CHG}$	V_{OUT} < V_{LOWV}, R_{ISET} = 1080Ω, $R_{PRE-TERM}$ = High-Z			16	21	26	$\%I_{OUT-CC}$
Pre-Charge Current Formula		$R_{PRE-TERM}$ = $K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)			$R_{PRE-TERM}/K_{PRE-CHG}$ %			
% Pre-Charge Factor	$K_{PRE-CHG}$	V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2kΩ to 10kΩ, R_{ISET} = 1080Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 20% to 100%			90	100	112	Ω/%
		V_{OUT} < V_{LOWV}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1kΩ to 2kΩ, R_{ISET} = 1080Ω, $R_{PRE-TERM}$ = $K_{PRE-CHG}$ × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 20%			71	100	133	
Termination - Set by PRE-TERM Terminal for SGM40571								
Termination Threshold Current (Default Setting)	$\%_{TERM}$	V_{OUT} > V_{RCH}, R_{ISET} = 1kΩ, $R_{PRE-TERM}$ = High-Z			7.6	11	14	$\%I_{OUT-CC}$
Termination Current Threshold Formula		$R_{PRE-TERM}$ = K_{TERM} (Ω/%) × $\%_{TERM}$ (%)			$R_{PRE-TERM}/K_{TERM}$			
% Term Factor	K_{TERM}	V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 2kΩ to 10kΩ, R_{ISET} = 750Ω K_{TERM} × $\%I_{FAST-CHG}$, where $\%I_{FAST-CHG}$ is 10% to 50%			174	200	221	Ω/%
		V_{OUT} > V_{RCH}, V_{IN} = 5V, $R_{PRE-TERM}$ = 1kΩ to 2kΩ, R_{ISET} = 750Ω K_{TERM} × $\%I_{SET}$, where $\%I_{SET}$ is 5% to 10%			119	199	273	
Current for Programming the Term and PRE-CHG with Resistor, $I_{TERM-START}$ is the Initial PRE-TERM Current	$I_{PRE-TERM}$	$R_{PRE-TERM}$ = 2kΩ, V_{OUT} = 4.15V			70	75	80	μA
Termination Current Formula	$\%_{TERM}$				R_{TERM}/K_{TERM} %			

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Termination - Set by PRE-TERM Terminal for SGM40571						
Elevated PRE-TERM Current for, $t_{TERM-START}$, during Start of Charge to Prevent Recharge of Full Battery	$I_{TERM-START}$		79	85	90	μA
Recharge or Refresh						
Recharge Detection Threshold - Normal Temp	V_{RCH}	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: $V_{OUT(REG\_TYP)}$ + 50mV → V_{RCH}	$V_{OUT(REG)}$ - 0.2	$V_{OUT(REG)}$ - 0.13	$V_{OUT(REG)}$ - 0.05	V
Recharge Detection Threshold - Hot Temp		V_{IN} = 5V, V_{TS} = 0.2V, V_{OUT}: $V_{O\_HT(REG\_TYP)}$ + 50mV → V_{RCH}	$V_{O\_HT(REG)}$ - 0.2	$V_{O\_HT(REG)}$ - 0.13	$V_{O\_HT(REG)}$ - 0.04	V
Battery Detect Routine (Note: In Hot Mode $V_{OUT(REG)}$ Becomes $V_{O\_HT(REG)}$)						
VOUT Reduced Regulation During Battery Detect	V_{REG-BD}	V_{IN} = 5V, V_{TS} = 0.5V, battery absent	$V_{OUT(REG)}$ - 0.43	$V_{OUT(REG)}$ - 0.40	$V_{OUT(REG)}$ - 0.34	V
Sink current during V_{REG-BD}	$I_{BD-SINK}$	V_{IN} = 5V, V_{TS} = 0.5V, battery absent	4	8	12	mA
High Battery Detection Threshold	V_{BD-HI}	V_{IN} = 5V, V_{TS} = 0.5V, battery absent	$V_{OUT(REG)}$ - 0.2	$V_{OUT(REG)}$ - 0.13	$V_{OUT(REG)}$ - 0.05	V
Low Battery Detection Threshold	V_{BD-LO}	V_{IN} = 5V, V_{TS} = 0.5V, battery absent	V_{REG-BD} + 0.02	V_{REG-BD} + 0.08	V_{REG-BD} + 0.17	V
Battery-Pack NTC Monitor, TS Terminal: SGM40571: 10kΩ NTC and 100kΩ NTC						
NTC Bias Current	$I_{NTC-100k}$	V_{TS} = 0.3V	3	5	7	μA
	$I_{NTC-10k}$		47	50	54	
NTC Bias Current when Charging is Disabled	$I_{NTC-DIS-100k}$	V_{TS} = 0V	3	5	7	μA
	$I_{NTC-DIS-10k}$		28	31	33	
I_{NTC} is reduced Prior to Entering TTDM to Keep Cold Thermistor from Entering TTDM	$I_{NTC-FLDBK-100k}$	V_{TS}: set to 1.49V		1	3	μA
	$I_{NTC-FLDBK-10k}$	V_{TS}: set to 1.49V		2	9	
Termination and Timer Disable Mode Threshold - Enter	$V_{TTDM(TS)}$	V_{TS}: 0.5V → 1.7V, timer held in reset	1490	1570	1660	mV
Hysteresis Exiting TTDM	$V_{HYS-TTDM(TS)}$	V_{TS}: 1.7V → 0.5V, timer enabled		100		mV
TS Maximum Voltage Clamp	$V_{CLAMP(TS)(NTC-100k)}$	V_{TS} = open (floating)	1585	1725	1865	mV
	$V_{CLAMP(TS)(NTC-10k)}$		1865	2000	2150	
TS Voltage where I_{NTC} is Reduce to Keep Thermistor from Entering TTDM	$V_{TS\_I-FLDBK}$	V_{TS}: 1.4V → 1.49V		1450		mV
Low Temperature CHG Pending	$V_{TS-0℃}$	Low temp charging to pending, V_{TS}: 1V → 1.5V	1140	1202	1260	mV
Hysteresis at 0℃	$V_{HYS-0℃}$	Charge pending to low temp charging, V_{TS}: 1.5V → 1V		123		mV
Low Temperature, Half Charge	$V_{TS-10℃}$	Normal charging to low temp charging, V_{TS}: 0.5V → 1V	730	773	816	mV
Hysteresis at 10℃	$V_{HYS-10℃}$	Low temp charging to normal CHG, V_{TS}: 1V → 0.5V		34		mV
High Temperature at 4.1V	$V_{TS-45℃}$	Normal charging to high temp CHG, V_{TS}: 0.5V → 0.2V	251	276	299	mV
Hysteresis at 45℃	$V_{HYS-45℃}$	High temp charging to normal CHG, V_{TS}: 0.2V → 0.5V		10		mV
High Temperature Disable	$V_{TS-60℃}$	High temp charge to pending, V_{TS}: 0.2V → 0.1V	155	177	198	mV
Hysteresis at 60℃	$V_{HYS-60℃}$	Charge pending to high temp CHG, V_{TS}: 0.1V → 0.2V		10		mV
Charge Enable Threshold (10kΩ NTC)	$V_{TS-EN-10k}$	V_{TS}: 0V → 0.175V	67	87	124	mV
HYS below $V_{TS-EN-10k}$ to Disable (10kΩ NTC)	$V_{TS-DIS\_HYS-10k}$	V_{TS}: 0.125V → 0V		11		mV

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Regulation						
Temperature Regulation Limit	$T_{J(REG)}$			125		℃
Thermal Shutdown Temperature	$T_{J(OFF)}$			155		℃
Thermal Shutdown Hysteresis	$T_{J(OFF-HYS)}$			20		℃
Logic Levels on ISET2						
Logic Low Input Voltage	V_{IL}	Sink 8μA			0.4	V
Logic High Input Voltage	V_{IH}	Source 8μA	1.3			V
Sink Current Required for LO	I_L	V_{ISET2} = 0.4V	3		6.6	μA
Source Current Required for HI	I_H	V_{ISET2} = 1.4V	3.3		7	μA
ISET2 Floating Voltage	V_{FLT}		700	800	910	mV
Logic Levels on nCHG and nPG						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.1	V
Leakage Current into IC	I_{LEAK}	V_{nCHG} = 5V, V_{nPG} = 5V			0.5	μA

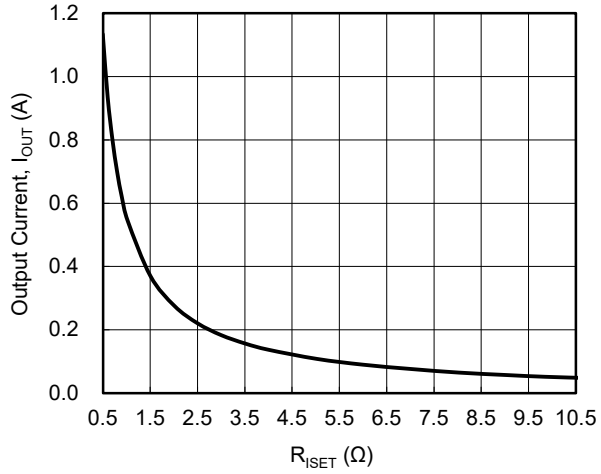
TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Deglitch Time on Exiting Sleep	$t_{DGL(PG\_PWR)}$	Time measured from V_{IN}: 0V → 5V 1μs rise-time to nPG = low, V_{OUT} = 3.6V		45		μs
Deglitch Time on $V_{HYS(INDT)}$ Power-Down, Same as Entering Sleep	$t_{DGL(PG\_NO-PWR)}$	Time measured from V_{IN}: 5V → 3.2V 1μs fall-time to nPG = OC, V_{OUT} = 3.6V		29		ms
Input Over-Voltage Blanking Time	$t_{DGL(OVP-SET)}$	V_{IN}: 5V → 12V		113		μs
Deglitch Time Exiting OVP	$t_{DGL(OVP-REC)}$	Time measured from V_{IN}: 12V → 5V 1μs fall-time to nPG = low		30		μs
ISET Short-Circuit Test						
Deglitch Time Transition from ISET Short to I_{OUT} Disable	t_{DGL_SHORT}	Clear fault by disconnecting IN or cycling (high/low) TS		1		ms
Pre-Charge - Set by PRE-TERM Pin						
Deglitch Time on Pre-Charge to Fast-Charge Transition	$t_{DGL1(LOWV)}$			70		μs
Deglitch Time on Fast-Charge to Pre-Charge Transition	$t_{DGL2(LOWV)}$			32		ms
Termination - Set by PRE-TERM Pin						
Deglitch time, Termination Detected	$t_{DGL(TERM)}$			29		ms
Elevated termination Threshold Initially Active for $t_{TERM-START}$	$t_{TERM-START}$			1.25		min
Recharge or Refresh						
Deglitch Time, Recharge Threshold Detected	$t_{DGL1(RCH)}$	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT}: 4.25V → 3.5V in 1μs, $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
Deglitch Time, Recharge Threshold Detected in OUT-Detect Mode	$t_{DGL2(RCH)}$	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT} = 3.5V inserted, $t_{DGL(RCH)}$ is time to ISET ramp		3.6		ms
Battery Detect Routine (Note: In Hot Mode $V_{OUT(REG)}$ Becomes $V_{O\_HT(REG)}$)						
Regulation Time at V_{REG} or V_{REG-BD}	$t_{DGL(HI/LOW\ REG)}$			25		ms
Battery Charging Timers and Fault Timers						
Pre-Charge Safety Timer Value	t_{PRECHG}	Restarts when entering pre-charge, always enabled when in pre-charge	1790	2080	2370	s
Charge Safety Timer Value	t_{MAXCH}	Clears fault or resets at UVLO, TS disable, OUT short, exiting LOWV and refresh	38270	44400	50530	s
Battery-Pack NTC Monitor, TS Terminal: SGM40571: 10kΩ NTC						
Deglitch Exit TTDM between States	$t_{DGL(TTDM)}$			57		ms
Deglitch Enter TTDM between States				16		μs
Deglitch for TS Thresholds: 10℃	$t_{DGL(TS\_10C)}$	Normal to cold operation, V_{TS}: 0.6V → 1V		50		ms
		Cold to normal operation, V_{TS}: 1V → 0.6V		12		
Deglitch for TS Thresholds: 0℃/45℃/60℃	$t_{DGL(TS)}$	Battery charging		30		ms

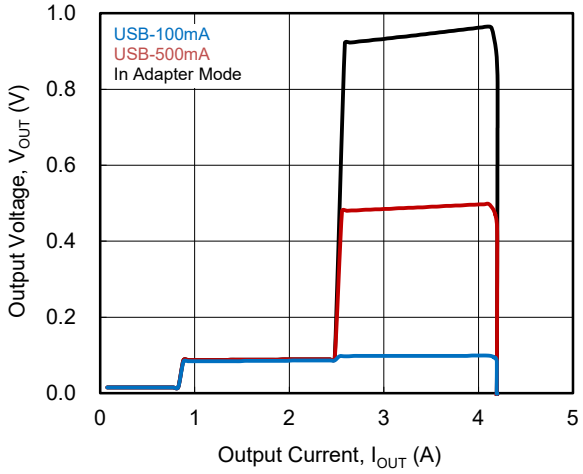
TYPICAL PERFORMANCE CHARACTERISTICS

For SGM40571-426AEJMF, based on the EVB test, unless otherwise noted.

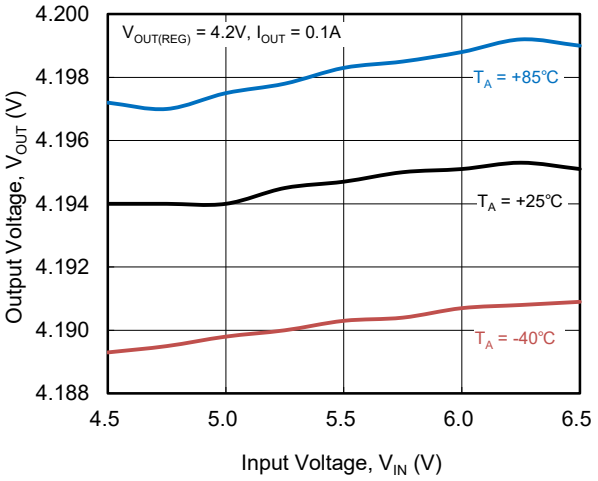
Output Current vs. R_{ISET}



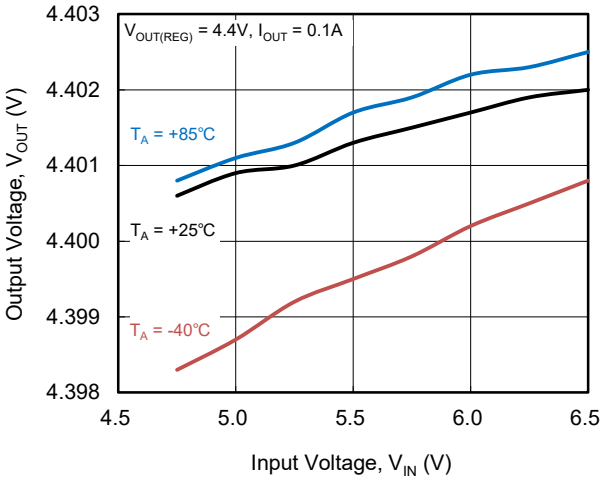
Charge Profile



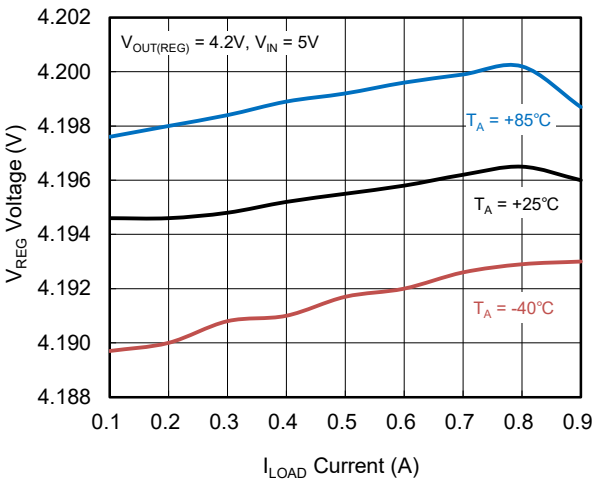
Line Regulation



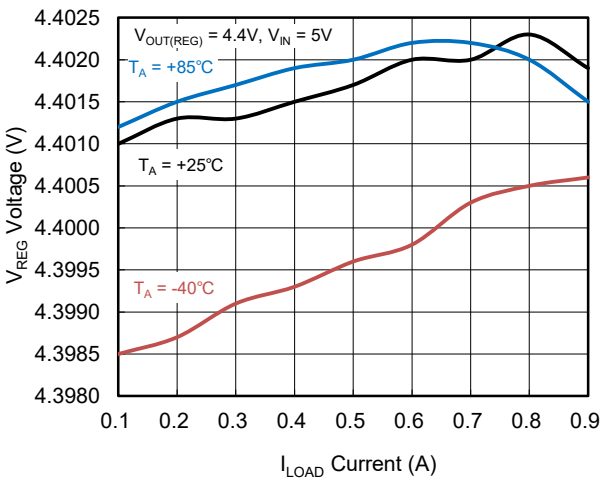
Line Regulation



Load Regulation



Load Regulation



FUNCTIONAL BLOCK DIAGRAM

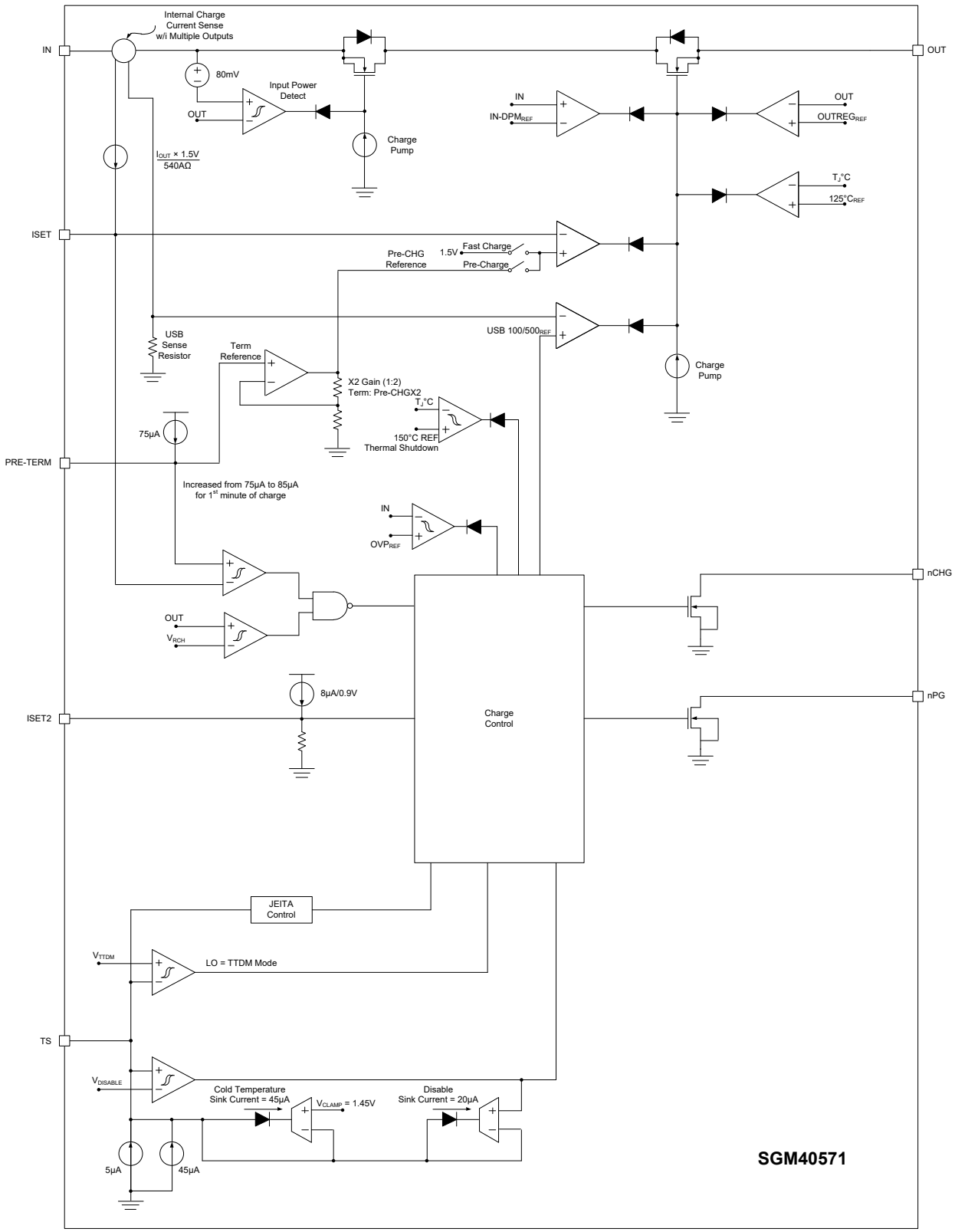


Figure 1. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM40571 is a highly integrated single-cell Li-Ion/ Li-polymer charger IC. This device supports three operational modes: charging a battery, powering a system, or simultaneously performing both functions. Charging progresses through three phases: Pre-charge to recover deeply discharged batteries, constant-current fast-charge for buck-regulated current delivery, and voltage regulation to achieve full capacity safely. The SGM40571 offers flexible programmability of fast-charge current and pre-charge/ termination thresholds. Designed for USB or DC adapter inputs, it incorporates automatic battery presence detection.

The charger incorporates comprehensive safety features including JEITA Temperature Standard, over-voltage protection (OVP), input dynamic power management (IN-DPM), safety timers, and ISET short-circuit protection. Detailed specifications for these and additional safeguards are provided in subsequent sections.

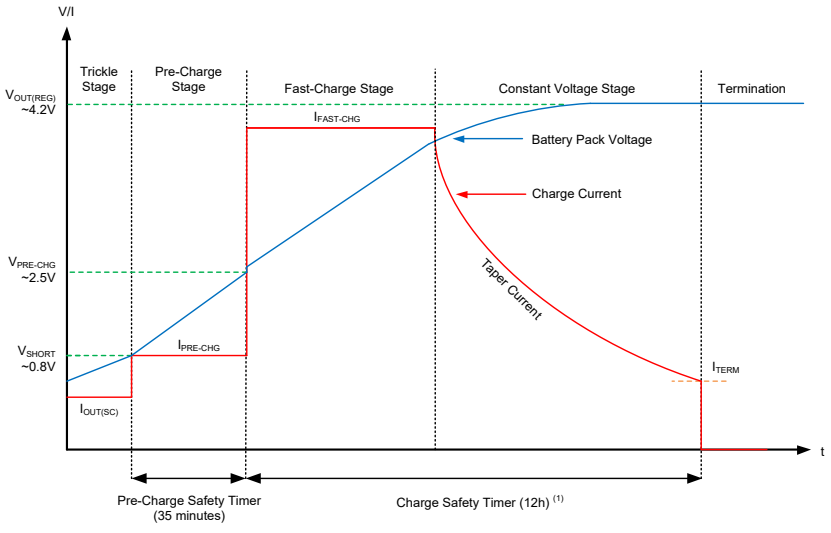
This SGM40571 implements a single power path architecture between input and output terminals for charging single-cell Li-Ion/Li-polymer battery packs. Upon application of a 5V DC input source, the device autonomously executes ISET and OUT short-circuit checks to ensure valid charge cycle initiation.

When battery voltage falls below the V_{LOWV} threshold, the device initiates a pre-charge cycle for discharged batteries. The pre-charge current is programmable via the PRE-TERM terminal, allowing configuration from 10% to 100% of the fast-charge current value. This feature compensates for concurrent system loads connected across the battery that divert charging current. By increasing pre-charge current, both system power demands and proper battery conditioning are simultaneously accommodated. The PRE-TERM terminal serves a dual function: setting pre-charge current and termination current thresholds. Note that the termination current threshold is fixed at 50% of the programmed pre-charge current threshold.

When the battery voltage reaches the V_{LOWV} threshold, fast-charge mode initiates with application of the programmed constant-current. The fast-charge current value is configured via the ISET terminal, delivering the majority of the total charge capacity. During this phase, the SGM40571 power dissipation peaks at lower battery voltages. If the junction temperature of SGM40571 reaches 125℃, thermal regulation activates: The timer clock frequency halves, and charge current reduces dynamically to prevent further temperature rise. Figure 2 illustrates this charging profile with thermal regulation. Under typical operating conditions, the junction temperature of SGM40571 remains below 125℃, avoiding thermal regulation activation.

Once the battery cell attains the regulation voltage, the voltage control loop engages and maintains the battery at this voltage until the charge current decays to the termination threshold. Termination functionality may be disabled if required. The nCHG terminal asserts a low state (illuminating the LED) exclusively during the initial charge cycle and de-asserts upon reaching the termination threshold, irrespective of whether charge current termination is enabled or disabled.

Additional operational details are provided in the Device Functional Modes section.



NOTE:
1. Safety timer is 2 × 12h, if in cold operation or IN-DPM or thermal regulation or in USB current limit mode.

Figure 2. Charging Profile with Safety Timer

DETAILED DESCRIPTION (continued)

Power-Down or Under-Voltage Lockout (UVLO)

The SGM40571 enters a power-down state when the V_{IN} falls below $V_{UVLO(FALL)}$. In this state, all terminals assume a high-impedance condition. When V_{IN} exceeds $V_{UVLO(RISE)}$, the IC transitions to either sleep mode or active mode, determined by the OUT terminal (battery) voltage level.

Power-Up

The SGM40571 resumes operation when V_{IN} exceeds $V_{UVLO(RISE)}$ (see Sleep Mode section), resetting all logic circuits and timers while initiating continuous monitoring routines. During typical operation where the input voltage quickly rises through $V_{UVLO(RISE)}$ and exits sleep states, the SGM40571 declares power good status, initiates a 100mA qualification charge, sets input current limit based on ISET2 terminal configuration, activates safety timers, and enables the nCHG terminal.

Sleep Mode

When the V_{IN} is between V_{OUT} + $V_{IN(DT)}$ and $V_{UVLO(RISE)}$, the charge current is disabled, safety timer counting stops (without reset), and both nPG and nCHG terminals become high-impedance. Upon input voltage rise causing the charger to exit sleep mode, the nPG terminal goes low, the safety timer resumes counting, charging is enabled, and the nCHG terminal returns to its prior state. Refer to Figure 3.

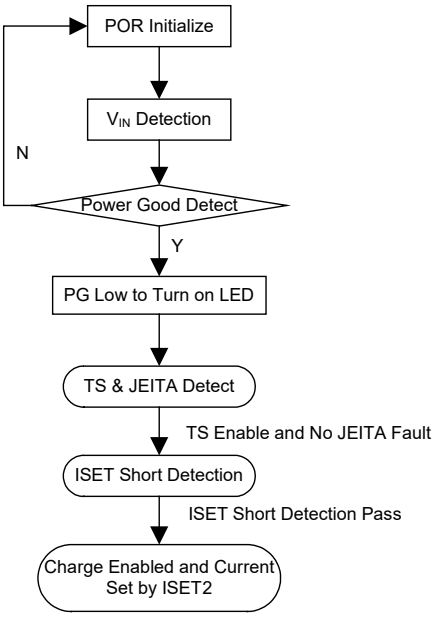


Figure 3. Power-Up Flow Diagram

New Charge Cycle

A new charge cycle is initiated upon the occurrence of any of the following events: application of a valid power source, toggling the chip enable/disable state via the TS pin, exiting from termination and timer disable mode (TTDM), detection of battery insertion, or when the OUT voltage drops below the V_{RCH} threshold. The nCHG signal remains active exclusively during the initial charge cycle. Consequently, exiting TTDM or the OUT voltage falling below V_{RCH} will not activate the nCHG signal if it is already in the open-drain (off) state.

Over-Voltage Protection (OVP) - Continuously Monitored

When the input source applies an over-voltage, the pass FET (if previously on) turns off after a deglitch period, t_{BLK} (OVP). The safety timer ends, and both the nCHG and nPG terminals enter a high-impedance state. Once the over-voltage condition resolves and normal voltage is restored, the nPG terminal goes low, the timer resumes counting, charging continues, and the nCHG terminal goes low after a 25ms deglitch period.

Power Good Indication (nPG)

When input voltage above V_{BAT} + $V_{IN(DT)}$ but remains below V_{OVP}, the PG FET activates and establishes a low-impedance path to ground.

nCHG Terminal Indication

The nCHG pin internally is an open-drain FET that turns on (pulls down to VSS) during the first charging cycle (independent of TTDM), deactivating once the battery reaches voltage regulation and charge current tapers to the termination current. This terminal remains high-impedance during sleep mode and OVP (if nPG is high-impedance), reverting to prior state upon condition clearance.

Power cycling, toggling the TS pin (low → release), or entering pre-charge mode resets nCHG (causing it to go low when the valid power and the discharged battery are present), marking the start of a new first charge cycle.

Device Functional Modes

nPG and nCHG LED Pull-Up Source

For host monitoring, connect a pull-up resistor between the nPG/nCHG pin and VCC of host. For visual indication, connect an LED in series with a current-limiting resistor between the STATUS terminal and a power source. If the nPG or nCHG source voltage may exceed 6V, implement a 5.6V Zener diode for voltage clamping. When using the OUT terminal as the source, note that LED brightness will vary with battery voltage fluctuations due to changing forward voltage requirements.

DETAILED DESCRIPTION (continued)

Table 1. nPG and nCHG LED Behaviors

V_{IN} Power Good State	nPG FET/LED	Charging State	nCHG FET/LED
UVLO	OFF	First Charge after VIN Applied	ON
Sleep Mode		Sleep Mode	OFF
OVP Mode		OVP Mode	
Normal Input (V_{OUT} + $V_{IN(DT)}$ < V_{IN} < V_{OVP})	ON	Refresh Charge	
PG is Independent of Chip Disable		Battery Temperature Fault	Remain Unchanged

IN-DPM (V_{IN}-DPM or IN-DPM)

The IN-DPM feature detects an input voltage that is dropping (folding back), reaching its current limit due to excessive load. When the input voltage drops to the V_{IN-DPM} threshold, the internal FET starts to reduce the current until the input voltage stops dropping. This prevents a source with voltage below V_{IN-DPM} from powering the OUT pin. This works well with current-limited adapters and USB ports if their nominal voltage is above V_{IN-DPM}, respectively. This is an added safety feature that helps protect the source from excessive load.

OUT

The OUT pin serves as the power source, delivering current both to the battery and to any connected system. The SGM40571 offers multiple operational modes: charging the battery while simultaneously powering the system, charging the battery exclusively, or solely supplying power to the system (TTDM), provided the system demands stay within the available current. The OUT pin functions as a current-limited source featuring built-in short-circuit protection. If the system load surpasses the set current limit, the output voltage will drop unless adequate capacitance or a charged battery is present to absorb the overload.

ISET

An external resistor determines the programmed output current range (50mA to 1000mA). This same resistor also enables current monitoring functionality.

$$R_{ISET} = K_{ISET}/I_{FAST-CHG} \quad (1)$$

where

• $I_{FAST-CHG}$ is the target fast-charge current value.

• K_{ISET} is a scaling coefficient provided in the electrical characteristics.

The ISET resistor incorporates short-circuit protection and triggers detection when its resistance falls below $R_{ISET(SHORT)}$. This detection mechanism requires a minimum output current of 90mA to activate. Upon detecting a "short" condition, the SGM40571 will enter a latched-off state. Normal operation can only be restored by power cycling. Internally, the OUT current is clamped to a maximum value ranging from 1.07A to 1.55A. This current limiting operates independently of the ISET short-detection circuit, as illustrated in Figure 4.

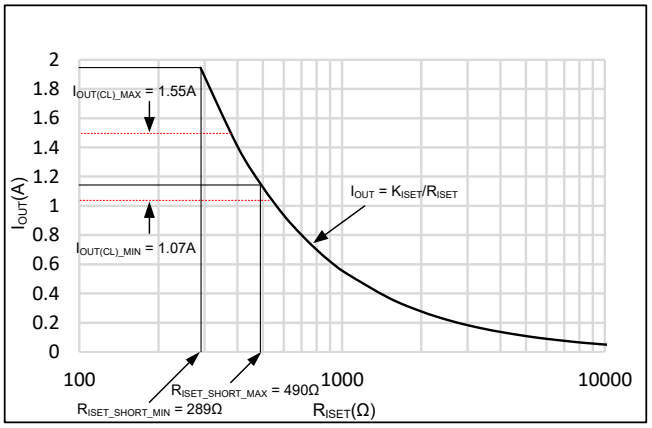


Figure 4. Programmed/Clamped Out Current

PRE-TERM - Pre-Charge and Termination Programmable Threshold

The PRE-TERM pin configures both the pre-charge current and the termination current threshold. The pre-charge current is consistently set at twice the level of the termination current. The termination current threshold can be adjusted within a range of 5% to 50% of the full-scale output current programmed via the ISET pin. Leaving this pin unconnected defaults the termination and pre-charge levels to 10% and 20%, respectively. Additionally, the pre-charge to fast-charge transition voltage (V_{LOWV}) is fixed at 2.5V.

$$R_{PRE-TERM} = \%_{TERM} \times K_{TERM} = \%_{PRE-CHG} \times K_{PRE-CHG} \quad (2)$$

where

• $\%_{TERM}$ is the termination current as a percentage of the fast-charge current.

• $\%_{PRE-CHG}$ is the target of pre-charge current as a percentage of the fast-charge current.

• K_{TERM} and $K_{PRE-CHG}$ are scaling coefficient provided in the electrical characteristics.

ISET2

The ISET2 pin functions as a three-state input (low, floating or high) that configures the input current limit and regulation threshold. A Low state programs the regulated fast-charge current through the ISET resistor. A floating state establishes a 100mA current limit. And a high state sets a 500mA current limit.

DETAILED DESCRIPTION (continued)

TS

The TS function implements the updated JEITA temperature standard for Li-Ion/Li-polymer batteries, defining four critical thresholds: 0℃, 10℃, 45℃, and 60℃. Normal charging operation is permitted within the 10℃ to 45℃ range. Temperatures between 0℃ and 10℃ trigger a 50% reduction in charge current, while the 45℃ to 60℃ range reduces the regulation voltage to a maximum of 4.05V (refer to Figure 5).

This feature employs an internal 50μA current source to bias an external thermistor connected between the TS and VSS pins. The design requires a 10kΩ NTC thermistor with β = 3370 (e.g., SEMITEC 103AT-2 or Mitsubishi TH05-3H103F). When thermal monitoring is unnecessary, normal operation can be maintained by installing a fixed 10kΩ resistor between TS and VSS pins. This configuration is applicable when system-level thermal management exists, allowing the host controller to disable charging by pulling TS low.

The TS pin incorporates two additional control functions: pulling the pin low disables charging, while driving the pin high or leaving it floating enables TTDM (timer/termination/disable mode) operation. Charging is automatically disabled outside the 0℃ to 60℃ operational window.

A specialized foldback mechanism reduces the TS bias current to approximately 30μA when the pin is pulled low (see Figure 6). Additionally, when thermistor temperatures drop below ≈ -10℃, the current automatically reduces to prevent false TTDM activation during extreme cold conditions (-10℃ to -50℃). Due to fixed current sourcing and calibrated temperature thresholds, compatibility is strictly limited to 10kΩ NTC thermistors (rated at 25℃).

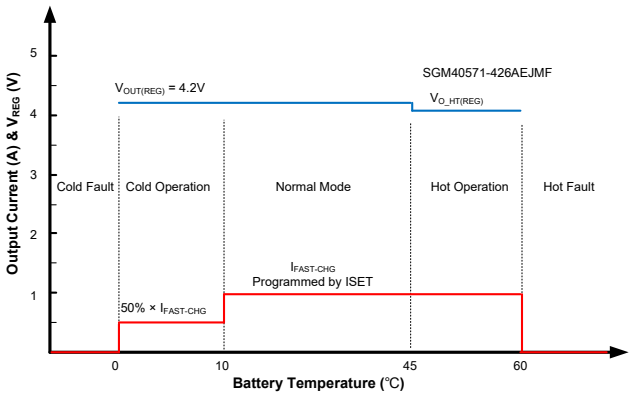
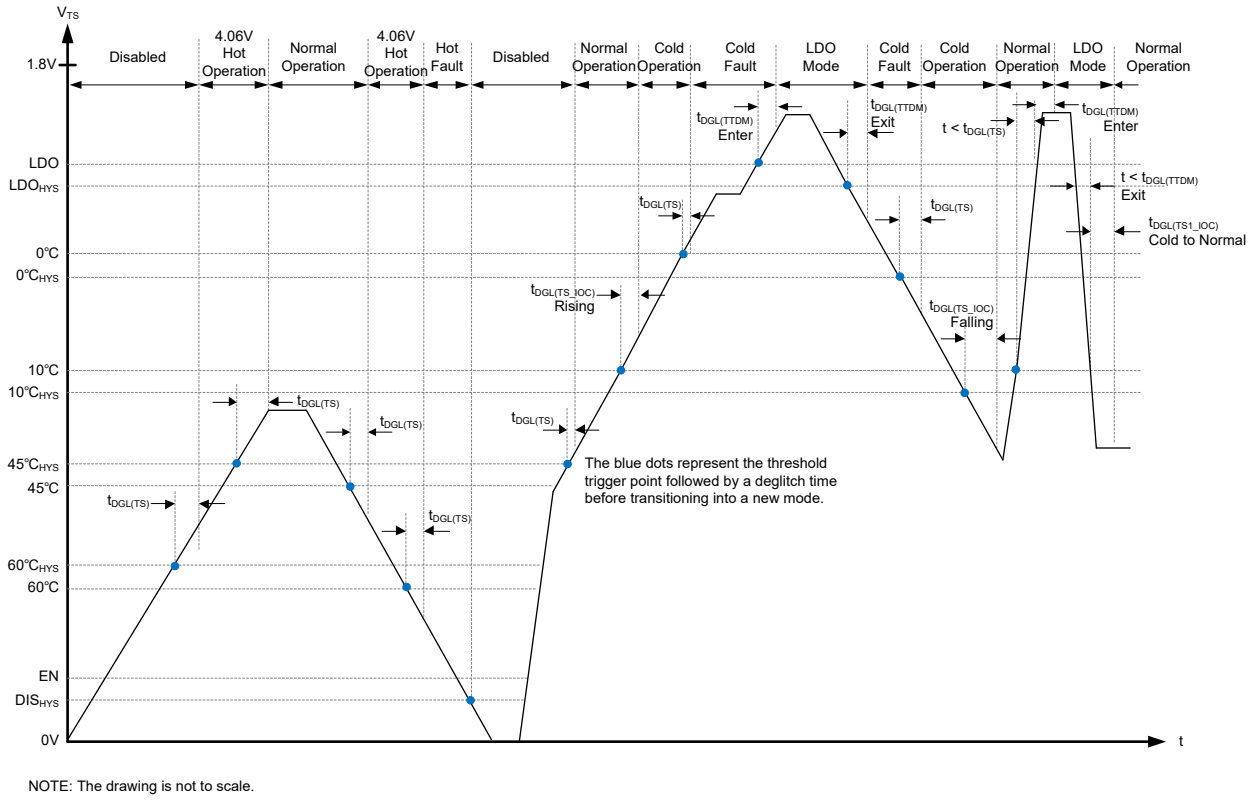


Figure 5. Operation vs. Battery Temperature



NOTE: The drawing is not to scale.

Figure 6. TS Battery Temperature Bias Threshold and Deglitch Timers

DETAILED DESCRIPTION (continued)

Termination and Timer Disable Mode (TTDM) - TS Terminal High

The charger enters TTDM mode when the TS terminal voltage exceeds the TTDM threshold, either due to thermistor disconnection (battery removal/floating TS pin) or active pull-up to this voltage level. In TTDM mode: the 12-hour safety timer remains held in reset. Charge termination is disabled. And a battery detection sequence is initiated. If battery absence is confirmed, the nCHG terminal enters high-impedance state (if not already). When a battery is detected, nCHG maintains its current state until charge current decays to the termination threshold, at which point it switches to high-impedance (while output regulation persists).

The core charging profile remains unaltered (preserving pre-charge, constant-current fast charge, and constant-voltage phases), ensuring safe charging with natural current decay to zero. Upon exiting TTDM, the battery detection reruns. If a battery is present, a new charge cycle starts with nCHG LED illumination.

Avoid configuring any capacitance exceeding 100pF on the TS pin, as this may inadvertently trigger TTDM mode during battery pack temperature sense insertion/removal.

To prevent unintended TTDM triggering during thermistor-equipped battery removal: connect a 237kΩ resistor between TS and VSS pins. This configuration blocks the current source from elevating TS voltage to TTDM threshold, introducing temperature sensing errors of ≈ 0.1℃ at high temperatures and ≈ 3℃ at low temperature.

Timers

The pre-charge timer is fixed at 35 minutes duration. The pre-charge current is programmable to compensate for system loads, ensuring sufficient time allocation within this interval.

The fast-charge timer operates at a fixed 12-hour duration, extendable during thermal regulation, IN-DPM activation, or USB current limiting. Under these conditions, the timer clock frequency halves (counting at 50% nominal rate). When the timer expires, the charging terminates with the nCHG terminal transitioning to high-impedance state if not already inactive.

Timer reset occurs upon IC disablement, power cycling, or TTDM mode entry/exit sequences.

Termination

When V_{OUT} exceeds V_{RCH} (entering voltage regulation mode) with concurrent charge current decay to the termination threshold, the nCHG terminal transitions to high-impedance state while initiating a battery detection routine to discern between battery removal and full-charge condition. If the battery presence is verified, charging current terminates. If simultaneous battery and thermistor removal occurs, the TS terminal voltage elevates, triggering TTDM mode entry. If only battery removal occurs while TS remains within active monitoring range, the detection routine persists cyclically until battery reinsertion.

Battery Detect Routine

The purpose of the battery detection routine is to verify the absence of a battery while maintaining a usable voltage level at the OUT terminal. When a missing battery is detected, the nCHG terminal shall enter a high-impedance state. This routine executes during transitions into and out of TTDM to confirm battery presence. If the battery is absent and the device is not in TTDM, the routine operates continuously.

During system power-up, if the detected battery voltage exceeds the preset V_{RCH}, the battery detection routine is triggered immediately to determine battery presence.

Note that the battery detection is disabled when the IC is operating in TTDM or when a TS fault occurs.

Refer to Figure 7 (Battery Detect Flow Diagram) for the detailed detection logic flow.

Refresh and Recharge

After charge termination, if the V_{OUT} falls to V_{RCH} (defined as 100mV below the regulation voltage), a new charge is initiated. The nCHG terminal maintains a high-impedance state (off).

Starting a Charge on a Full Battery

During the $t_{TERM-START}$ time of a charge cycle, the termination threshold is elevated by approximately 14%. This ensures prompt termination (< $t_{TERM-START}$) when initiating a new charge or when a fully charged battery is reinserted. Batteries exhibiting significant relaxation (multiple hours) may require several minutes to reach the termination threshold as charging current tapers.

DETAILED DESCRIPTION (continued)

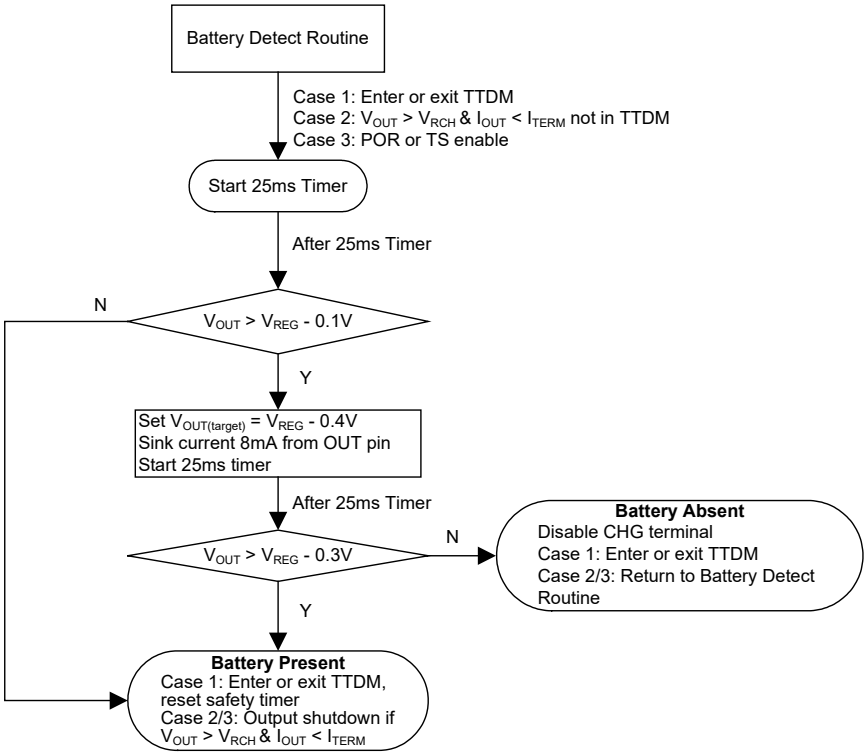


Figure 7. Battery Detect Flow Diagram

APPLICATION INFORMATION

The SGM40571 supports configuration of fast charge current, pre-charge current, and termination current via an external resistor. Different power sources, such as adapters or USB, can configure distinct voltage levels through ISET2. Additionally, suitable input and output capacitors can be selected based on the input voltage range and load current. A typical application circuit is shown in Figure 8.

Design Requirements

- Supply voltage (5V)
- Fast charge current ($I_{FAST-CHG}$ = 540mA)
- Pre-charge current ($I_{PRE-CHG}$ =108mA)
- Termination current (I_{TERM} = 54mA)

Input Capacitor (C_{IN}) and Out Capacitor (C_{OUT})

The input capacitors are selected by ensuring adequate voltage margin above the maximum surge voltage, while avoiding excessive margin to limit the peak currents drawn from the source and reduce input noise. For the input capacitor (C_{IN}), use a 1μF low ESR ceramic bypass capacitor placed as close as possible to the IN and VSS pins.

The output capacitor (C_{OUT}) should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients. It is recommended to connect a 1μF low equivalent series resistance (ESR) ceramic bypass capacitor (X7R/X5R grade) between the OUT pin and the VSS pin, and place it at the position with the shortest trace length. For high output current conditions, increase the capacitance value proportionally to maintain stability and transient response.

Detailed Design Procedure Calculations

ISET Resistor Selection (R_{ISET}), Configure Fast Charge Current

$$R_{ISET} = K_{ISET}/I_{FAST-CHG} \quad (3)$$

where

- K_{ISET} = 540AΩ.
- R_{ISET} = 540AΩ/0.54A = 1.0kΩ.

Select the closest standard value, place a 1kΩ resistor between the ISET pin and VSS.

PRE-TERM Resistor Selection ($R_{PRE-TERM}$), Configure Pre-Charge Current and Fast Charge Current

$$R_{PRE-TERM} = K_{PRE-CHG} \times \%I_{FAST-CHG} \quad (4)$$

where

- $\%I_{FAST-CHG}$ = 20%.
- $R_{PRE-TERM}$ = 100Ω/% × 20% = 2kΩ.

Select the closest standard value, place a 2kΩ resistor between the PRE-TERM pin and VSS.

Power Supply Recommendations

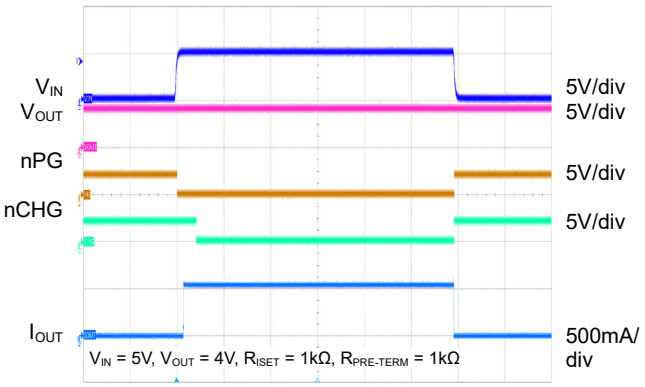
The SGM40571 is designed to operate from an input supply voltage ranging from 3.5V to 28V, with a current capability of at least the maximum designed charge current. The input supply should be well-regulated. If the connection point of the power supply is more than a few centimeters (or inches) away from the IN and VSS pin of SGM40571, it is recommended to use a larger capacitor.

APPLICATION INFORMATION (continued)

Application Curves

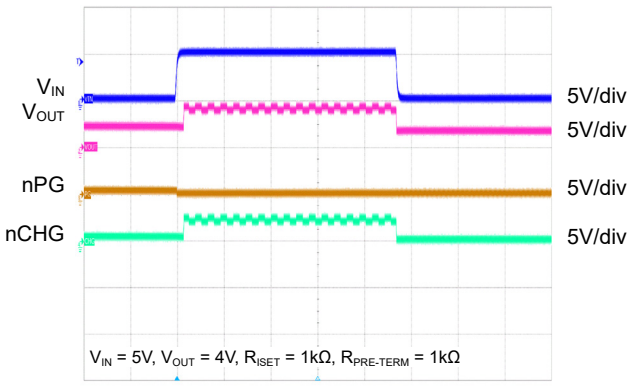
For SGM40571-426AEJMF, based on the EVB test, unless otherwise noted.

Plug-in or Plug-out V_{IN} with Battery



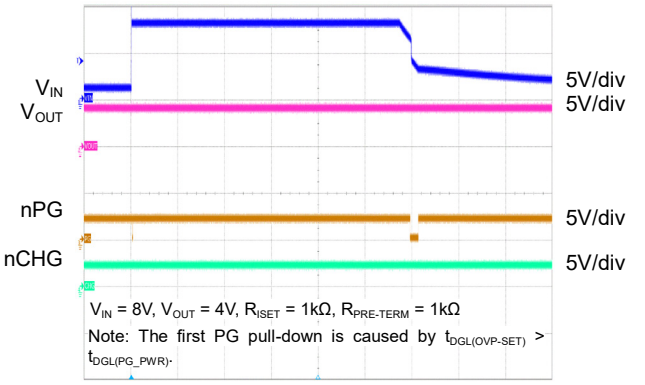
Time (200ms/div)

Plug-in or Plug-out V_{IN} without Battery, Not in TTDM



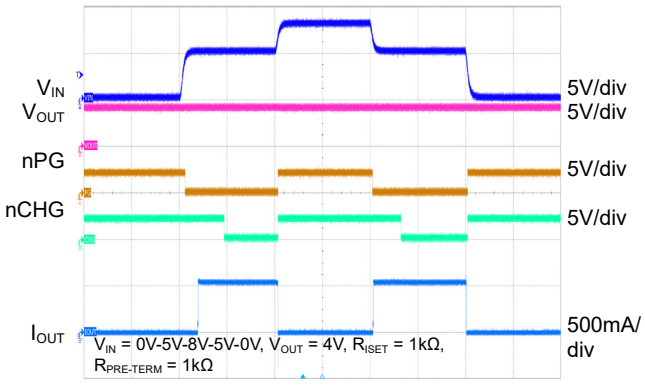
Time (200ms/div)

Plug-in or Plug-out V_{IN} with Battery



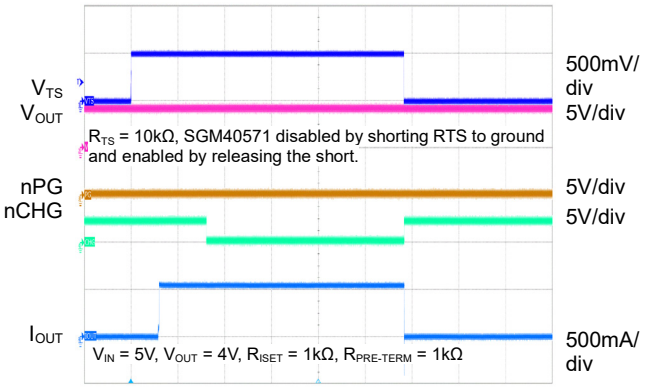
Time (20ms/div)

The Triggering and Release of $V_{IN(OVP)}$ in Normal Operation Mode



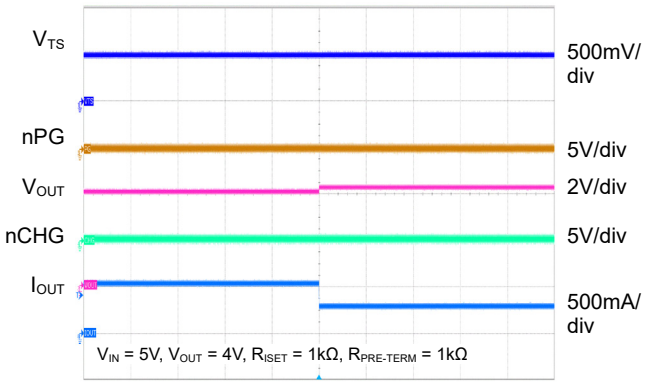
Time (100ms/div)

TS Enable and Disable



Time (50ms/div)

Remove Battery When I_{LOAD} = 0.3A > I_{TERM}



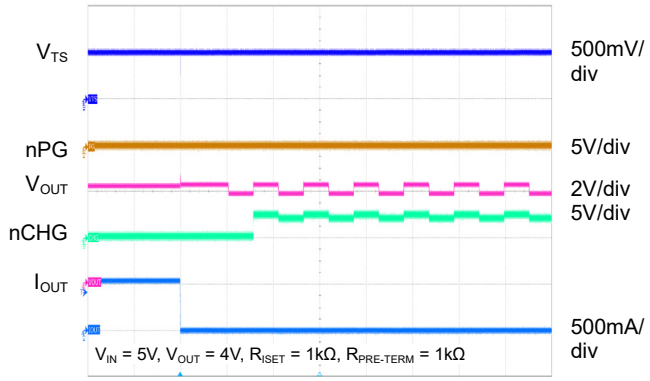
Time (50ms/div)

APPLICATION INFORMATION (continued)

Application Curves (continued)

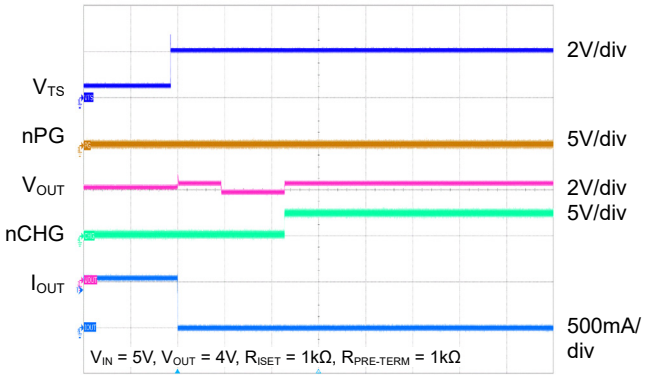
For SGM40571-426AEJMF, based on the EVB test, unless otherwise noted.

Remove Battery When I_{LOAD} = 10mA < I_{TERM}



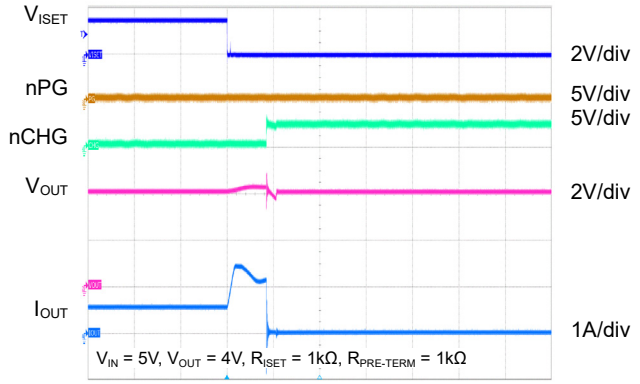
Time (50ms/div)

Remove Battery and R_{TS}



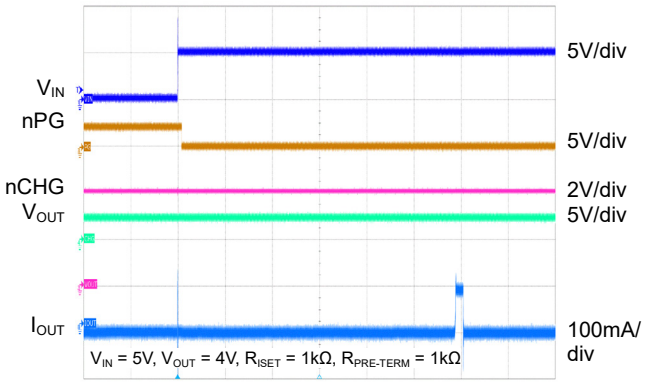
Time (20ms/div)

ISET Shorted during Normal Operation



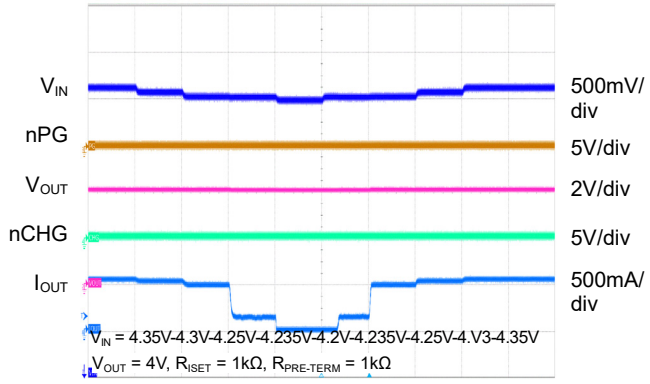
Time (1ms/div)

VIN Power-On When ISET Shorted



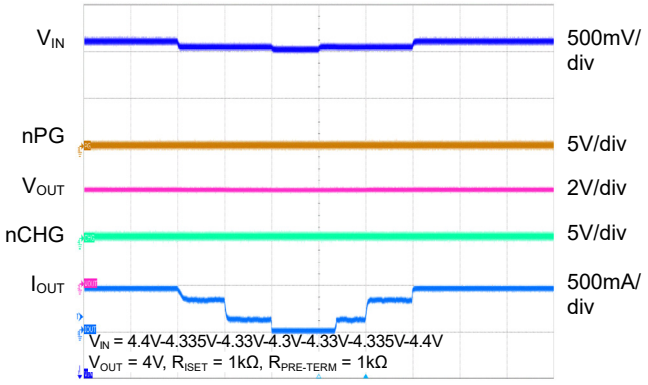
Time (5ms/div)

VIN-DPM (Adapter Mode)



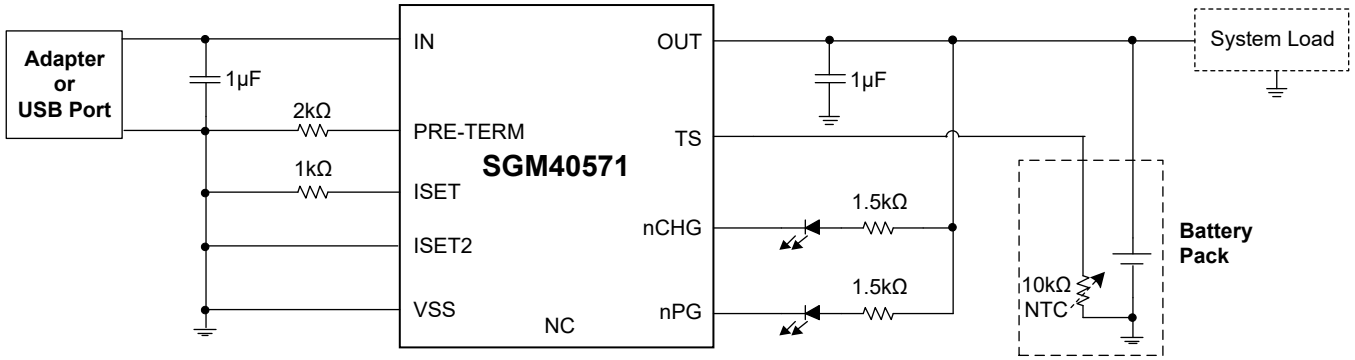
Time (200ms/div)

VIN-DPM (USB-500mA)



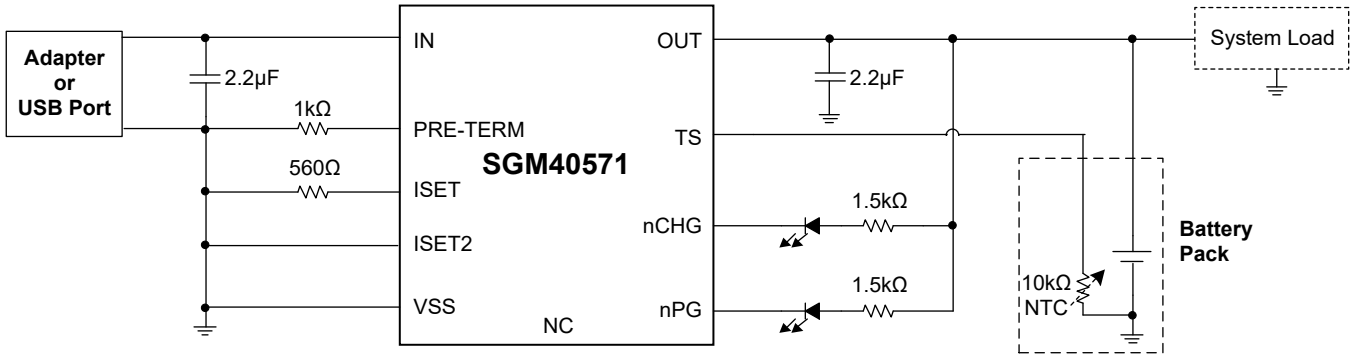
Time (200ms/div)

APPLICATION INFORMATION (continued)



NOTE: $I_{OUT(FAST-CHG)}$ = 540mA, $I_{OUT(PRE-CHG)}$ = 108mA, $I_{OUT(TERM)}$ = 54mA.

(a)



NOTE: $I_{FAST-CHG}$ ≈ 1A, $I_{OUT(PRE-CHG)}$ = 96mA, $I_{OUT(TERM)}$ = 48mA.

(b)

Figure 8. Typical Application Circuit

APPLICATION INFORMATION (continued)

Layout Guidelines

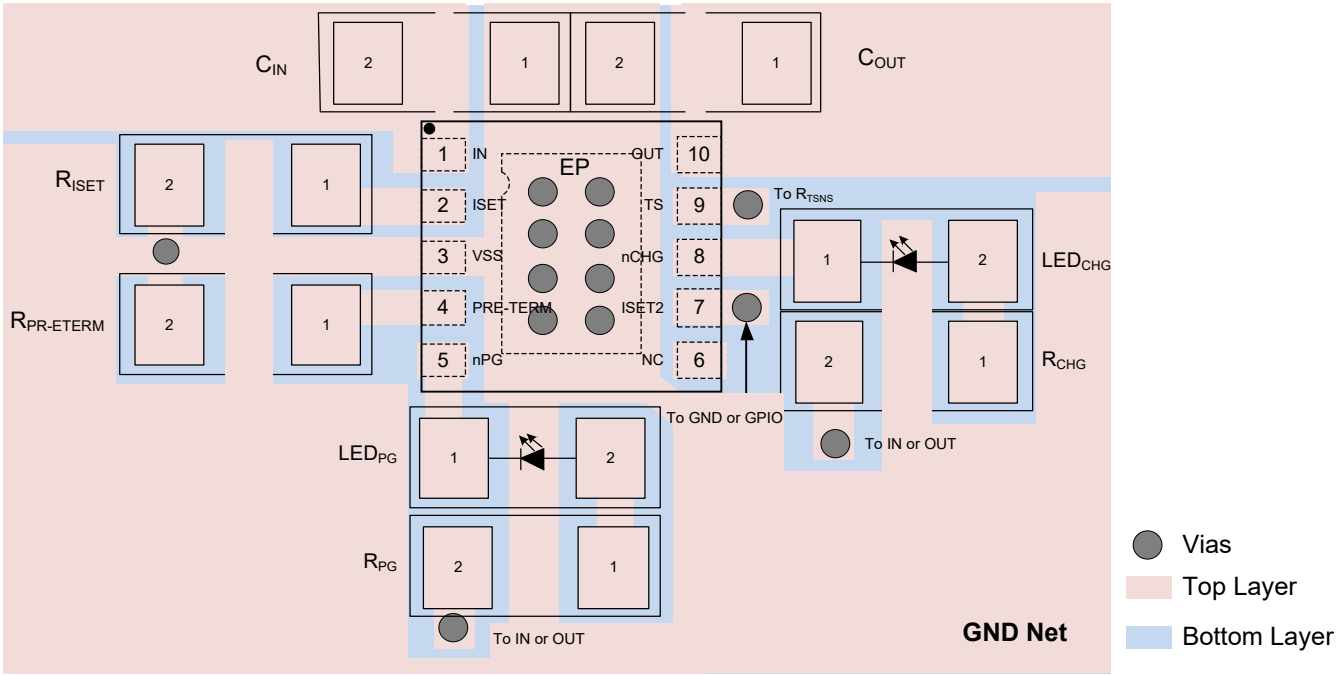
For optimal performance, the decoupling capacitor from the IN pin to GND (thermal pad) and the output filter capacitor from the OUT pin to GND (thermal pad) should be placed as close as possible to the SGM40571 chip, while ensuring that the trace lengths from IN, OUT, and GND (thermal pad) to these components are kept as short as possible.

• All low-current GND connections should be separated from high-current charging or discharging paths from the battery. Use a single-point grounding technique that combines small-signal ground paths and power ground paths.

• The high-current charging paths entering from the IN interface and flowing out from the OUT interface must be appropriately sized according to the maximum charging current to avoid voltage drops in these traces.

• To effectively transfer heat from the SGM40571 to the PCB, the thermal pad and pin traces (especially those for IN and OUT) should be designed with as wide a copper width as possible for the optimal thermal performance.

• The SGM40571 adopts TDFN-2×2-10L package with enhanced thermal performance. This package includes a thermal pad to provide efficient thermal contact between the chip and the printed circuit board (PCB). This thermal pad also serves as the main ground connection for the device. Connect the thermal pad to the PCB's ground connection. It is recommended to use multiple 10mil vias in the chip's power pad and place them sufficiently close to conduct heat to the bottom ground plane. The substrate plane on the bottom should avoid traces that "cut off" the heat conduction path. The thinner the PCB, the lower the temperature rise. The EVM PCB has a thickness of 0.8mm (approximately 0.031 inches), with 2oz. copper (2.8mil thick) on both top and bottom layers, serving as an example of optimal thermal performance.



NOTE: The PCB layout diagram is for illustrative purposes only and does not represent the actual demo board design.

Figure 9. Board Layout

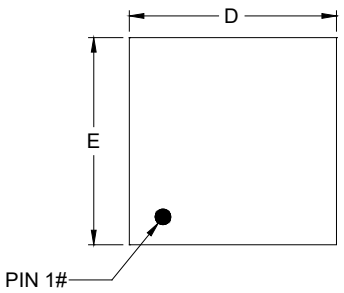
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

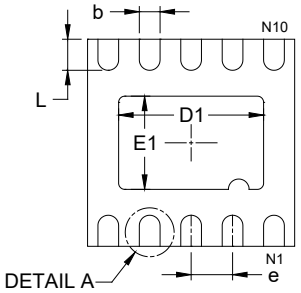
Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

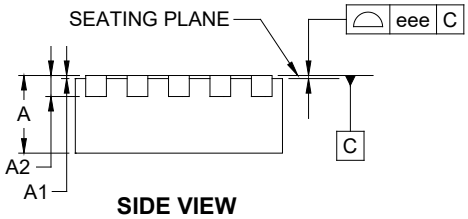
TDFN-2×2-10L



TOP VIEW



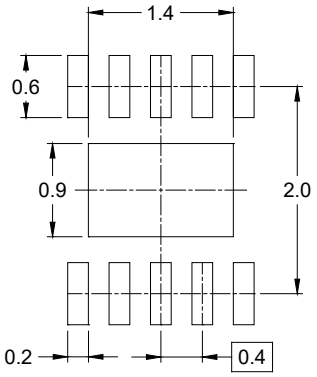
BOTTOM VIEW



SIDE VIEW

DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



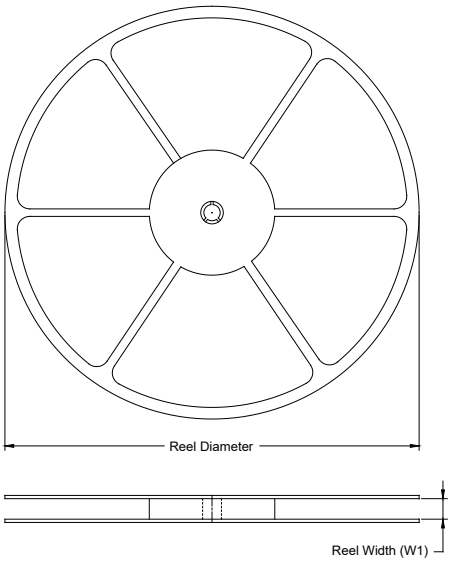
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
D	1.900	-	2.100
D1	1.300	-	1.500
E	1.900	-	2.100
E1	0.800	-	1.000
e	0.400 BSC		
L	0.200	-	0.400
eee	0.080		

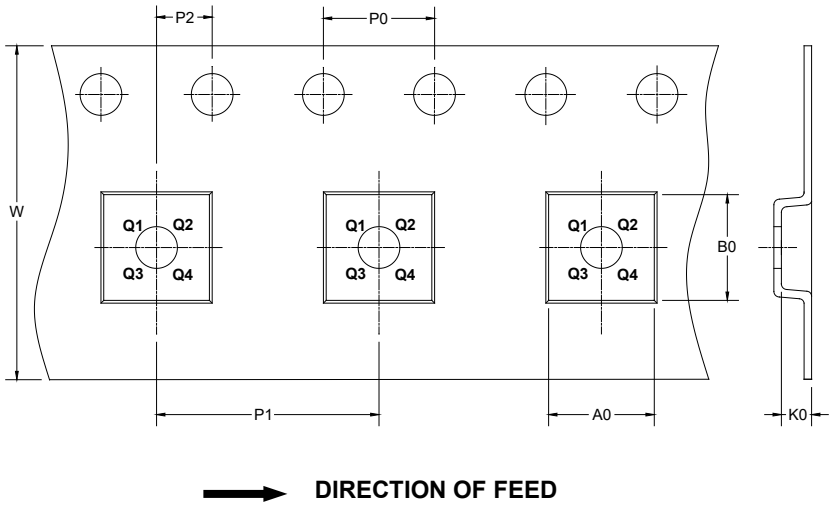
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



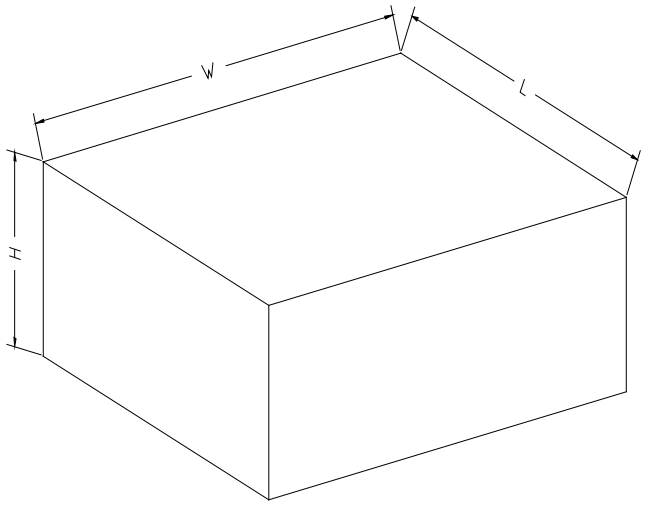
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-10L	7″	9.5	2.30	2.30	1.00	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002