SGM2238xQ Automotive 40V, 300mA, Low Quiescent Current and Low Dropout Voltage Linear Regulator

GENERAL DESCRIPTION

The SGM2238xQ is a high voltage, low quiescent current and low dropout voltage linear regulator. It is capable of supplying 300mA output current with typical dropout voltage of 450mV. The operating input voltage range is from 3V to 40V. The fixed output voltage range is from 1.8V to 12V and the adjustable output voltage range is from 1.25V to 24V.

Other features include current limit and thermal shutdown protection. The SGM2238xQ has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

This device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM2238xQ is available in a Green SOIC-8 (Exposed Pad) package. It operates over an operating temperature range of -40℃ to +125℃.

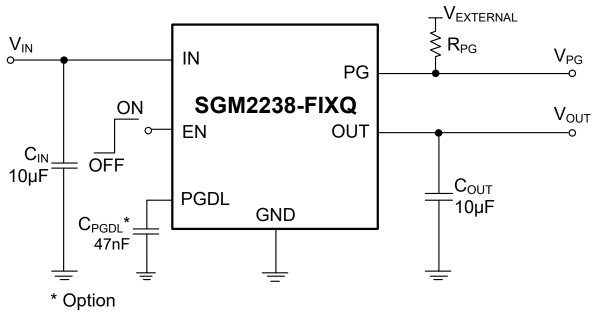
APPLICATIONS

Automotive
Battery-Powered Equipment
Ultra-Low Power System
Medical Equipment
Industrial Equipment

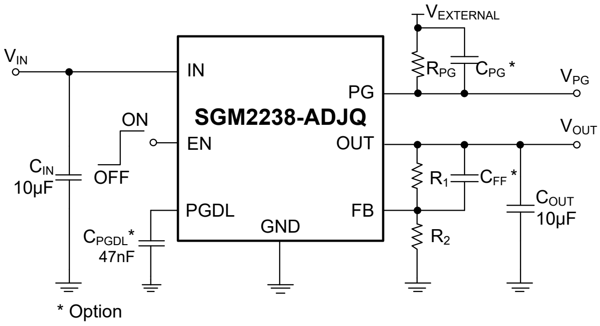
FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Operating Input Voltage Range: 3V to 40V**
- **Enable Pin Accept Voltages Higher than the Supply Voltage and up to 40V**
- **Fixed Output from 1.8V to 12V**
- **Adjustable Output from 1.25V to 24V**
- **300mA Output Current**
- **Output Voltage Accuracy: ±1% at +25℃**
- **Low Quiescent Current: 3.8μA (TYP)**
- **Low Dropout Voltage:**
  450mV (TYP) at 300mA, $V_{OUT(NOM)} \geq 3.3V$
- **Current Limiting and Thermal Protection**
- **Support Power-Good Indicator Function**
- **With Output Automatic Discharge**
- **Stable with Small Case Size Ceramic Capacitors**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

TYPICAL APPLICATION



Fixed Output Voltage Version



Adjustable Output Voltage Version

Figure 1. Typical Application Circuits

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2238-1.8Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-1.8QPS8G/TR	1DZPS8 XXXXX	Tape and Reel, 4000
SGM2238-2.5Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-2.5QPS8G/TR	1E0PS8 XXXXX	Tape and Reel, 4000
SGM2238-3.0Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-3.0QPS8G/TR	1E1PS8 XXXXX	Tape and Reel, 4000
SGM2238-3.3Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-3.3QPS8G/TR	160PS8 XXXXX	Tape and Reel, 4000
SGM2238-3.6Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-3.6QPS8G/TR	1E2PS8 XXXXX	Tape and Reel, 4000
SGM2238-4.2Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-4.2QPS8G/TR	1E3PS8 XXXXX	Tape and Reel, 4000
SGM2238-5.0Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-5.0QPS8G/TR	15ZPS8 XXXXX	Tape and Reel, 4000
SGM2238-8.0Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-8.0QPS8G/TR	1E4PS8 XXXXX	Tape and Reel, 4000
SGM2238-9.0Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-9.0QPS8G/TR	1E5PS8 XXXXX	Tape and Reel, 4000
SGM2238-12Q	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-12QPS8G/TR	161PS8 XXXXX	Tape and Reel, 4000
SGM2238-ADJQ	SOIC-8 (Exposed Pad)	-40℃ to +125℃ (T_A)	SGM2238-ADJQPS8G/TR	162PS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X XXX X

- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, EN to GND .... -0.3V to 42V
OUT to GND .... -0.3V to MIN(42V, V_{IN} + 0.3V)
FB to GND .... -0.3V to 42V
PG to GND.. -0.3V to 42V
PGDL to GND .... -0.3V to 6V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA}..................................... 40℃/W
SOIC-8 (Exposed Pad), θ_{JB}................................... 16.7℃/W
SOIC-8 (Exposed Pad), $\theta_{JC(TOP)}$ .... 55.9℃/W
SOIC-8 (Exposed Pad), $\theta_{JC(BOT)}$ .... 6℃/W
Junction Temperature...+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility (1) (2)
HBM...±2000V
CDM ....±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN}......................................3V to 40V
Enable Input Voltage Range, V_{EN} ....3V to 40V
Input Effective Capacitance, C_{IN} .... 1μF (MIN)
Output Effective Capacitance, C_{OUT} ....1μF to 100μF
Operating Ambient Temperature Range.......-40℃ to +125℃
Operating Junction Temperature Range.......-40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

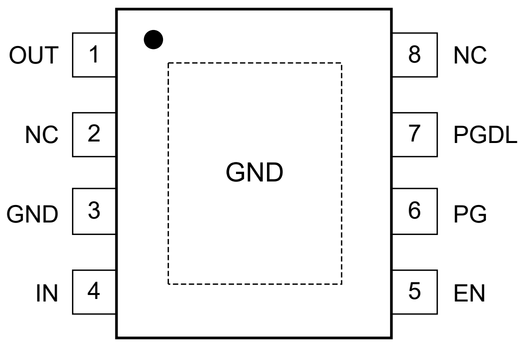
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

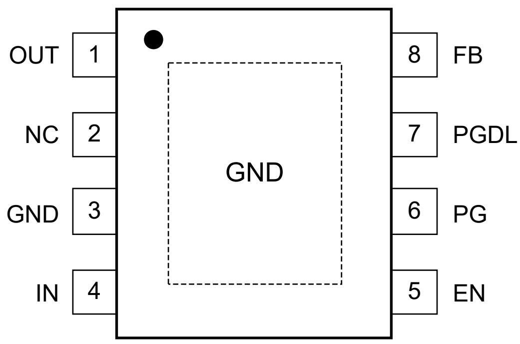
PIN CONFIGURATIONS

SGM2238-FIXQ (TOP VIEW)



SOIC-8 (Exposed Pad)

SGM2238-ADJQ (TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with effective capacitance in the range of 1μF to 100μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
2	NC	No Connection.
3	GND	Ground.
4	IN	Input Supply Voltage Pin. It is recommended to use a 2.2μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
5	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator.
6	PG	Power-Good Indicator Output Pin. An open-drain, active-high output that indicates the status of V_{OUT}. When the output voltage reaches PG_{HTH} of the target, the PG pin goes into a high-impedance state.
7	PGDL	Power-Good Delay Pin. Keep this pin floating when it is not in use.
8	NC	No Connection (Fixed Version Only).
	FB	Feedback Voltage Input Pin (adjustable voltage version only). Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAMS

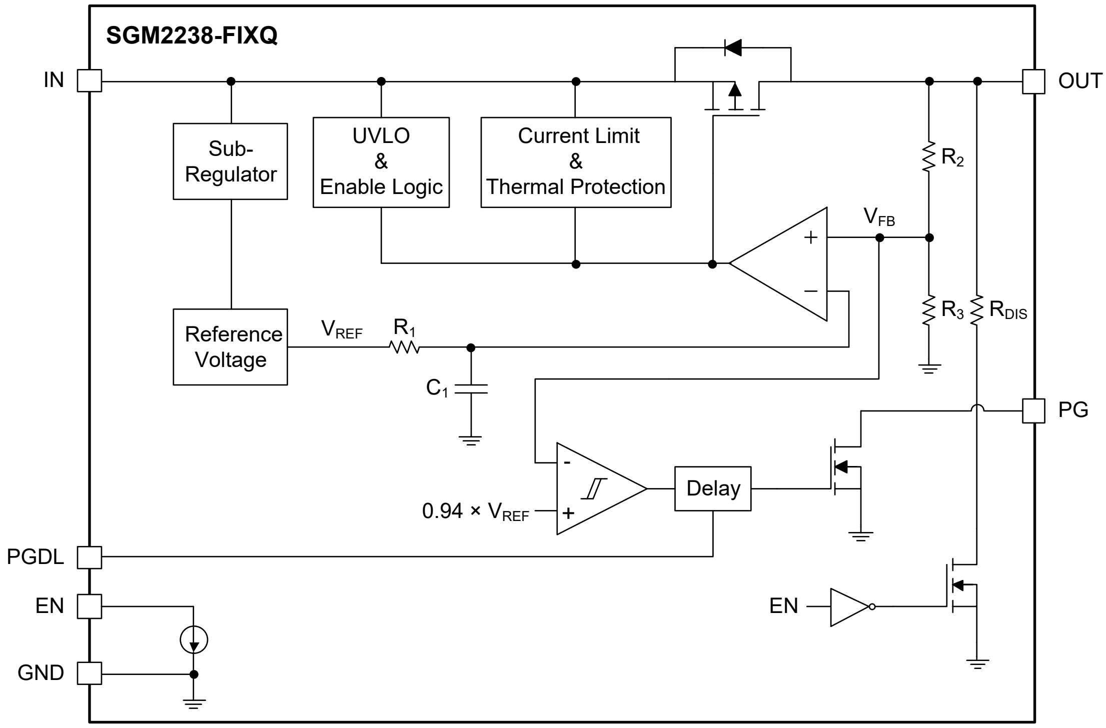


Figure 2. Block Diagram of Fixed Output Version

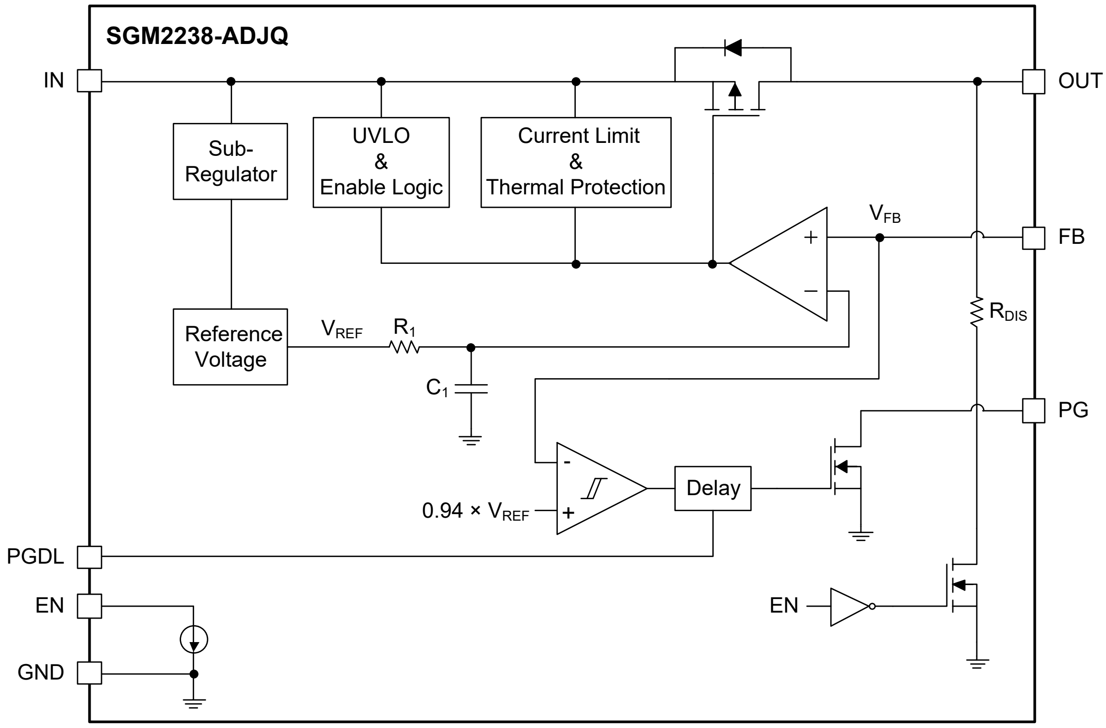


Figure 3. Block Diagram of Adjustable Output Version

ELECTRICAL CHARACTERISTICS

(V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, T_J = -40℃ to +125℃ (1), typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			3		40	V
Output Voltage Range	V_{OUT}			1.25		24	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) to 40V, I_{OUT} = 1mA to 300mA	T_J = +25℃	-1		+1	%
			T_J = -40℃ to +125℃	-2		+1.5	
Feedback Voltage	V_{FB}	V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) to 40V, I_{OUT} = 1mA to 300mA	T_J = +25℃	1.237	1.25	1.263	V
			T_J = -40℃ to +125℃	1.225	1.25	1.269	
FB Pin Input Current	I_{FB}	V_{FB} = 1.3V			1	100	nA
Under-Voltage Lockout	V_{UVLO}	V_{IN} rising		1.75	2.12	2.5	V
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) to 40V, I_{OUT} = 1mA			0.0003	0.01	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT} \times V_{OUT}}$	I_{OUT} = 1mA to 300mA			0.00005	0.0015	%/mA
Dropout Voltage	V_{DROP}	V_{OUT} = 95% × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ ≥ 3.3V	I_{OUT} = 150mA		220	450	mV
			I_{OUT} = 300mA		450	900	
Output Current Limit	I_{LIMIT}	V_{IN} = V_{OUT} + 3V, V_{OUT} = 90% × $V_{OUT(NOM)}$		0.51	1.1		A
Output Short-Circuit Current	I_{SHORT}	V_{IN} = $V_{OUT(NOM)}$ + 3V, V_{OUT} = 0V			470		mA
Ground Pin Current	I_{GND}	I_{OUT} = 0mA			3.8	8	μA
		I_{OUT} = 300mA			110	260	
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 3V to 40V			0.3	1.5	μA
EN Pin High-level Input Voltage	V_{IH}	V_{IN} = 3V to 40V		1.5		40	V
EN Pin Low-level Input Voltage	V_{IL}	V_{IN} = 3V to 40V		0		0.3	V
EN Pin Input Current	I_{EN}	V_{EN} = 0V, V_{IN} = 40V			0.01	1	μA
		V_{EN} = 40V, V_{IN} = 40V			0.1	1	
Output Discharge Resistance	R_{DIS}	V_{EN} = 0V			215		Ω
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 90% × $V_{OUT(NOM)}$	$V_{OUT(NOM)}$ = 1.25V		1.1	1.8	ms
			$V_{OUT(NOM)}$ = 3.3V		1.1	2.0	
			$V_{OUT(NOM)}$ = 5V		1.4	2.5	
PG High Threshold	PG_{HTH}	V_{OUT} rising		90	94	97	$\%V_{FB}$
PG Low Threshold	PG_{LTH}	V_{OUT} falling		84	87	90	$\%V_{FB}$
PG Pin Low-Level Output Voltage	$V_{PG(LO)}$	I_{SINK} = 1mA			0.1	0.3	V
PG Pin Leakage Current	$I_{PG(LKG)}$	V_{PG} = 5V			1	500	nA
PGDL Charging Current	I_{DLY}	V_{PGDL} = 1V			5	10	μA
PGDL Rising Threshold	V_{HDLY}			1.3	1.6	1.9	V
PGDL Falling Threshold	V_{LDLY}			0.2	0.35	0.7	V
PG Delay Time	t_{PGD}	C_{PGDL} = 47nF			12	30	ms
PG Reaction Time	t_{PGR}	C_{PGDL} = 47nF			0.6		μs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, T_J = -40℃ to +125℃ [(1)], typical values are at T_A = +25℃, unless otherwise noted.)

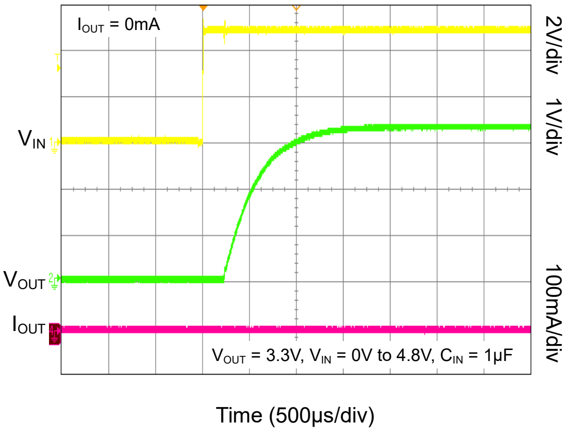
PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio	PSRR	$V_{OUT(NOM)}$ = 3.3V, I_{OUT} = 10mA	f = 100Hz		62		dB
			f = 1kHz		46		
			f = 100kHz		43		
Output Voltage Noise	e_n	f = 10Hz to 100kHz, $V_{OUT(NOM)}$ = 1.25V, I_{OUT} = 10mA			54		$μV_{RMS}$
Thermal Shutdown Temperature	T_{SHDN}				160		℃
Thermal Shutdown Hysteresis	$ΔT_{SHDN}$				30		℃

NOTE:
1. Tested under pulse load conditions, so $T_J ≈ T_A$.

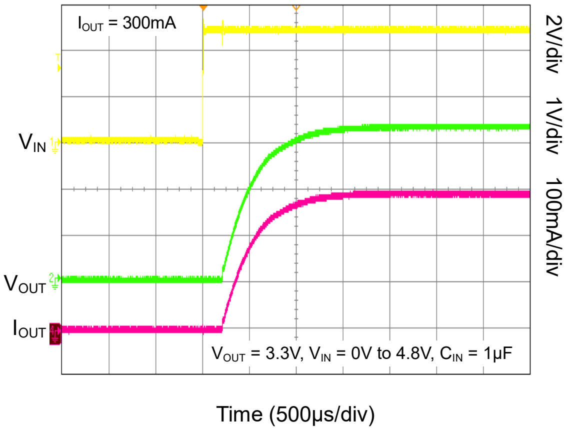
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

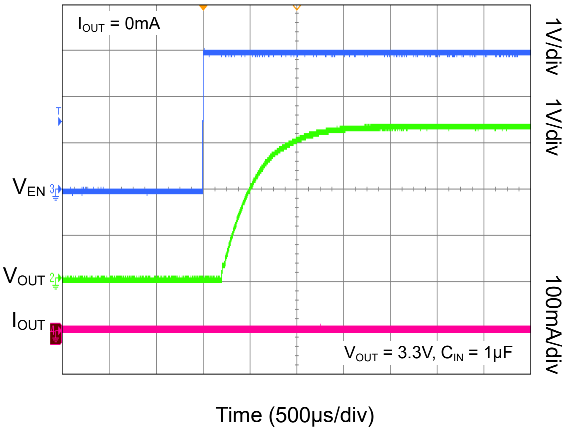
V_{IN} Power-Up Response



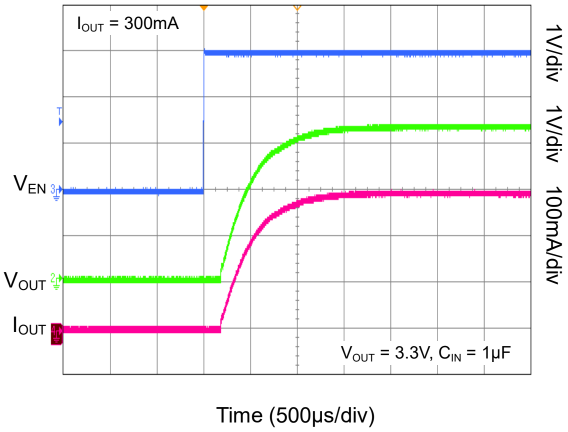
V_{IN} Power-Up Response



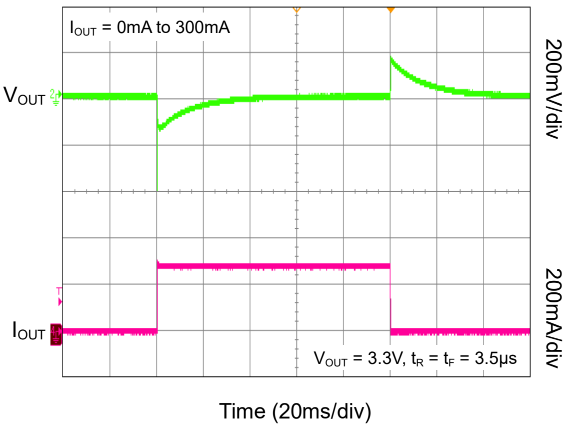
Enable Turn-On Response



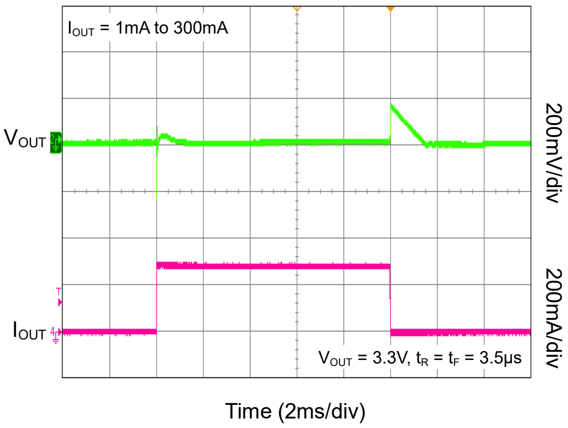
Enable Turn-On Response



Load Transient Response



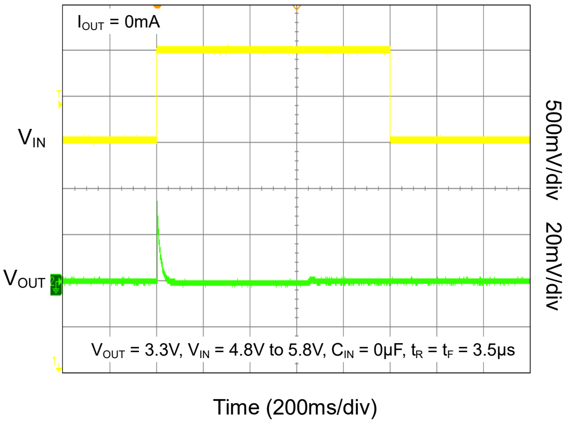
Load Transient Response



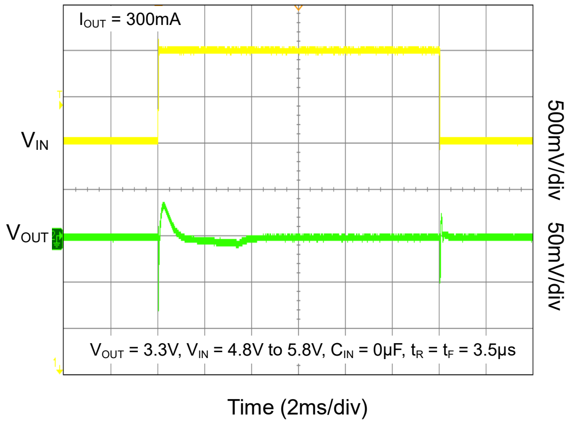
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

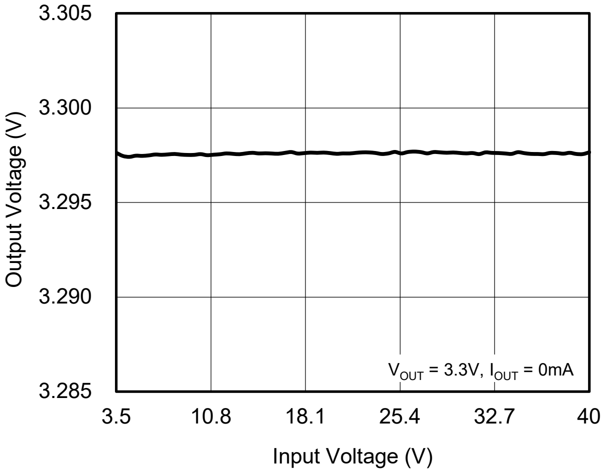
Line Transient Response



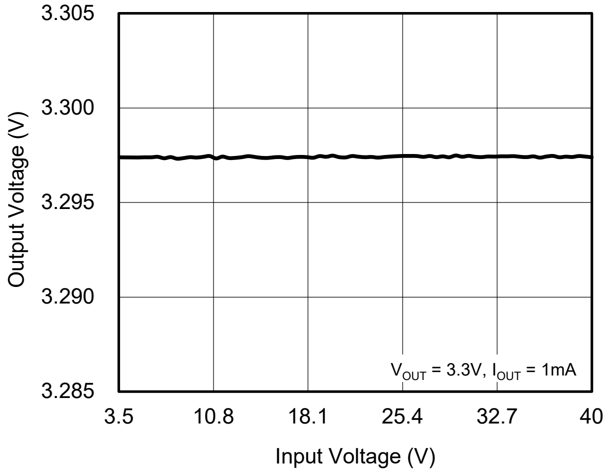
Line Transient Response



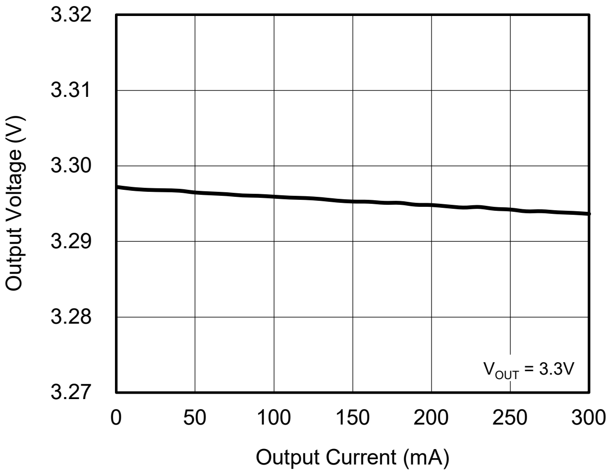
Output Voltage vs. Input Voltage



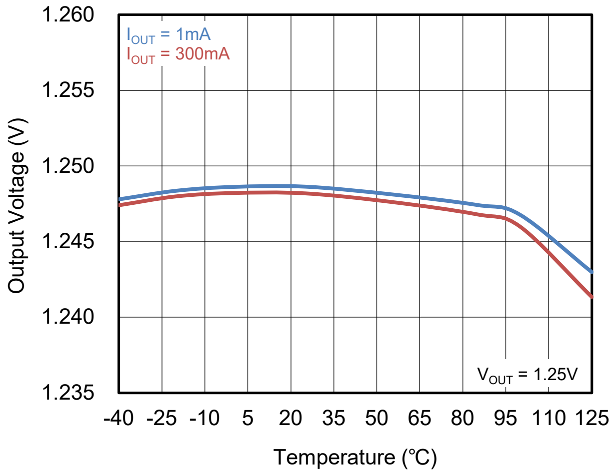
Output Voltage vs. Input Voltage



Output Voltage vs. Output Current

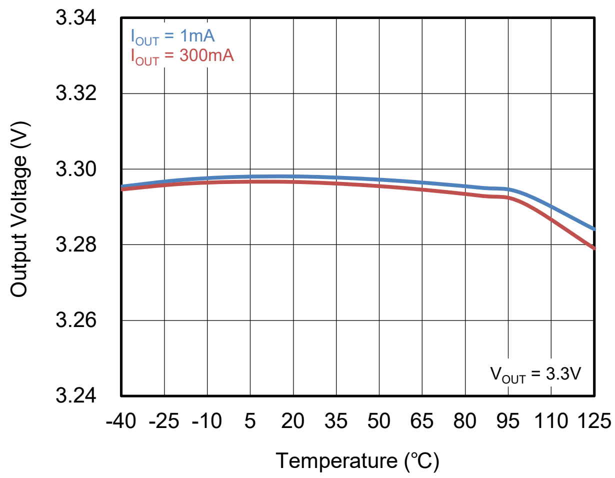


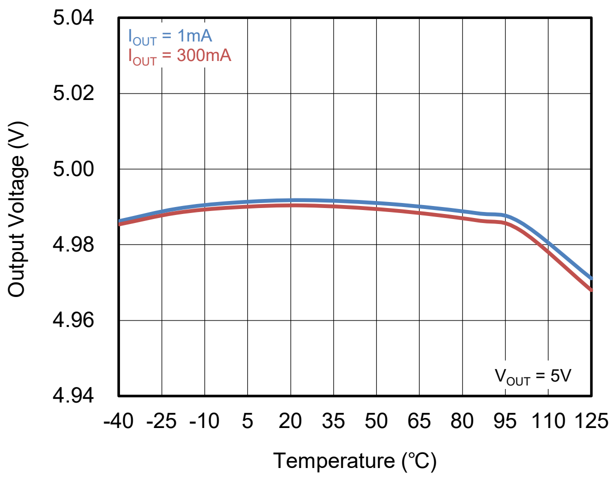
Output Voltage vs. Temperature

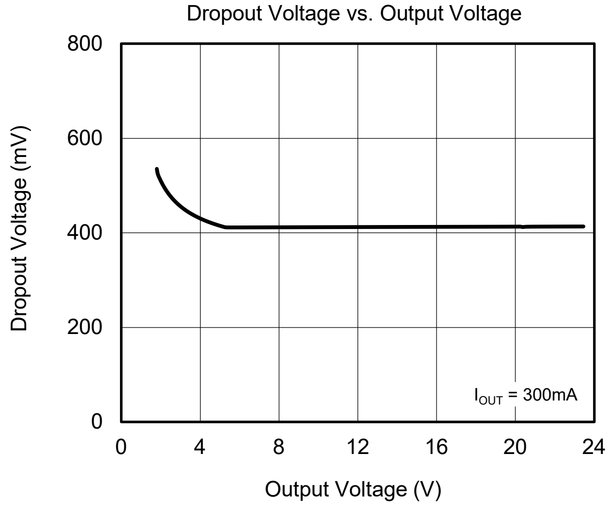


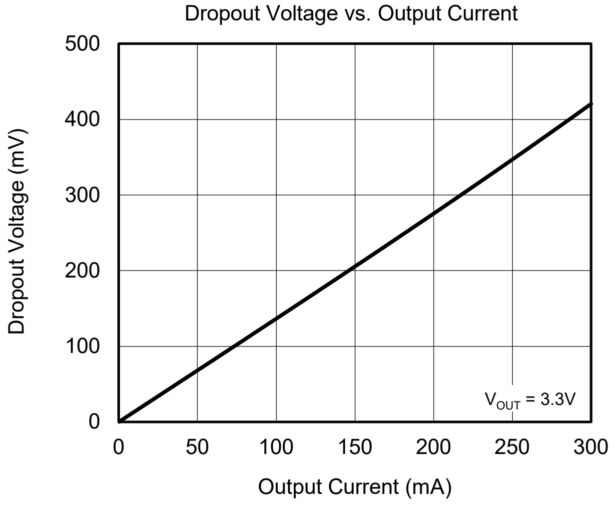
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

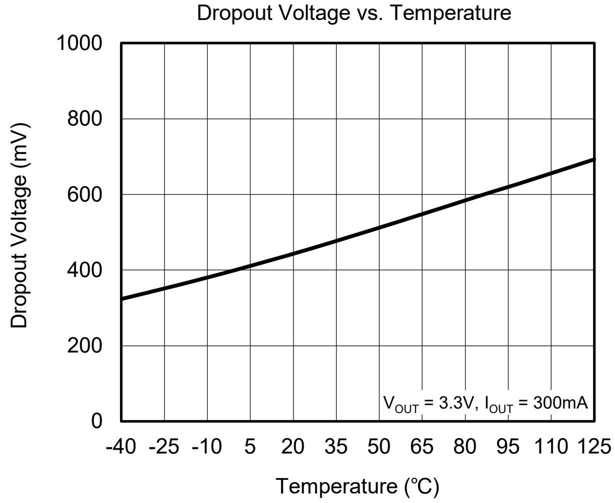
T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

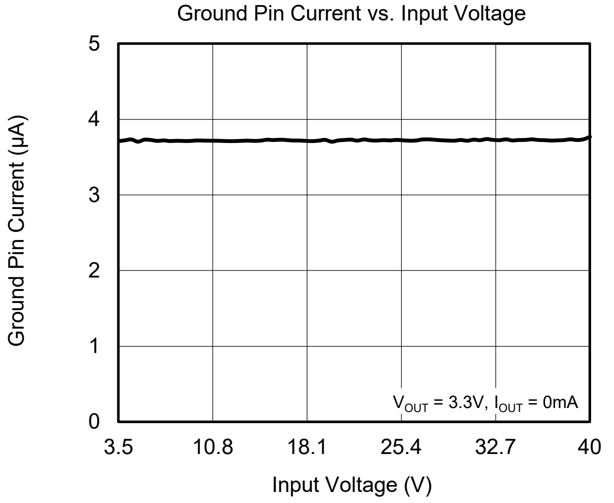






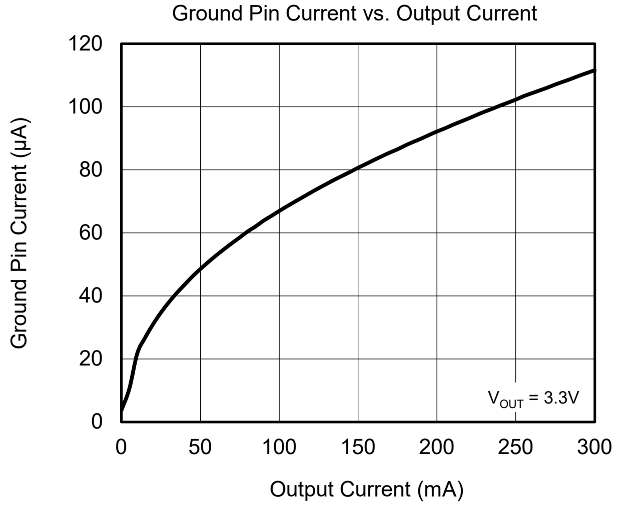


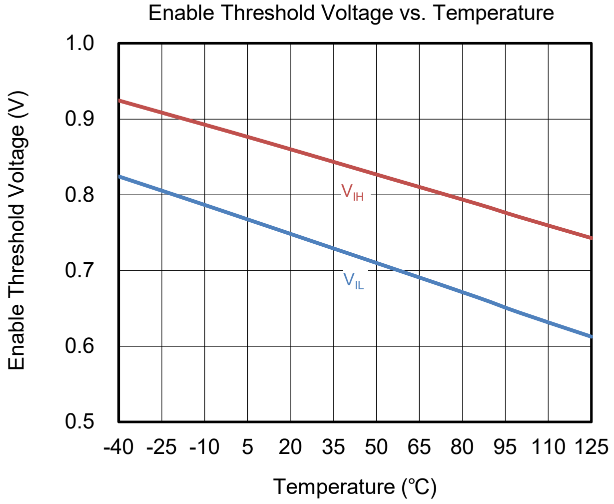


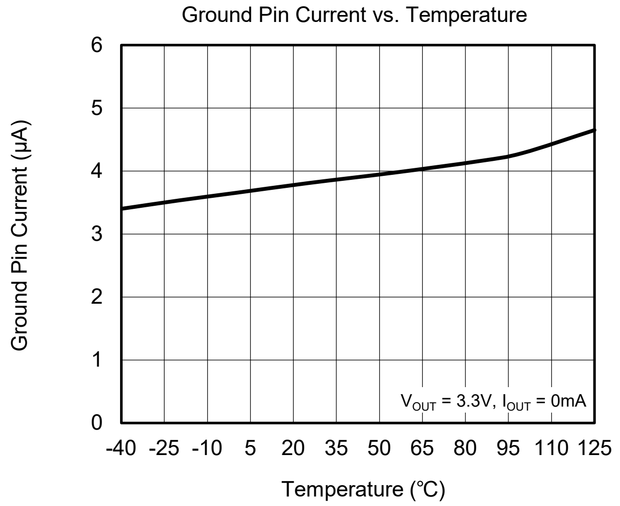


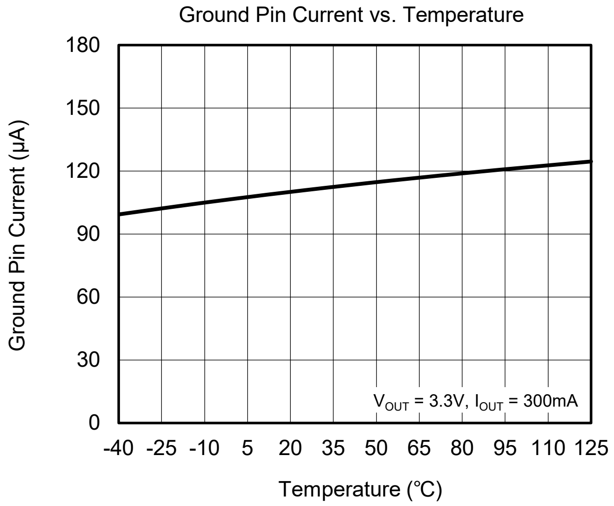
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

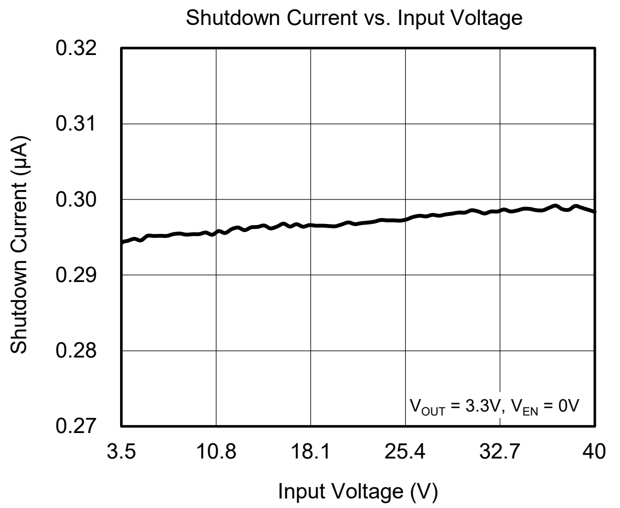
T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

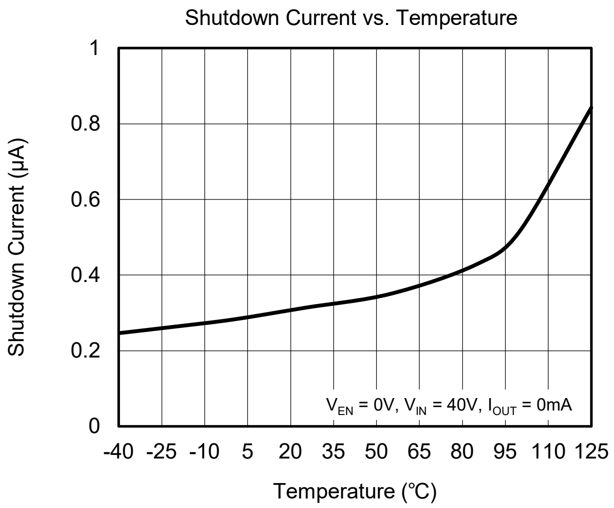






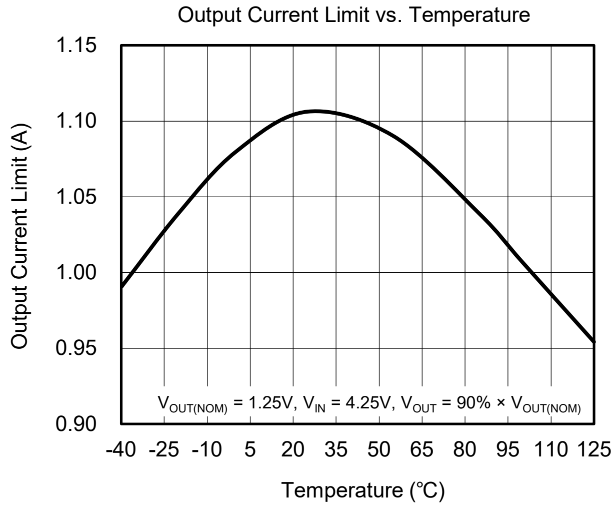


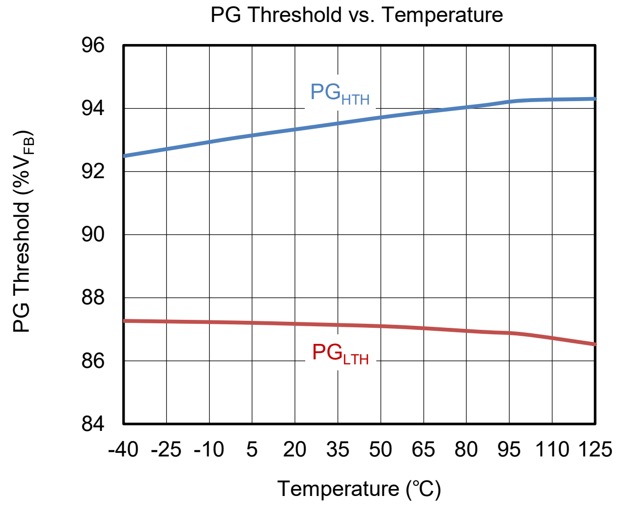


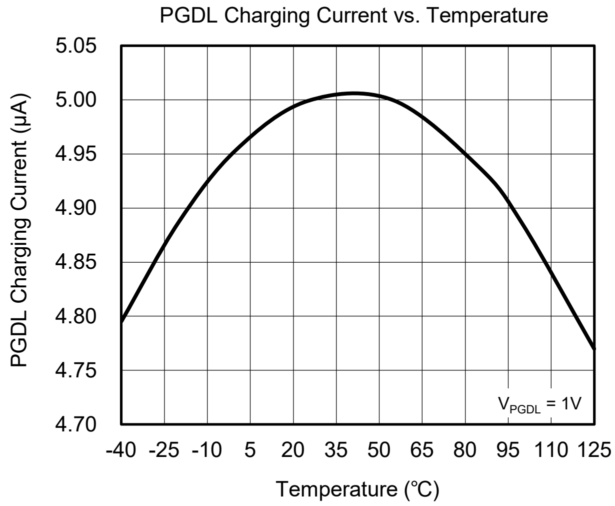


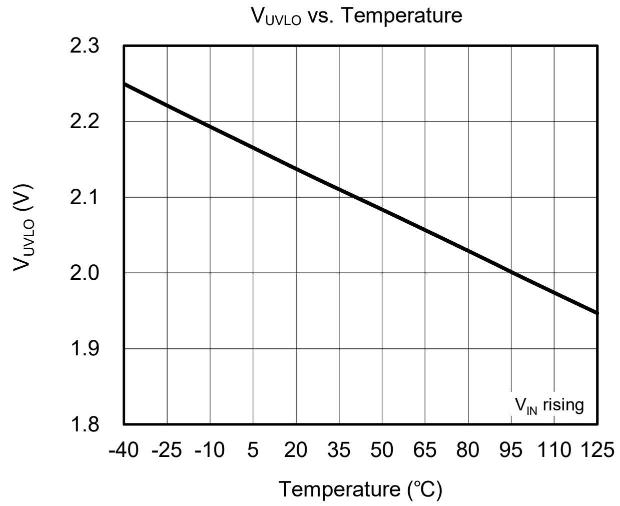
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

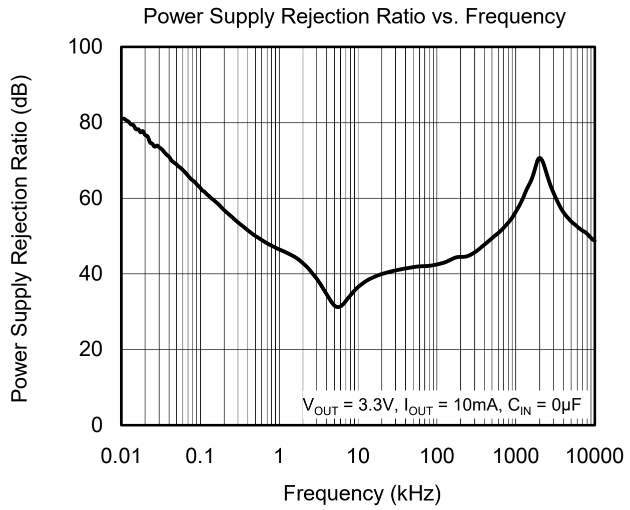
T_J = +25℃, V_{IN} = ($V_{OUT(NOM)}$ + 1.5V) or 3V(whichever is greater), V_{EN} = V_{IN}, C_{IN} = 10μF, C_{OUT} = 10μF, C_{FF} = 0nF, unless otherwise noted.

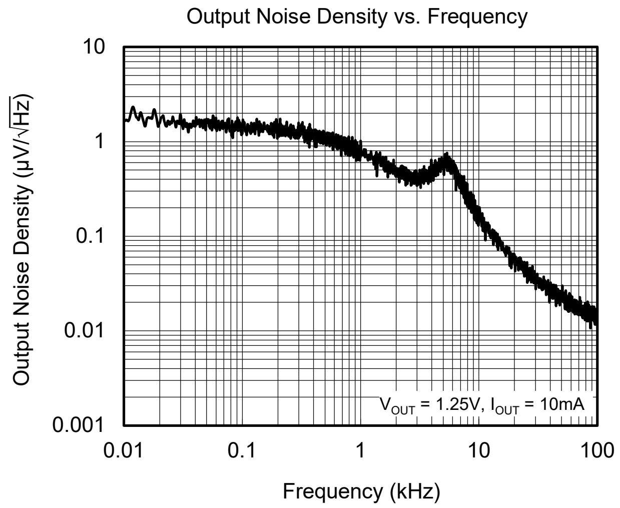












APPLICATION INFORMATION

The SGM2238xQ is a high voltage, low quiescent current and low dropout LDO and provides 300mA output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2238xQ useful in a variety of applications. The SGM2238xQ provides protection functions for output overload and overheating.

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 2.2μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings. For C_{OUT} with larger capacitance, it is recommended to choose the larger capacitance C_{IN}.

Output Capacitor Selection (C_{OUT})

One or more output capacitors are required to maintain the stability of the LDO, and the output capacitors should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R and X5R ceramic capacitors as output capacitors. Ceramic capacitors have low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitors is affected by temperature, DC bias and package size.

For example, Figure 4 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10μF±10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

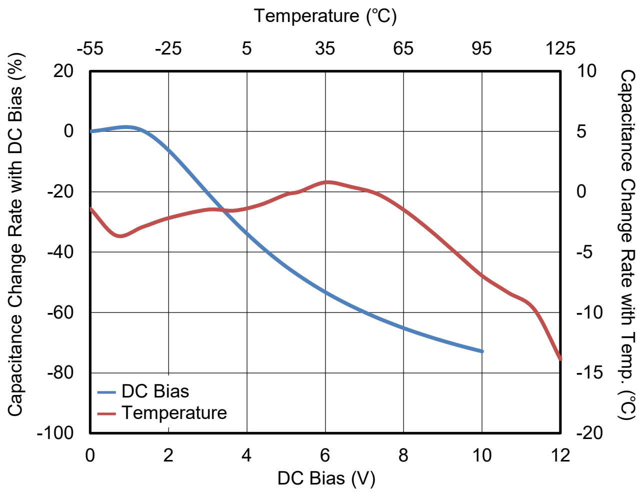


Figure 4. Capacitance vs. DC Bias and Temperature Characteristics

The SGM2238xQ requires a minimum effective capacitance of 1μF for C_{OUT} to ensure stability. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Adjustable Regulator

The output voltage of the SGM2238-ADJQ can be adjusted from 1.25V to 24V. The FB pin will be connected to two external resistors as shown in Figure 5. The output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

where:

V_{OUT} is output voltage and V_{FB} is the internal voltage reference, V_{FB} = 1.25V. R_1 and R_2 can be calculated for any output voltage range using equation 1. It is recommended that the R_2 resistance be less than 40kΩ and C_{FF} = 1nF.

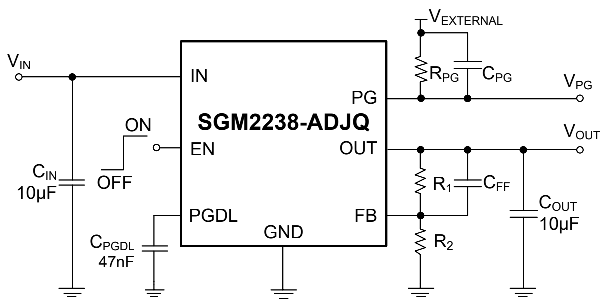


Figure 5. Adjustable Output Voltage Application

APPLICATION INFORMATION (continued)

Enable Operation

The SGM2238xQ uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.3V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 215Ω (TYP) resistor and the PG output is pulled down.

When the EN pin voltage is higher than 1.5V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

Power-Good Function

The SGM2238xQ features PG function for monitoring the feedback voltage, so as to reflect the state of the output voltage. When the output voltage is lower than PG_{LTH}, the PG pin open-drain engages and pulls the PG pin close to GND. When the output voltage is higher than PG_{HTH}, the PG pin is indicated as high impedance. Connecting the PG pin to an external power supply via a pull-up resistor enables any downstream device to receive a power-good valid logic signal for sequencing. The resistance of the pull-up resistor is recommended to be between 10kΩ and 100kΩ.

Both the fixed-voltage and adjustable-voltage versions of the SGM2238xQ integrate an internal feedforward capacitor ($C_{FF\_INTERNAL}$, typical value 10pF). When an external feed-forward capacitor (C_{FF}) is added in application, the total LDO startup time constant increases by approximately $3 \times R_1 \times (C_{FF} + C_{FF\_INTERNAL})$.

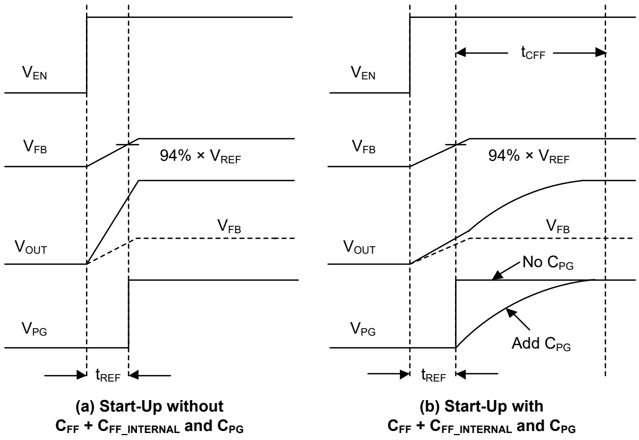
If the Power-Good (PG) output time constant remains unchanged, the PG signal may not accurately indicate whether V_{OUT} has reached the expected voltage. To ensure a valid PG output, the following design configurations must be implemented to match the time constants.

Add a PG delay capacitor (C_{PG}) and connect C_{PG} in parallel with the PG pull-up resistor (R_{PG}) refer to Figure 5. Ensure the following condition is met: $3 \times R_{PG} \times C_{PG} \geq 3 \times R_1 \times (C_{FF} + C_{FF\_INTERNAL})$.

For the adjustable version, refer to Figure 5 for R_1 selection. For the fixed version, calculate R_1 as follows:

$$R_1 = \left(\frac{V_{OUT(NOM)}}{1.25} - 1\right) \times 12M\Omega \quad (2)$$

Figure 6 shows the differences in PG signals when C_{FF} and C_{PG} are added. In Figure 6, t_{REF} is the time that takes for the V_{FB} voltage to rise from 0V to 94% × V_{REF}, t_{CFF} is the startup time contributed by C_{FF} and $C_{FF\_INTERNAL}$.



NOTE: Both (a) and (b) are under the condition of C_{PGDL} = 0nF.

Figure 6. Typical Power-Good Timing Diagram

The power-good (PG) delay period is determined by the external capacitor (C_{PGDL}) connected to the PGDL pin. When the V_{FB} voltage reaches PG_{HTH} of the target, this adjustable delay function configures the required wait time before the PG pin asserts high and achieved by connecting an external capacitor between the PGDL pin and GND. When the PGDL pin is left floating, the delay time defaults to 40μs. If a capacitor is connected between the PGDL pin and GND, the delay time is defined by the following equation:

$$t_{PGD} = 40\mu s + C_{PGDL} \times \frac{V_{HDLY}}{I_{DLY}} \quad (3)$$

Adjust the programmable PG delay (t_{PGD}) (adjustable version only), if using the adjustable PG delay feature, set: $t_{PGD} \geq 3 \times R_1 \times (C_{FF} + C_{FF\_INTERNAL})$.

The PG output is pulled down when the SGM2238xQ is in one of the following states, including disabled, thermal shutdown and UVLO.

APPLICATION INFORMATION (continued)

Reverse Current Protection

The power transistor has an inherent body diode. This body diode will be forward biased when V_{OUT} > (V_{IN} + 0.3V). When V_{OUT} > (V_{IN} + 0.3V), the reverse current flowing from the OUT pin to the IN pin will damage the SGM2238xQ. If reverse current protection function is needed in application, the circuit in Figure 7 is good solution to provide reverse current protection.

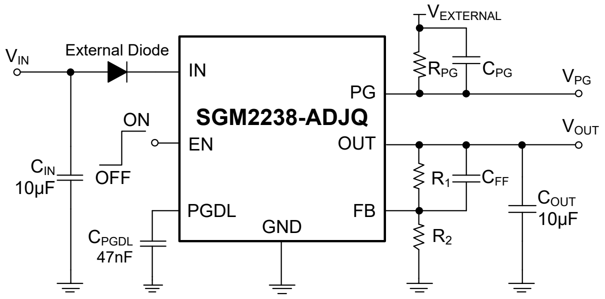


Figure 7. Reverse Protection Reference Design

Output Current Limit Protection

When overload events happen, the output current is internally limited to 1.1A (TYP). When the OUT pin is shorted to ground, the output current is internally limited to 470mA (TYP).

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2238xQ will be in shutdown state and it will remain in this state until the die temperature decreases to +130℃. When the device enters thermal shutdown, the PG output is pulled low.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2238xQ can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2238xQ is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \tag{4}$$

Layout Guidelines

To get good PSRR, low output noise and high transient response performance, the input and output bypass capacitors must be placed as close as possible to the IN pin and OUT pin separately.

REVISION HISTORY

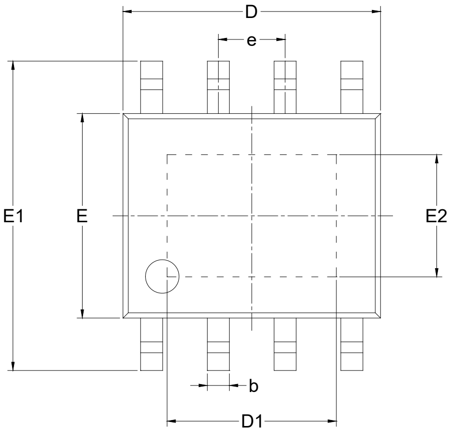
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

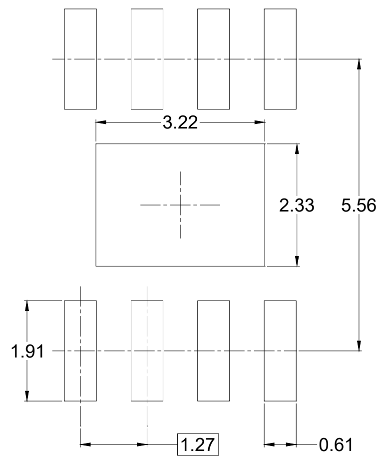
JULY 2026 – REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings section	3

AUGUST 2025 – REV.A to REV.A.1	Page
Added SGM2238-1.8Q/2.5Q/3.3Q to Package/Ordering Information section	2
Updated Absolute Maximum Ratings section	3
Updated Electrical Characteristics section	6, 7

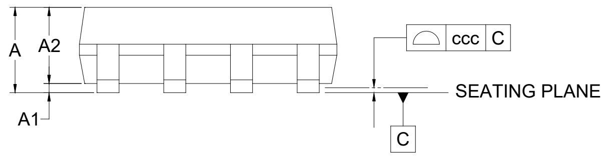
Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

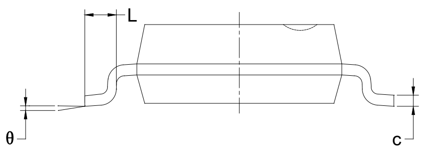
PACKAGE OUTLINE DIMENSIONS
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



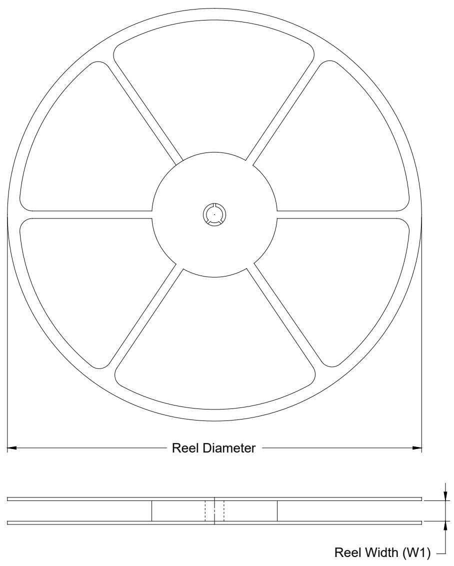


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

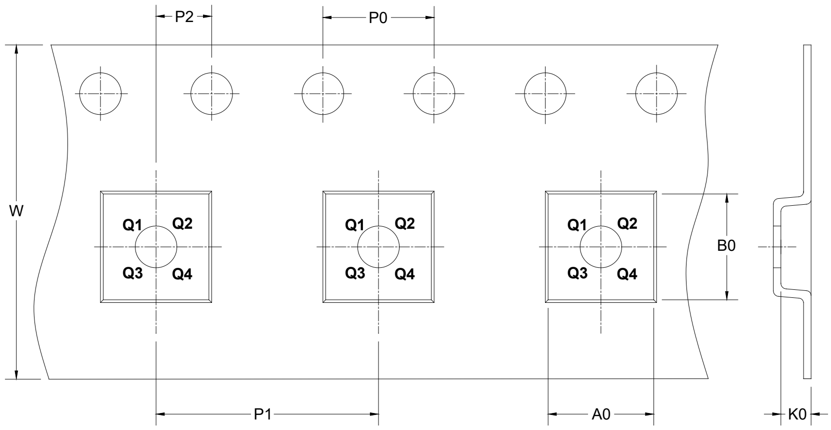
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

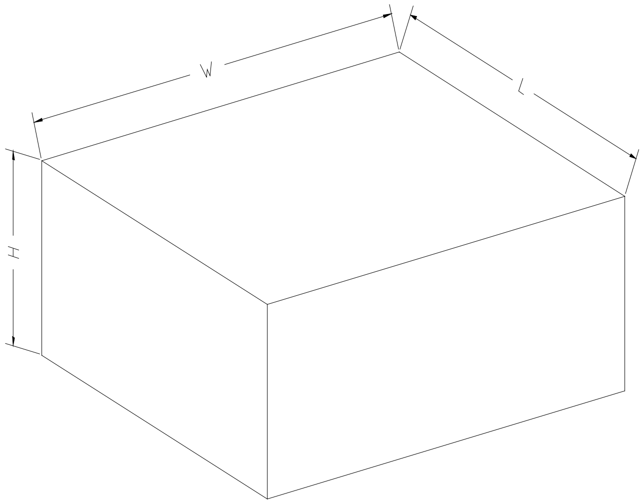
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002