SGM41620

I²C Controlled Single Cell High Efficiency 8A Switched Cap and 4A Switched Mode Buck Charger with PD PHY, Dual-Channel LED Driver Integrated

FEATURES

- 8A Switched Cap Charger
  - 96.5% Efficiency for 6A Fast Charge (V_{BAT} = 4.4V)
  - Support 2:1 and 1:1 Fast Charging
  - Integrated VAC, VBUS, BAT, BATSNS OVP
  - Integrated IBUS, Switching MOSFET Cycle-by-Cycle Current Protection
  - CFLY Short, BAT Short, VBUS Short and VBUS In-Range Protection
- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 3.9V to 13.5V Operating Input Voltage Range
  - 22V Absolute Maximum VBUS Voltage Rating
  - Programmable Input Current Limit and Dynamic Power Management
  - Programmable Input Voltage Limit (VINDPM) and VINDPM Tracking of Battery Voltage
  - Switching MOSFET Cycle-by-Cycle Current Limit
  - High Battery Discharge Efficiency with 15mΩ Switch
  - Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
  - ±0.5% Charge Voltage Regulation (8mV/Step)
  - ±5% Charge Current Regulation at 2A
  - ±5.5% Input Current Regulation at 0.9A
  - Fully Integrated Switches, Current Sense and Compensation
  - Up to 3.25A OTG Output Current
  - 20μA Ship Mode Low Battery Leakage Current
- 10 Channels 12-Bit ADC (VAC, VBUS, IBUS, VBAT, VBATSNS, VSYS, IBAT, TSBUS, TSBAT, TDIE)
- Dual-Channel LED Driver
  - Up to 1.5A Flash Current for Each Channel
  - Up to 500mA Torch Current for Each Channel
  - Can Work Simultaneously
- BC1.2 & USB PD & UFCS PHY
  - Support USB PD3.1 PPS except Fast Role Swap Function
  - Cable Plug and Orientation Detection
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adapters
  - Integrated UFCS PHY

APPLICATIONS

Smartphone
Tablet PC

SIMPLIFIED SCHEMATIC

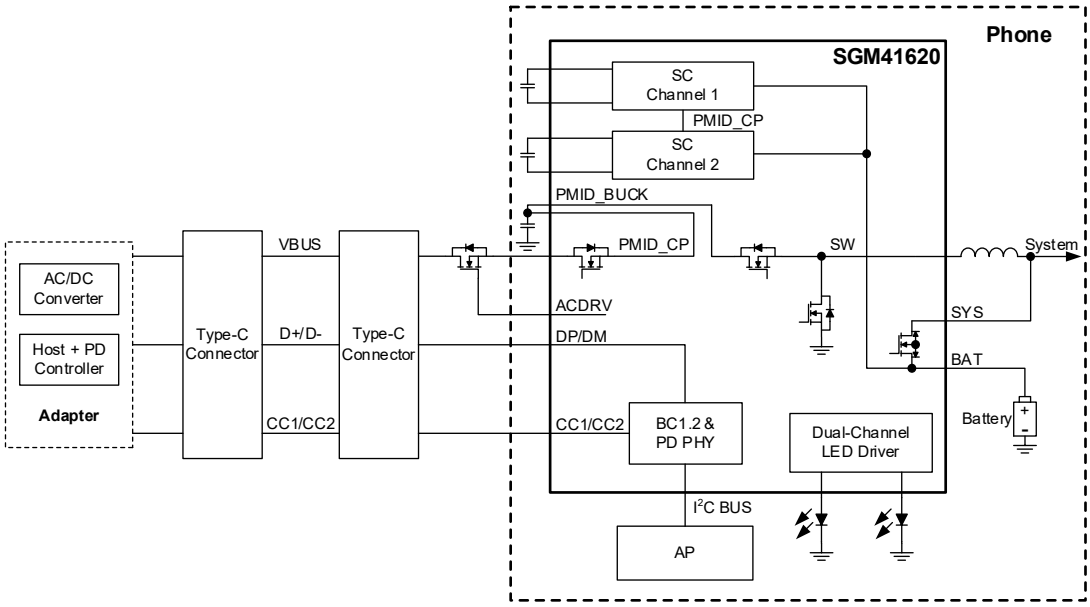


Figure 1. Simplified Schematic

GENERAL DESCRIPTION

The SGM41620 is a highly integrated charging solution for smartphone and tablet PC, which includes a 4A switched mode Buck charger, 8A switched cap fast charger, USB PD3.1 PHY (PPS) and dual-channel LED driver etc.

The 4A switched mode Buck charger is a NVDC system power path management device with integrated converter and power switches for use with single-cell Li-Ion or Li-polymer batteries. This highly integrated 4A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. I^2C programming makes it a very flexible powering and charger design solution.

The 8A switched cap fast charger can be configured to the divider mode and bypass mode by I^2C interface. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.2V to 11V input voltage range (VBUS) from smart wall adapters or wireless charger. A two-channel switched capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. Necessary protection features for safe charging performance; including over-voltage protection (by Q_{OVP} external switch).

The dual-channel LED driver provides a tight solution of LED drive on the mobile phone or other portable device. The maximum source current for driving flash LED can reach 1.5A. When two rails LED work simultaneously, the maximum total source current can reach 2A. Control is done via an I^2C-compatible interface. This includes adjustment of the flash and torch current levels, changing the flash timeout duration, and changing the current limit. Additionally, there are flag and status bits that indicate flash current timeout, LED short, device thermal shutdown, etc.

The SGM41620 also has a built-in 12-bit effective resolution ADC, which can be used to monitor the VBAT, VBATSNS (V_{BATP} - V_{BATN}), IBAT (charging current through BATFET Q4 for Buck charger), VAC, VBUS, VSYS, IBUS, TSBUS, TSBAT, and TDIE for better management of the charging process.

The SGM41620 integrates a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection. Upon cable attachment, the device performs cable detection according to the USB Type-C specification. It also communicates on the CC wire using the USB PD protocol.

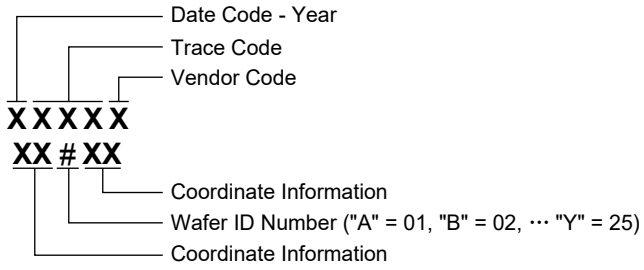
The SGM41620 integrates a UFCS (Universal Fast Charging Specification) controller, by which host can communicate with the UFCS supported adaptor to perform the fast charging for the mobile devices.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41620	WLCSP-3.8×3.86-64B	-40℃ to +85℃	SGM41620YG/TR	SGM 41620 XXXXX XX#XX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
- VAC ..... -2V to 36V
- VBUS ..... -2V to 22V
- SW ..... -2V to 16V
- PMID_CP, PMID_BUCK, BST3, FLASH_VDD ... -0.3V to 22V
- BST1, BST2 ..... -0.3V to (PMID+5.5) V
- BST3 to SW ..... -0.3V to 6V
- CFH1, CFH2 to VOUT ..... -0.3V to 6V
- CFL1, CFL2, BAT, SYS, PMID_CP - BAT (Voltage Divider Mode) ..... -0.3V to 6V
- ACDRV ..... -0.3V to 22V
- LED1, LED2, TORCH_VDD ..... -0.3V to 6V
- CC1, CC2 ..... -0.3V to 24V
- SDA, SCL, DP, DM, VCONN, nINT, PD_nINT, nSYS_OK, REGN, CC_DIR, nRST ..... -0.3V to 6V
- BATP, BATN ..... -0.3V to 6V
- RST0, RST1, V2X ..... -0.3V to 16V
- EDL_TSBUS, TSBAT ..... -0.3V to 6V

Output Sink Current, nINT 6mA

Package Thermal Resistance
- WLCSP-3.8×3.86-64B, θ_{JA} ..... 33.1℃/W
- WLCSP-3.8×3.86-64B, θ_{JB} ..... 7.7℃/W
- WLCSP-3.8×3.86-64B, θ_{JC} ..... 7.5℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±2000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Voltage Range
- VBUS ..... 13.5V (MAX)
- BAT, SYS ..... 5V (MAX)
- CFHx - BAT, CFL1, CFL2 ..... 5V (MAX)
- PMID_CP - BAT (Voltage Divider Mode) ..... 5V (MAX)
- LED1, LED2 ..... 5.5V (MAX)
- Battery Voltage, V_{BATOP} ..... 4.856V (MAX)

I_{CHG_OP} (Buck Charger) ..... 4A (MAX)

I_{CHG_OP} (Voltage Divider Mode for Fast Charger) .... 8A (MAX)

Discharging Current (Continuous), I_{BATOP} ..... 6A (MAX)

Discharging Current (1s Pulse), I_{BATOP} ..... 10A (MAX)

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

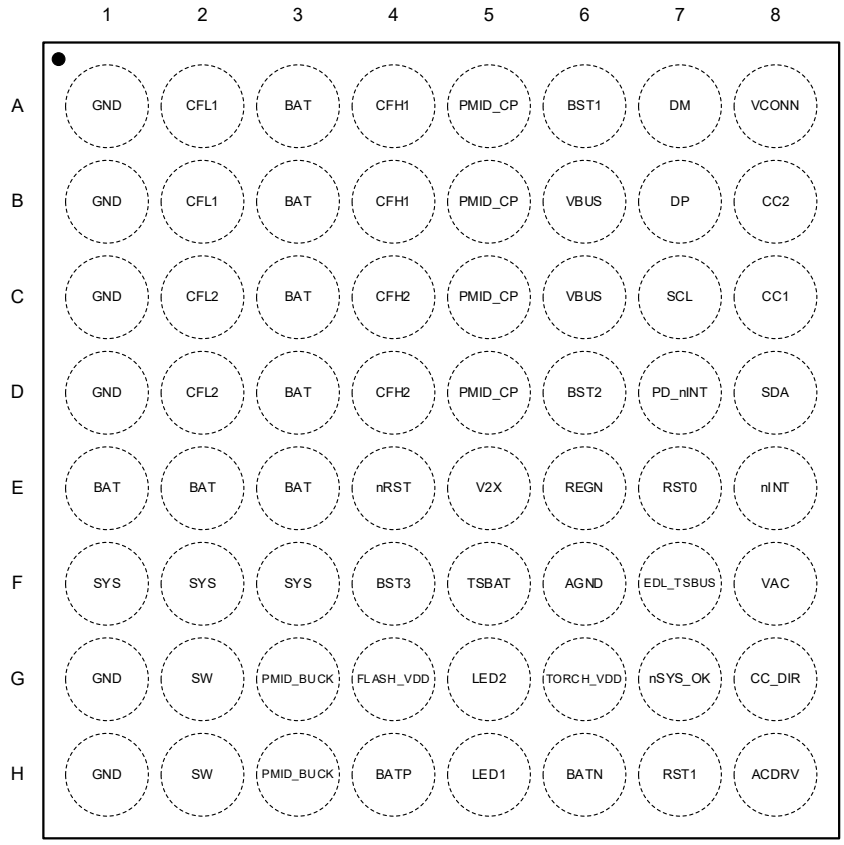
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.8×3.86-64B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1, B1, C1, D1, G1, H1	GND	P	Power Ground.
A2, B2	CFL1	P	Channel-1 Flying Capacitor Negative Pins. Connect three 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device.
A3, B3, C3, D3, E1, E2, E3	BAT	P	Battery Positive Terminal Pins. Use two 10μF capacitors between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
A4, B4	CFH1	P	Channel-1 Flying Capacitor Positive Pins. Connect three 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device.
A5, B5, C5, D5	PMID_CP	P	The Input to the Power Stage for Switched Cap Charger. Connect a 10μF capacitor to PMID_CP pin as close as possible. This pin should be connected to PMID_BUCK on PCB with copper plane.
A6	BST1	AIO	Channel-1 Bootstrap Pin. It is the BST pin to supply Q_{CH1} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH1.
A7	DM	AIO	Negative Line of the USB Data Line Pair.
A8	VCONN	P	VCONN Supply Input. The recommended voltage is in range from 3V to 5.5V. If VCONN is not required in the system, it is recommended to connect to GND.
B6, C6	VBUS	P	Charger Input (VIN). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID_CP pins. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device.
B7	DP	AIO	Positive Line of the USB Data Line Pair.
B8	CC2	AIO	Type-C Connector Configuration Channel 2. It is used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols and configured as the output of VCONN supply.
C2, D2	CFL2	P	Channel-2 Flying Capacitor Negative Pins. Connect three 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device.
C4, D4	CFH2	P	Channel-2 Flying Capacitor Positive Pins. Connect three 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device.
C7	SCL	DI	I^2C Interface Clock Line. Connect SCL to the logic high rail through a pull-up resistor (typical 10kΩ). The IC works as a slave.
C8	CC1	AIO	Type-C Connector Configuration Channel 1. It is used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols and configured as the output of VCONN supply.
D6	BST2	AIO	Channel-2 Bootstrap Pin. It is the BST pin to supply Q_{CH2} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH2.
D7	PD_nINT	DO	Open-Drain Interrupt Output. Connect the PD_nINT to a logic high rail through a 10kΩ resistor. Pull the PD_nINT pin low to notify host to read PD events.
D8	SDA	DIO	I^2C Interface Data Line. Connect SDA to the logic high rail through a pull-up resistor (typical 10kΩ).
E4	nRST	DO	Push-Pull Configuration. Pull low to GND when the device enters ship mode. Pull high to internal pull-up and keep high level when exit ship mode command is confirmed.
E5	V2X	P	Device Power Input from the Positive Terminal of 2-Cell Battery. For 1-cell battery system, short this pin to BAT pin. For 2-cell battery system, V2X is connected to 2-cell battery positive terminal and used to power the chip in ship mode.
E6	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Connect a 4.7μF (10V rating) ceramic capacitor from REGN pin to GND. The capacitor should be placed close to the IC.
E7	RST0	AI	Reset Input or BATFET On/Off Control Input. When connect to the power key, if this pin and RST1 are low at the same time, nRST pin will switch to low for 100ms if T_PD_nRST = 0, which is used for hardware reset. RST0 is active low. Internal pull-up for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn on the BATFET, a logic low pulse with a duration of $t_{SHIPMODE}$ (2s TYP) can be applied to RST0. When VBUS source is not connected, a logic low pulse with a duration of t_{SYS_RST} (10s TYP) for both RST0 and RST1 resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (200ms TYP) and then goes back to provide a full power reset for system.
E8	nINT	DO	Open-Drain Interrupt Output. Connect the nINT to a logic high rail through a 10kΩ resistor. The nINT pin sends an active low, 256μs pulse to the host to report charger device status and fault.
F1, F2, F3	SYS	P	Connection Point to Converter Output. SYS is connected to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect two 10μF capacitors between SYS pin and GND close to the device.
F4	BST3	AIO	High-side Driver Positive Supply. It is internally connected to the bootstrap diode cathode. Use a 47nF ceramic capacitor (C_{BOOT}) from SW pin to BTS3 pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
F5	TSBAT	AI	Temperature Qualification Voltage Input (Supports JEITA Profile). Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charge suspends if TSBAT voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC or TSBAT pin function is not needed, use a 10kΩ/10kΩ pair for the resistor divider.
F6	AGND	P	Analog Ground Pin (reference for low current signals).
F7	EDL_TSBUS	AIO	EDL Output by Default. Push-Pull Configuration. When plug in debug cable, it will output programmable low or high level to force AP reboot. This pin can be configured as bus temperature sense input pin when EDL_TSBUS_SEL bit is set to 1.
F8	VAC	AI	Input Voltage Sense Pin.
G2, H2	SW	P	Switching Node Output. Connect SW pins to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BST3 pin.
G3, H3	PMID_BUCK	P	The Input to the Power Stage for Switched Mode Buck Charger. Connect a 10μF capacitor to PMID_BUCK pin as close as possible. These pins should be connected to PMID_CP on PCB with copper plane.
G4	FLASH_VDD	P	Input Source Pin for LED Flash Function.
G5	LED2	AO	Driver Output for LED2. Connect to LED anode.
G6	TORCH_VDD	P	Input Source Pin for LED Torch Function.
G7	nSYS_OK	DO	Buck Charger VSYS Soft-Start Finished Indication. Open-drain configuration. Pull low when $V_{VBUS\_PRESENT} < V_{VBUS} < V_{VBUS\_OVP}$ and switched mode Buck charger is working.
G8	CC_DIR	DO	CC Line Detection Output. Push-pull configuration. Output low when CC1 is connected to the CC of Type-C cable. Output high when CC2 is connected to the CC of Type-C cable.
H4	BATP	AI	Positive Input for Battery Voltage Sensing. Series 100Ω to negative terminal of battery pack.
H5	LED1	AO	Driver Output for LED 1. Connect to LED anode.
H6	BATN	AI	Negative Input for Battery Voltage Sensing. Series 100Ω to negative terminal of battery pack.
H7	RST1	AI	Reset Input 1. When connect to the volume key, if both this pin and RST0 are low for 10s, nRST switches to low, which is used for system reset. RST1 is active low, internal pull-up for maintaining the default high logic (whenever a source or battery is available).
H8	ACDRV	AO	Gate Driver for External MOSFET. The output voltage is 4.75V higher than the greater of VBUS and VAC voltages in normal state.

NOTE: P = power, AIO = analog input/output, AI = analog input, DI = digital input, DO = digital output, AO = analog output, DIO = digital input/output.

TYPICAL APPLICATION CIRCUITS

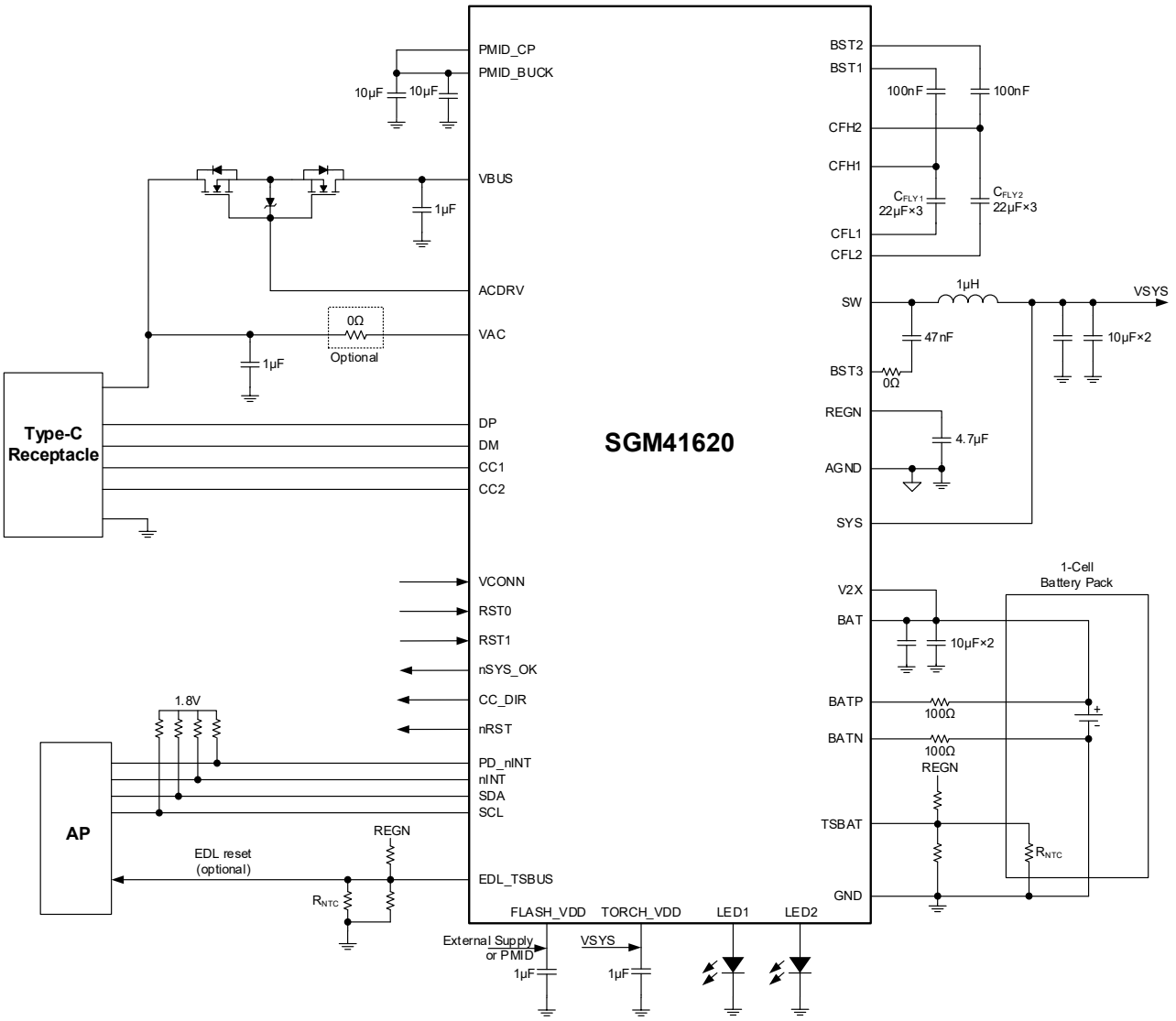


Figure 2. 1 Cell Battery Typical Application for SGM41620

TYPICAL APPLICATION CIRCUITS (continued)

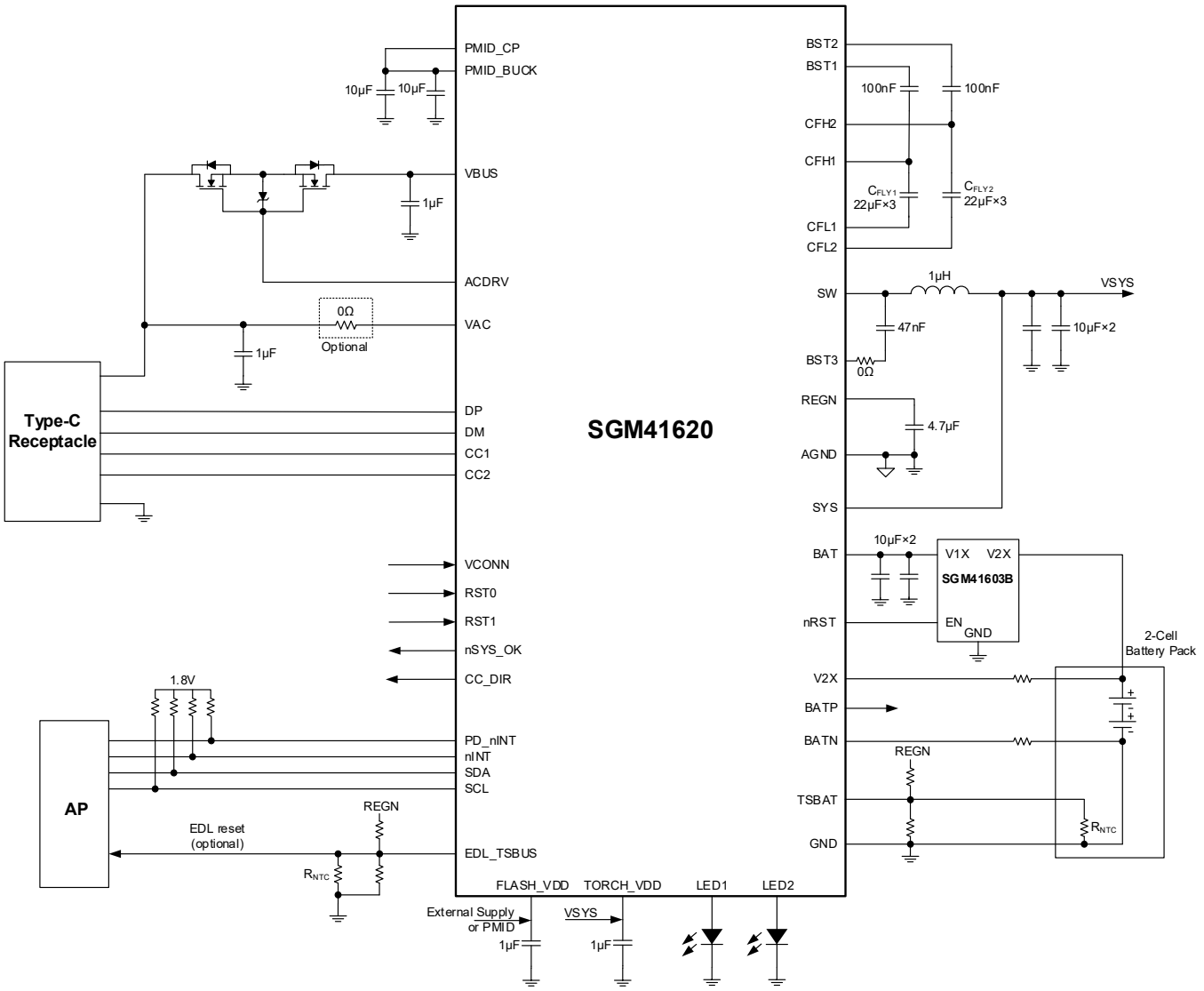


Figure 3. 2-Cell Battery Typical Application for SGM41620

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VBAT/V2X Quiescent Current	I_{Q_VBAT} I_{Q_V2X}	Ship mode V_{BAT} = 4.5V, Buck HIZ mode, no VBUS, BATFET disabled, ADC disabled, PD PHY in shutdown mode		20		μA
		Ship mode V_{V2X} = 9V, no VBUS, V_{BAT} = 0V, ADC disabled, PD PHY in shutdown mode		25		μA
		Ship mode V_{BAT} = 4.5V, Buck HIZ mode, no VBUS, BATFET disabled, ADC disabled, PD PHY CC in UFP mode		90		μA
		Ship mode V_{BAT} = 4.5V, Buck HIZ mode, no VBUS, BATFET disabled, ADC disabled, PD PHY CC in DRP mode		100		μA
		Standby mode V_{BAT} = 4.5V, Buck HIZ mode, no VBUS, BATFET enabled, ADC Disable, PD PHY CC in UFP mode		95		μA
		V_{VBUS} = 5V, V_{BAT} = 4.2V, after EOC, ADC disabled		35		μA
VAC Quiescent Current	I_{Q_VAC}	V_{VAC} = 5V, Buck HIZ mode and BATFET disabled, no battery, ADC disabled, ACDRV enabled		520		μA
		V_{VAC} > V_{VAC_UVLO}, V_{VBUS} > V_{BAT}, Buck switching, ADC disabled, not charging, V_{VAC} = 5V		4		mA
Battery Discharge Current in Boost Mode	I_{BOOST}	V_{BAT} = 4.2V, I_{VBUS} = 0A, converter switching		4.5		mA
House Keeping						
Pull-Down Current and Resistance						
VBUS Pull-Down Current	I_{VBUS_PD}	VBUS_PD_EN bit = 1		100		mA
VAC Pull-Down Current	I_{VAC_PD}	VAC_PD_EN bit = 1		50		mA
PMID_CP Pull-Down Resistor	$R_{PMID\_PD\_CP}$	PMID_PD_EN bit = 1		1		kΩ
Internal Threshold						
VAC for Active I²C, no Battery	V_{VAC_UVLO}	Rising threshold		2.7	2.9	V
		Falling hysteresis		280		mV
VAC to Turn on ACDRV	$V_{VAC\_PRESENT}$	Rising threshold		3	3.2	V
		Falling hysteresis		230		mV
VBUS for Active I²C, no Battery	V_{VBUS_UVLO}	Rising threshold		2.7	2.9	V
		Falling hysteresis		280		mV
VBUS for REGN Power Up and CP Charging Enable	$V_{VBUS\_PRESENT}$	Rising threshold		3	3.2	V
		Falling hysteresis		230		mV
VBAT for Active I²C, no Adaptor	V_{BAT_UVLO}	Rising threshold		2.25		V
		Falling hysteresis		300		mV
ACDRV						
ACDRV Drive Voltage	V_{ACDRV}	V_{VAC} = 8V, external FET gate drive voltage, measured from gate to VAC, with minimum 8nF C_{GS}, ACDRV enabled		4.75		V
Input Over-Voltage Protection						
VAC OVP	V_{VAC_OVP}	Range, rising threshold, VAC_OVP[2:0]	6.5		17	V
		Falling hysteresis		500		mV
		Comparator accuracy for 6.5V	-4		4	%
		Comparator accuracy for 11V to 17V	-3		3	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS OVP	V_{VBUS_OVP}	6V, rising threshold, VBUS_OVP[1:0] = 00		6		V
		Hysteresis		300		mV
		10V, rising threshold, VBUS_OVP[1:0] = 01		10		V
		Hysteresis		300		mV
		12V, rising threshold, VBUS_OVP[1:0] = 10		12		V
		Hysteresis		300		mV
		14V, rising threshold, VBUS_OVP[1:0] = 11		14		V
		Hysteresis		300		mV
		Comparator rising accuracy	-1.5		3.5	%
ADC Measurement						
ADC BUS Current Readable in Register 0x11 and 0x12	IBUS_ADC	Range	0		10.24	A
		LSB		2.5		mA
		Accuracy at I_{BUS} = 3A	-3		3	%
ADC VBUS Voltage Readable in Register 0x13 and 0x14	VBUS_ADC	VBUS pin voltage range	0		15.36	V
		LSB		3.75		mV
		Accuracy at V_{VBUS} = 8V (Initialization), T_J = +25℃	-1		1	%
ADC VAC Voltage Readable in Register 0x15 and 0x16	VAC_ADC	VAC pin voltage range	0		20.48	V
		LSB		5		mV
		Accuracy at V_{VAC} = 8V (Initialization), T_J = +25℃	-1.2		1.2	%
ADC VBAT Sense Voltage Readable in Register 0x17 and 0x18	VBATSNS_ADC	BATP-BATN pin voltage range	0		5.12	V
		LSB		1.25		mV
		Error at BATP-BATN = 4.4V (Initialization), T_J = +25℃	-2		12	mV
		Accuracy at BATP-BATN = 3.5V ~ 4.5V (Initialization), T_J = +25℃	-0.5		0.5	%
ADC VBAT Voltage Readable in Register 0x19 and 0x1A	VBAT_ADC	BAT pin voltage range	0		5.12	V
		LSB		1.25		mV
		Accuracy at V_{BAT} = 4V (Initialization), T_J = +25℃	-0.5		0.5	%
ADC IBAT Current Readable in Register 0x1B and 0x1C	IBAT_ADC (BATFET sense)	Range, charging current in Buck mode	0		5.12	A
		LSB		1.25		mA
		Accuracy at I_{BAT} = 4A	-5		5	%
ADC VSYS Voltage Readable in Register 0x1D and 0x1E	VSYS_ADC	SYS pin voltage Range	0		5.12	V
		LSB		1.25		mV
		Accuracy at V_{SYS} = 4V (Initialization), T_J = +25℃	-0.8		0.8	%
ADC TSBUS Pin Voltage Readable in Register 0x1F and 0x20	TSBUS_ADC	TSBUS pin voltage range	0.2		2.7	V
		ADC Range	0		50	%
		LSB		0.09766		%
		2V TSBUS pin voltage as percentage of REGN Accuracy (Initialization), T_J = +25℃	-1		1	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC TSBAT Pin Voltage Readable in Register 0x21 and 0x22	TSBAT_ADC	TSBAT pin voltage range	0.2		2.7	V
		ADC Range	0		50	%
		LSB		0.09766		%
		2V TSBAT pin voltage as percentage of REGN Accuracy (Initialization), T_J = +25℃	-1		1	%
ADC Die Temperature Readable in Register 0x23 and 0x24	TDIE_ADC	Range	0		150	℃
		LSB		0.5		℃
		Accuracy	-5		5	℃
REGN LDO						
REGN	V_{REGN}	V_{VBUS} = 8V		5.1		V
REGN Current Limit	I_{REGN}	V_{VBUS} = 8V, V_{REGN} = 4.5V	50			mA
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SHUT}	Rising threshold		150		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}	Hysteresis		30		℃
I²C Interface						
SCL Clock Frequency	f_{SCL}				1000	kHz
Input Logic High	V_{IH}	SCL and SDA pins	0.825			V
Input Logic Low	V_{IL}	SCL or SDA is pulled up to 1.2V			0.4	V
Input Leakage Current	$I_{LEAKAGE}$	For SCL or SDA			1	μA
Interrupt						
Lasting Time during INT is Low	t_{INT_LOW}			256		μs
Minimum High Level Time after an INT Low Event	t_{INT_HIGH}			256		μs
Output Logic Low	V_{OL}	I_{OL} = 1mA, V_{PULL_UP} = 1.8V		0.4		V
Output Logic High Leakage Current	I_{OL}	Pull up to 1.8V			1	μA
Watchdog Timeout	$t_{WD\_TIMEOUT}$	Range	0.5	40	160	s
ACDRV Turn-on Deglitch Time	$t_{ACDRV\_ON\_DGL}$	Deglitch time between VAC over VAC present rising edge and turn on the external MOSFET, ACDRV_ON_DEG = 0 (20ms)		20		ms
VBUS Pull-Down Time before turn-on ACDRV	t_{VBUS_PD}			15.5		ms
VAC OVP Reaction Time	t_{VAC_OVP}			150		ns
VAC Pull-Down Time	t_{VAC_PD}			380		ms
VBUS OVP Reaction Time	t_{BUS_OVP}			1		μs
Resistances						
On-Resistance of Buck HSFET	R_{HSFET_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		22		mΩ
On-Resistance of Buck LSFET	R_{LSFET_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		26		mΩ
On-Resistance of BATFET	R_{BATFET_ON}	V_{BAT} = 4.2V		15		mΩ
Battery Depletion Threshold	V_{BAT_DPL}	Falling threshold		2.3		V
		Hysteresis		175		mV
Minimum VBUS-VBAT Voltage for Buck Sleep Mode	V_{SLEEP_BUCK}	Falling threshold	30	100	170	mV
		Hysteresis	90	150	220	mV
Bad Adaptor Detection Threshold	V_{VBUS_MIN}	Falling threshold		3.85		V
		Hysteresis		180		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bad Adaptor Detection Current from VBUS to GND	I_{BAD_SINK}			25		mA
Power Path Control						
Minimum System Voltage	V_{SYS_MIN}	Range	2.6		3.7	V
		Accuracy at 3.5V, V_{BAT} < V_{SYS_MIN}	-2		2	%
System Regulated Output Voltage	V_{SYS_REG}	VBUS present, during trickle and pre-charging, V_{BAT} < V_{SYS_MIN}		V_{SYS_MIN} + 0.25		V
		VBUS present, during fast charging, V_{BAT} ≥ V_{SYS_MIN}		V_{BAT} + I_{CHG} ×R_{BATFET_ON}		V
VBAT Tracking Voltage after End of Charging	V_{BAT_TRACK}	V_{SYS} = V_{BAT} + V_{BAT_TRACK}		60		mV
		Accuracy	-40		40	mV
BATFET Forward Voltage in Supplement Mode	V_{FWD}			20		mV
VBAT-VSYS Threshold Voltage to Trigger Supplement Mode	$V_{SUPPLEMENT}$	V_{BAT} ≥ V_{SYS_MIN}		160		mV
		V_{BAT} < V_{SYS_MIN}		50		mV
Supplement Mode Reaction Time	$t_{SUPPLEMENT}$			40		μs
BATFET Turn-on Deglitch Time when V_{BAT} > V_{BAT_DPL} Rising Threshold	$t_{BATFET\_ON\_DGL}$			125		ms
BATFET Soft Turn-on Time	$t_{BATFET\_ON\_SS}$			1		ms
Charger Management						
Charge Voltage Program Range	V_{BAT_REG}	Range	3.84		4.856	V
Charge Voltage Step		Step		8		mV
Charge Voltage Accuracy	$V_{BAT\_REG\_ACC}$	VBAT_REG[6:0] = 0101110 (4.208V)	-0.5		0.5	%
		VBAT_REG[6:0] = 1001100 (4.448V)	-0.5		0.5	%
		VBAT_REG[6:0] = 1010010 (4.496V)	-0.5		0.5	%
Constant Charging Current Range	I_{CC_RANGE}	I_{CC} range	0		4	A
Constant Charging Current Step	I_{CC_STEP}	I_{CC} step		50		mA
Constant Charging Current Accuracy, T_J = 0℃ to +55℃	I_{CC_ACC}	I_{CC} = 4A, ICHG_CC[6:0] = 1010000	-5		5	%
		I_{CC} = 2A, ICHG_CC[6:0] = 0101000	-5		5	%
		I_{CC} = 1A, ICHG_CC[6:0] = 0010100	-7		7	%
		I_{CC} = 200mA, ICHG_CC[6:0] = 0000100	-25		25	%
Trickle Charge Current	I_{TRICK}	V_{BAT} < V_{TRICK}		90		mA
Trickle Charge to Pre-charge Threshold	V_{TRICK}	Rising threshold	2	2.1	2.2	V
Trickle Charge to Pre-charge Threshold Hysteresis	V_{TRICK_HYS}			220		mV
Deglitch Time for Entering and Exiting Trick Charge	t_{TRICK_DGL}	Rising threshold		36		ms
Pre-Charge to Fast Charge Voltage Threshold	V_{PRE_CHG}	3V (VBAT_PRECHG = 1), rising threshold	2.9	3	3.1	V
		2.7V (VBAT_PRECHG = 0), rising threshold option	2.6	2.7	2.8	V
		Hysteresis		220		mV
Pre-Charge Current	I_{PRE_CHG}	Step		50		mA
		Range	50		800	mA
		I_{PRE_CHG} setting = 150mA (Initialization), T_J = +25℃	-25		25	%
		I_{PRE_CHG} setting = 400mA (Initialization), T_J = +25℃	-10		10	%
		I_{PRE_CHG} setting = 800mA (Initialization), T_J = +25℃	-7		7	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Termination Current	I_{TERM}	Step		50		mA
		Range	100		1650	mA
		I_{TERM} setting = 100mA – 200mA	-25		25	%
		I_{TERM} setting = 200mA – 400mA	-15		15	%
		I_{TERM} setting = 400mA – 800mA	-10		10	%
		I_{TERM} setting = 800mA – 1650mA	-7		7	%
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	VBAT falling threshold, 100mV (VRECHG[1:0] = 00)		100		mV
		VBAT falling threshold, 200mV (VRECHG[1:0] = 01)		200		mV
System Discharge Load when VSYS OVP is Triggered	$I_{SYSLOAD}$	V_{SYS} = 4.2V		25		mA
Deglitch Time for Charge Termination Range	t_{TERM_DGL}	Range, programmable by TERM_DEG, 256ms by default	48		256	ms
Deglitch Time for Recharge Range	t_{RECH_DGL}	Range, programmable by RECHG_DG[1:0], 1024ms by default	64		2048	ms
System Over-Current Deglitch Time to turn off BATFET	t_{BATOCP_DGL}	IBATOCP[1:0] = 01 (12A)		112		μs
System Over-Voltage Deglitch Time to Turn off DC/DC Converter	t_{SYSOVP_DGL}			1		μs
Battery Over-Voltage Deglitch Time to Turn off DC/DC Converter	t_{BATOVP_DGL}			1		μs
Input Voltage and Current Regulation						
Input Voltage Regulation Limit	V_{INDPM}	Range	4		10.7	V
		Minimum step		100		mV
Input Voltage Regulation Limit Tracking VBAT	V_{INDPM_VBAT}	V_{BAT} = 4V, VINDPM_VBAT[1:0] = 10 (250mV)		4.25		V
VBUS Input Current Regulation Limit	I_{INDPM}	Range	100		3250	mA
		Step		50		mA
		IINDPM[5:0] = 001000, 500mA	430	470	510	mA
		IINDPM[5:0] = 010000, 900mA	810	855	900	mA
		IINDPM[5:0] = 011100, 1500mA	1350	1425	1500	mA
		IINDPM[5:0] = 111111, 3250mA	2900	3075	3250	mA
Input Current Limit during System Start-up Sequence	I_{IN_START}			160		mA
Boost Mode Operation						
Boost Mode Regulation Voltage	V_{OTG_REG}	Range	3.9	4.9	5.8	V
		Step		100		mV
		Accuracy, no load at PMID_BUCK, V_{PMID_BUCK} = 4.9V	-3		3	%
Battery Voltage Exiting Boost Mode	$V_{BAT\_LOW\_OTG}$		2.7	2.8	2.9	V
		Hysteresis		230		mV
OTG Mode Output Current Limit when RBFET Q1 is Turned on	I_{OTG_LMT}	Range	0.5		3.25	A
		I_{OTG_LMT} setting = 0.5A (IBOOST_LIM[2:0] = 000)	0.475		0.72	A
		I_{OTG_LMT} setting = 1.5A (IBOOST_LIM[2:0] = 011)	1.5			A
		I_{OTG_LMT} setting = 3.25A (IBOOST_LIM[2:0] = 111)	3.25			A
Boost Over-Voltage Threshold on PMID Voltage Sense	V_{PMID_OVP}	Rising threshold	6.05	6.2	6.35	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JEITA (Buck Mode Only)							
NTC Cold Temp (0℃) Threshold Voltage on TSBAT Pin	V_{COLD}	Rising threshold, charge suspended above this voltage	with 103AT, as percentage of V_{REGN}	72.4	73.3	74.2	%
		Falling threshold, charge at cool temperature starts below this voltage		71.2	71.85	72.5	%
NTC Cool Temp Threshold Voltage on TSBAT Pin	V_{COOL}	5℃ rising threshold		70.25	70.75	71.25	%
		5℃ falling threshold		68.4	69	69.6	%
		10℃ rising threshold		67.75	68.25	68.75	%
		10℃ falling threshold		66.15	66.75	67.35	%
		15℃ rising threshold		64.75	65.25	65.75	%
		15℃ falling threshold		63.4	64	64.6	%
		20℃ rising threshold		61.75	62.25	62.75	%
		20℃ falling threshold		60.4	61	61.6	%
NTC Warm Temp Threshold Voltage on TSBAT Pin	V_{WARM}	40℃ rising threshold	with 103AT, as percentage of V_{REGN}	48.8	49.3	49.8	%
		40℃ falling threshold		47.65	48.15	48.65	%
		45℃ rising threshold		45.3	45.8	46.3	%
		45℃ falling threshold		44.1	44.6	45.1	%
		50℃ rising threshold		41.3	41.8	42.3	%
		50℃ falling threshold		40.1	40.6	41.1	%
		55℃ rising threshold		38.5	39	39.5	%
		55℃ falling threshold		37.1	37.6	38.1	%
NTC Hot Temp (60℃) Threshold Voltage on TSBAT Pin	V_{HOT}	Rising threshold, charge at warm temperature starts above this voltage	with 103AT, as percentage of V_{REGN}	34.8	35.3	35.8	%
		Falling threshold, charge suspended below this voltage		33.6	34.1	34.6	%
ICC Ration during JEITA Cool	I_{RATIO_COOL}	JEITA_ISET_COOL[1:0] = 00	As percentage of I_{CHG}		0		%
		JEITA_ISET_COOL[1:0] = 01			20		%
		JEITA_ISET_COOL[1:0] = 10			50		%
		JEITA_ISET_COOL[1:0] = 11			100		%
ICC Ration during JEITA Warm	I_{RATIO_WARM}	JEITA_ISET_WARM[1:0] = 00	As percentage of I_{CHG}		0		%
		JEITA_ISET_WARM[1:0] = 01			20		%
		JEITA_ISET_WARM[1:0] = 10			50		%
		JEITA_ISET_WARM[1:0] = 11			100		%
VBAT Regulation Voltage during JEITA Warm	V_{DELTA_WARM}	JEITA_VSET_WARM[1:0] = 00	Less than V_{BAT_REG}		0		mV
		JEITA_VSET_WARM[1:0] = 01			50		mV
		JEITA_VSET_WARM[1:0] = 10			100		mV
		JEITA_VSET_WARM[1:0] = 11			200		mV
NTC (Boost Mode)							
NTC Cold Temp Threshold	V_{BCOLD}	Rising threshold, as percentage of V_{REGN} (approx. -20℃ w/ 103AT)		79.3	80	80.7	%
		Falling threshold, as percentage of V_{REGN}		78.4	78.9	79.4	%
NTC Hot Temp Threshold	V_{BHOT}	Rising threshold, as percentage of V_{REGN}		33.9	34.4	35.1	%
		Falling threshold, as percentage of V_{REGN} (approx. 60℃ w/ 103AT)		30.6	31.1	31.6	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Protection						
Battery Discharge Over-Current Threshold	I_{BAT_OCP}	Range, programmable by IBATOCP[1:0]	10	12	16	A
Battery Over-Voltage Protection	$V_{BAT\_OVP\_BUCK}$	Falling threshold, as percentage of V_{BAT}	101	102	103	%
		Hysteresis		2		%
System Over-Voltage Protection	V_{SYS_OVP}	Rising threshold range , as percentage of V_{SYS_REG}	104		110	%
		Step		2		%
		Hysteresis		2		%
		Comparator accuracy	-2		2	%
System Short Threshold	V_{SYS_SHORT}	Falling threshold	2.1	2.25	2.4	V
		Hysteresis		160		mV
Thermal Regulation						
Thermal Regulation Temperature	T_{REG}	Range, programmable by TDIE_REG[1:0]	60		120	℃
		Step		20		℃
Timers						
PWM Switching Frequency in Buck Mode	f_{SW_BUCK}	Buck mode, 1500kHz (BUCK_FREQ[1:0] = 10)	1320	1500	1680	kHz
		Buck mode, 1000kHz (BUCK_FREQ[1:0] = 01)	880	1000	1120	kHz
PWM Switching Frequency in Boost Mode	f_{SW_BOOST}	Boost mode, 1500kHz (BOOST_FREQ[1:0] = 10)	1320	1500	1680	kHz
		Boost mode, 500kHz (BOOST_FREQ[1:0] = 00)	440	500	560	kHz
Maximum Duty Cycle in Buck Mode	D_{MAX_BUCK}			99		%
Bad Adaptor Detection Duration	t_{BADSRC}			28		ms
Safety Timer for Trickle Charge	$t_{TRICKLE\_TIMER}$			4.25		hours
Safety Timer for CC & CV Stage	t_{CCCV_TIMER}	Range, programmable by CHG_TIMER[1:0]	5	13	25	hours
Charge Pump						
Q_{RBFET} On-Resistance	R_{QB_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		10		mΩ
Q_{CH} On-Resistance	R_{QCH1_ON} R_{QCH2_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		15		mΩ
Q_{DH} On-Resistance	R_{QDH1_ON} R_{QDH2_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		10		mΩ
Q_{CL} On-Resistance	R_{QCL1_ON} R_{QCL2_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		10		mΩ
Q_{DL} On-Resistance	R_{QDL1_ON} R_{QDL2_ON}	V_{VBUS} = 9V, V_{BAT} = 4.5V		9		mΩ
Internal Threshold						
Minimum VBAT Voltage for CP Charging Enable	$V_{BAT\_MIN\_CP}$	Rising threshold		2.9	3.05	V
		Hysteresis		200		mV
Minimum VBUS-VBAT Voltage for Charge Pump	V_{SLEEP_CP}		-0.085	-0.07	-0.055	V_{BAT}

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS In–Range Protection for Charge Pump						
BUS over BAT High Threshold	$V_{VBUS2BAT\_HI}$	Rising threshold, VBUS/2-VBAT in 2:1 divider mode or VBUS-VBAT in bypass mode		0.2		V_{BAT}
		Falling threshold, VBUS/2-VBAT in 2:1 divider mode or VBUS-VBAT in bypass mode		0.17		V_{BAT}
BUS over BAT Low Threshold	$V_{VBUS2BAT\_LO}$	Rising threshold, VBUS/2-VBAT in 2:1 divider mode or VBUS-VBAT in bypass mode		0.02		V_{BAT}
		Falling threshold, VBUS/2-VBAT in 2:1 divider mode or VBUS-VBAT in bypass mode		0		V_{BAT}
Input/Output Short Protection for Charge Pump						
PMID_CP to BAT OVP	$V_{PMID2BAT\_OVP}$	Range, equal to V_{PMID_CP}/2 - V_{BAT} (2:1 divider mode) or V_{PMID_CP} - V_{BAT} (bypass mode)	250	400	600	mV
		Step		50		mV
PMID_CP to BAT UVP	$V_{PMID2BAT\_UVP}$	Range, equal to V_{PMID_CP}/2 - V_{BAT} (2:1 divider mode) or V_{PMID_CP} - V_{BAT} (bypass mode)	-225	-100	-50	mV
		Step		25		mV
Output Over-voltage Protection						
BAT Over-voltage Protection	$V_{BAT\_OVP\_CP}$	Rising threshold, CP mode	4.9	5	5.1	V
BAT Sense (BATP-BATN) Over-Voltage Protection	$V_{BATSNS\_OVP\_CP}$	Rising threshold, Range	3.5		5.075	V
		Step		25		mV
		Comparator accuracy, V_{BATSNS_OVP} setting = 4.5V (Initialization), T_J = +25℃	-0.5		0.5	%
Input Over-current Protection						
BUS Over-Current Protection Threshold	I_{BUS_OCP}	Rising threshold, range	1		6.5	A
		Step		250		mA
		Comparator accuracy, I_{BUS} = 3A	-5		5	%
BUS Under-Current Protection Threshold	I_{BUS_UCP}	Rising threshold		300	400	mA
		Falling threshold	10	150		mA
Timers for Charge Pump						
Charge Pump Switching Frequency	f_{PWM_CP}	Range	460	700	1000	kHz
Minimum VBUS In-range Duration before Charge Pump Start Switching	$t_{VBUS\_IN\_RANGE}$	VBUS over VBAT high or low threshold		5		ms
BUS Over-Current Reaction Time	t_{IBUS_OCP}			75		μs
BUS Under-Current Falling Deglitch Time	$t_{IBUS\_UCP\_F\_DGL}$	IBUS_UCP_FALL_DG_SET[1:0] = 00 (250μs)		250		μs
		IBUS_UCP_FALL_DG_SET[1:0] = 01 (5ms)		5		ms
		IBUS_UCP_FALL_DG_SET[1:0] = 10 (40ms)		40		ms
		IBUS_UCP_FALL_DG_SET[1:0] = 11 (160ms)		160		ms
PMID_CP to BAT OVP Reaction Time	$t_{PMID2BAT\_OVP}$			0.1		μs
PMID_CP to BAT UVP Reaction Time	$t_{PMID2BAT\_UVP}$			0.1		μs
BAT Over-Voltage Reaction Time	t_{BAT_OVP}			1		μs
BATSNS Over-Voltage Reaction Time	t_{BATSNS_OVP}			0.1		μs
Soft-Start Timeout	$t_{SS\_TIMEOUT}$	Range	0		10	s

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Drivers						
Output Current Accuracy	I_D	LED1/2 = 1500mA, flash mode, T_J = +25℃	1395	1500	1605	mA
		LED1/2 = 500mA, torch mode, T_J = +25℃	460	500	540	mA
Flash LED Timeout Time	$t_{TIMEOUT}$	Range	50		1200	ms
Headroom to Guarantee Accuracy (TORCH_VDD - LED1/2 or FLASH_VDD - LED1/2)	$V_{HEADROOM}$	$I_{LED1/2}$ = 1.5A in flash mode, I_{FLASH} drops to 1.4A		250		mV
		$I_{LED1/2}$ = 500mA in torch mode, I_{TORCH} drops to 430mA		80		mV
FLASH_VDD OVP	$V_{FLASH\_VDD\_OVP}$	Rising threshold		5.5		V
		Falling threshold		5.25		V
TORCH_VDD OVP	$V_{TORCH\_VDD\_OVP}$	Rising threshold		5.45		V
		Hysteresis		230		mV
TORCH_VDD UVP	$V_{TORCH\_VDD\_UVP}$	Falling threshold (Torch function is disabled when TORCH_VDD is below the threshold.)		2		V
		Hysteresis		120		mV
Minimum VBAT Voltage to Enable FLASH LED	$V_{MINVBAT\_EN\_FLASH}$	Rising threshold		3.6		V
		Falling threshold	3	3.2	3.4	V
PD PHY						
Bit Rate	$f_{BitRate}$		270	300	330	kbps
Maximum Difference between the Bit-rate during the Part of the Packet Following the Preamble and the Reference Bit-rate	$p_{BitRate}$				0.25	%
Time from the End of Last Bit of a Frame until the Start of the First Bit of the Next Preamble	$t_{InterFrameGap}$		25			μs
Time before the Start of the First Bit of the Preamble when the Transmitter Shall Start Driving the Line	$t_{StartDrive}$		-1		1	μs
Time to Cease Driving the Line after the End of the Last Bit of the Frame	$t_{EndDriveBMC}$				23	μs
Fall Time	t_{Fall}		300			ns
Time to Cease Driving the Line after the Final High-to-Low Transition	$t_{HoldLowBMC}$		1			μs
Rise Time	t_{Rise}		300			ns
Voltage Swing	V_{Swing}		1.05	1.125	1.2	V
Time Window for Detecting Non-Idle	$t_{TransitionWindow}$		12		20	μs
Receiver Input Impedance	R_{BmcRX}		1			MΩ
VSAFE0V Comparator Rising Threshold	$V_{SAFE0V\_TH\_R}$			0.85	0.9	V
VSAFE0V Comparator Falling Threshold	$V_{SAFE0V\_TH\_F}$		0.7	0.75	0.8	V
VSAFE0V Comparator Deglitch Time	t_{SAFE0V_DGL}			112		μs
VCONN Present Voltage Threshold	$V_{CONN\_PRESENT}$	Rising threshold		2.6		V
		Falling threshold		2.2		V
VBUS Present Deglitch Time	$t_{SAFE5V\_PRESENT\_DGL}$			5.5		ms

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC1/2 Pull-Up Current	$I_{CC\_80\mu A}$	V_{DD} = 3.3V, RP_VALUE[1:0] = 00	64	80	96	μA
	$I_{CC\_180\mu A}$	V_{DD} = 3.3V, RP_VALUE[1:0] = 01	150	180	210	μA
	$I_{CC\_330\mu A}$	V_{DD} = 3.3V, RP_VALUE[1:0] = 10	275	330	385	μA
CC1/2 Open Impedance	R_{CC_OPEN}	CC1/2 is in disabled status	126			kΩ
Voltage on both CC Pins when in Dead Battery and the Attached DFP is Presenting Default Current Advertisement	$I_{CC\_80\mu A\_DB}$	V_{DD} = 0V	0.25		1.5	V
Voltage on both CC Pins when in Dead Battery and the Attached DFP is Presenting 1.5A Current Advertisement	$I_{CC\_180\mu A\_DB}$	V_{DD} = 0V	0.45		1.5	V
Voltage on both CC Pins when in Dead Battery and the Attached DFP is Presenting 3A Current Advertisement	$I_{CC\_330\mu A\_DB}$	V_{DD} = 0V	0.88		2.18	V
Pull-Down Resistor when in UFP or DRP Mode	R_D	V_{DD} = 2.9V to 5.5V	4.85	5.1	5.45	kΩ
CC1/2 0.2V Comparison Threshold	$V_{CC\_0P2\_TH\_SRC}$	CC1/2 as sources	0.15	0.2	0.25	V
CC1/2 0.4V Comparison Threshold	$V_{CC\_0P4\_TH\_SRC}$		0.35	0.4	0.45	V
CC1/2 0.66V Comparison Threshold	$V_{CC\_0P66\_TH\_SRC}$		0.61	0.66	0.71	V
CC1/2 0.8V Comparison Threshold	$V_{CC\_0P8\_TH\_SRC}$		0.75	0.8	0.85	V
CC1/2 1.23V Comparison Threshold	$V_{CC\_1P23\_TH\_SRC}$		1.16	1.23	1.3	V
CC1/2 1.6V Comparison Threshold	$V_{CC\_1P6\_TH\_SRC}$		1.45	1.6	1.67	V
CC1/2 2.6V Comparison Threshold	$V_{CC\_2P6\_TH\_SRC}$		2.45	2.6	2.75	V
OVP Threshold at CC1/CC2 Pin	$V_{CC1/2\_OVP}$	Rising threshold	7	7.25	7.5	V
	$V_{CC1/2\_OVP\_HYS}$	Falling hysteresis		200		mV
CC OVP Deglitch Time	$t_{CC\_OVP\_DGL}$			5		μs
VCONN Switch On-Resistance	R_{VCONN}	V_{DD} = 3V, V_{CONN} = 3V		1.2		Ω
VCONN Current Capability	I_{VCONN}	Range, V_{CONN} = 3.7V	200		600	mA
VCONN OCP Rising Threshold for 200mA	$I_{VCONN\_OCP\_R}$	V_{CONN} = 5V		200		mA
VCONN OCP Rising Threshold for 300mA				300		mA
VCONN OCP Rising Threshold for 400mA				400		mA
VCONN OCP Rising Threshold for 500mA				500		mA
VCONN OCP Rising Threshold for 600mA				600		mA
VCONN OCP Deglitch Time	$t_{VCONN\_OCP\_DGL}$			8		μs
VCONN Soft Turn-on Time	t_{VCONN_SOFT}			400		μs
VCONN Discharge Resistor	R_{VCONN_DCHG}		2.4	4	5.6	kΩ
DP/DM						
DP/DM Source Voltage	V_{DP/DM_SRC}	DP/DM_DRIVE[2:0] = 010, V_{VAC} = 3.6V, 1mA source	0.5	0.6	0.7	V
		DP/DM_DRIVE[2:0] = 011, V_{VAC} = 3.6V, 1mA source	1.8	2	2.2	
		DP/DM_DRIVE[2:0] = 100, V_{VAC} = 3.6V, 1mA source	2.45	2.7	2.95	
		DP/DM_DRIVE[2:0] = 101, V_{VAC} = 3.6V, 1mA source	2.9	3.3	3.6	

ELECTRICAL CHARACTERISTICS (continued)

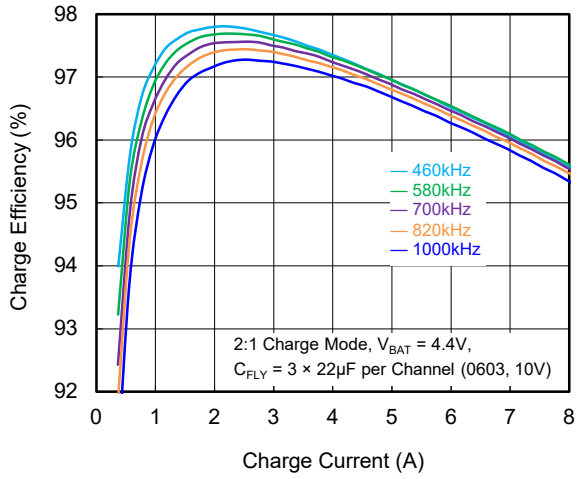
(V_{VBUS_UVLO} < V_{VBUS} < V_{VBUS_OVP}, V_{VAC_UVLO} < V_{VAC} < V_{VAC_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DP/DM Source Current Capability	I_{DP/DM_SRC}	BC1.2_DP/DM source capability	250			μA
DP/DM Sink Current Capability	I_{DP/DM_SINK}	BC1.2_DP/DM_SINK = 0	50	100	150	μA
		BC1.2_DP/DM_SINK = 1	25	50	75	μA
10μA Source Current on DP	$I_{DP\_SRC\_10μA}$		7	10	13	μA
Leakage Resistor on DP	R_{DP_LKG}	DP_DRIVE[2:0] = 000	300			kΩ
Pull-Down Resistor on DM	R_{DM_DWN}	DM_DRIVE[2:0] = 001	14.25	19.53	24.8	kΩ
Pull-Up Resistor to 3.3V Buffer	R_{DP/DM_PU}	DM_DRIVE[2:0] = 110		3		kΩ
0.325V Comparison Threshold on DP/DM	V_{TH_0P325}	BC1.2_VDAT_REF_SET = 1	0.24	0.275	0.31	V
		BC1.2_VDAT_REF_SET = 0	0.29	0.325	0.36	V
1V Comparison Threshold on DP/DM	V_{TH_1P0}			1		V
1.35V Comparison Threshold on DP/DM	V_{TH_1P35}			1.35		V
2.2V Comparison Threshold on DP/DM	V_{TH_2P2}			2.2		V
3V Comparison Threshold on DP/DM	V_{TH_3P0}			3		V
DP/DM OVP Threshold	V_{TH_OVP}			5.9		V
Miscellaneous						
CC_DIR	V_{OH}	20kΩ load	1.26			V
	V_{OL}	1mA sink			0.54	V
Input Voltage Low Level for RST0/RST1	V_{IL}				0.4	V
Input Voltage High Level for RST0/RST1	V_{IH}		1.35			V
Deglitch Time from Buck Charger Soft-Start Finished to nSYS_OK is Pulled Low	$t_{nSYS\_OK\_DGL}$	Range	50	150	300	ms
Reset Confirmation Time	t_{SYS_RST}	By pulling down RST0 & RST1		10		s
System Reset Time	t_{BATFET_RST}	T_BATFET_RST = 0		0.2		s
Shipping Mode Confirmation Time	t_{SM_DLY}	BATFET_DLY = 1		20		s
Exit Shipping Mode Time	$t_{SHIPMODE}$	By pulling down RST0		2		s
Deglitch Time of Exiting Shipping Mode by VAC Present Rising Threshold	$t_{VACRISE\_EXITSM\_DGL}$			5.6		ms

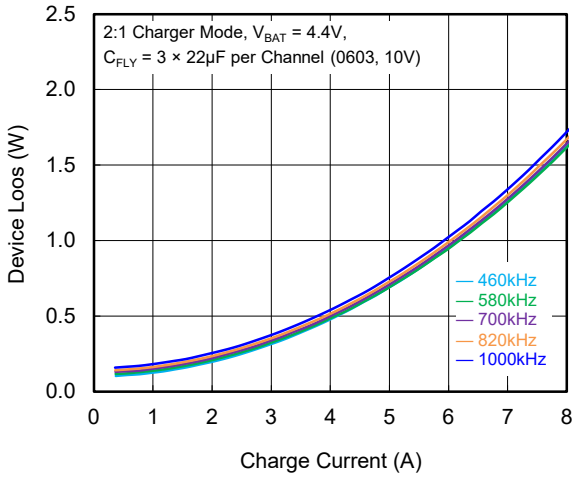
TYPICAL PERFORMANCE CHARACTERISTICS

Switched Cap Charger

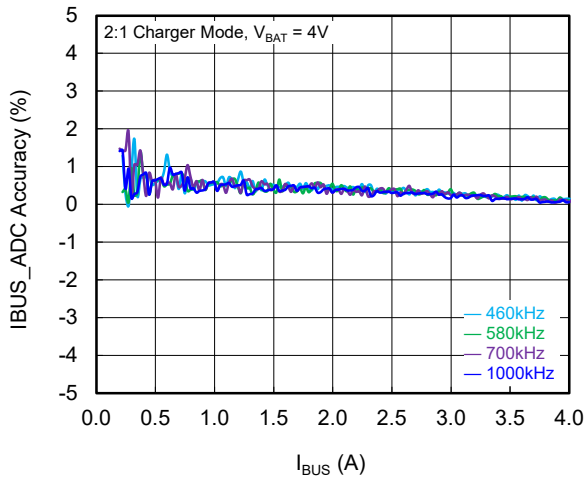
Charge Efficiency vs. Charge Current



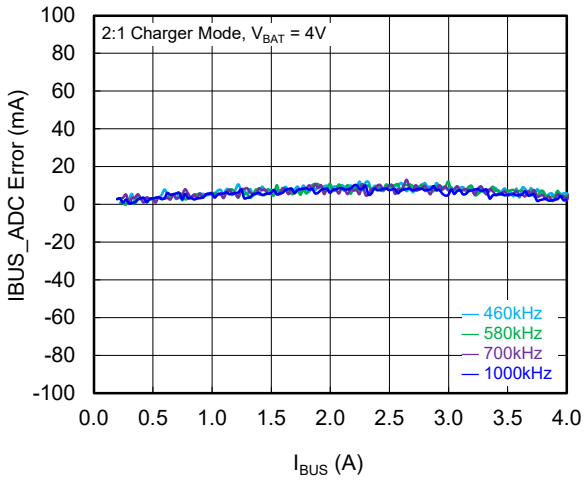
Device Loss vs. Charge Current



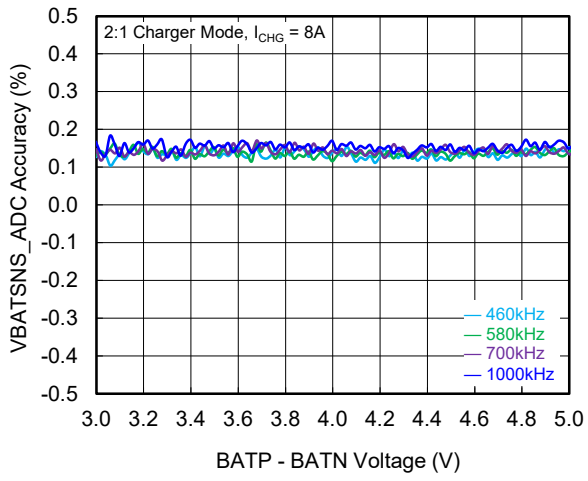
IBUS_ADC Accuracy vs. BUS Current



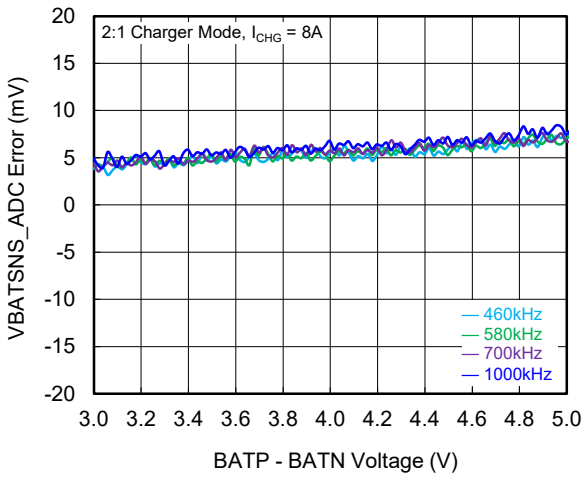
IBUS_ADC Error vs. BUS Current



VBATSNS_ADC Accuracy vs. BATP-BATN Voltage

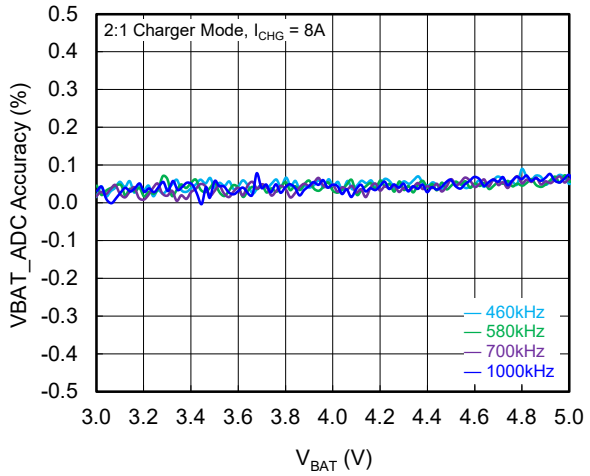


VBATSNS_ADC Error vs. BATP-BATN Voltage

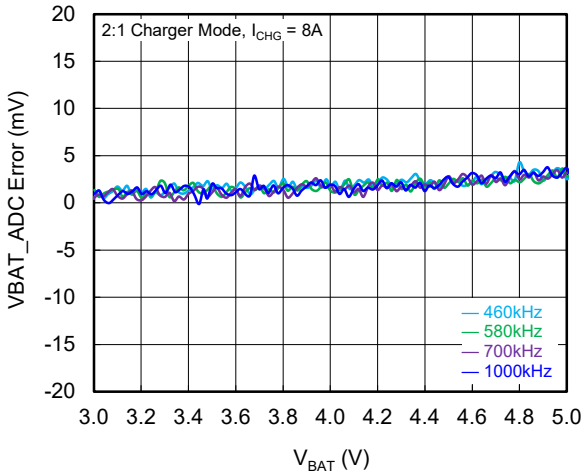


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

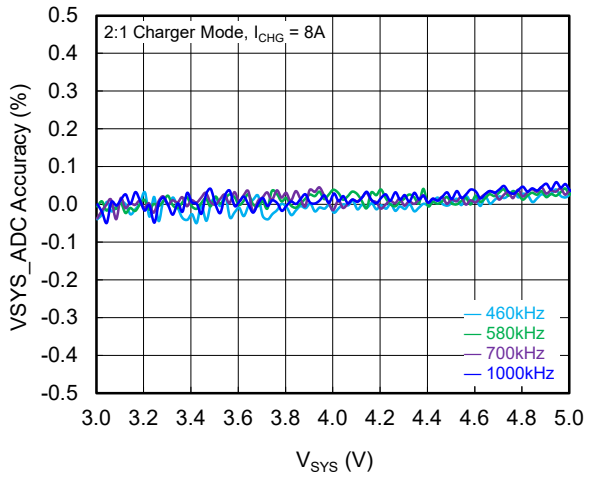
VBAT_ADC Accuracy vs. BAT Voltage



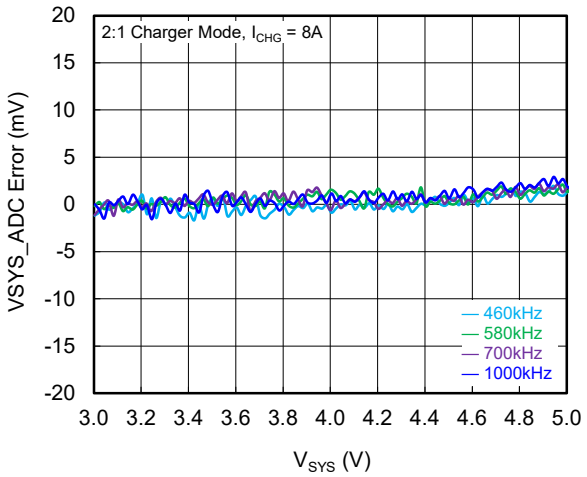
VBAT_ADC Error vs. BAT Voltage



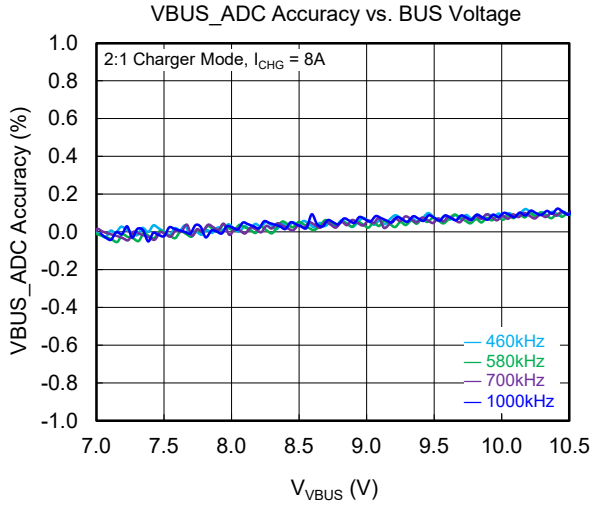
VSYS_ADC Accuracy vs. SYS Voltage



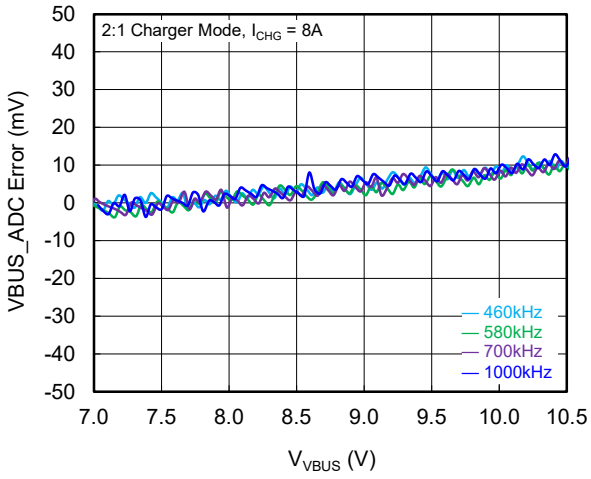
VSYS_ADC Error vs. SYS Voltage



VBUS_ADC Accuracy vs. BUS Voltage

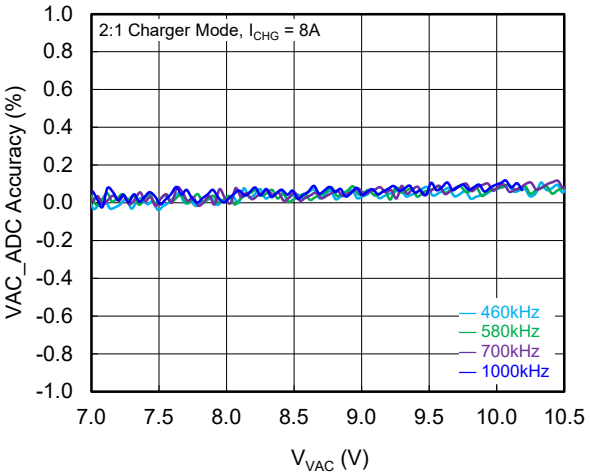


VBUS_ADC Error vs. BUS Voltage

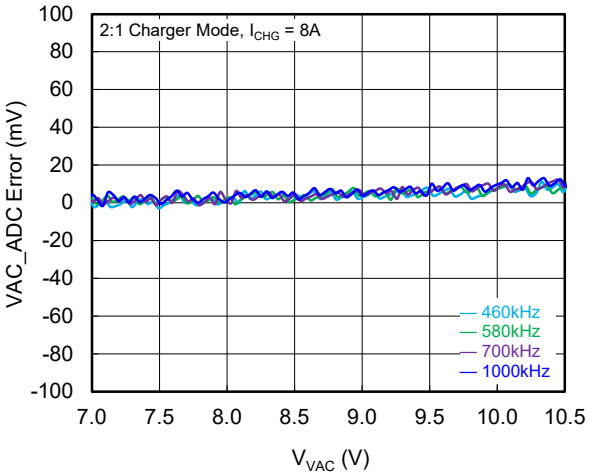


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

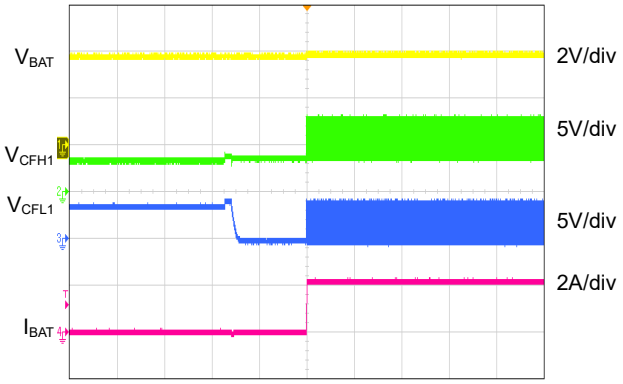
VAC_ADC Accuracy vs. VAC Voltage



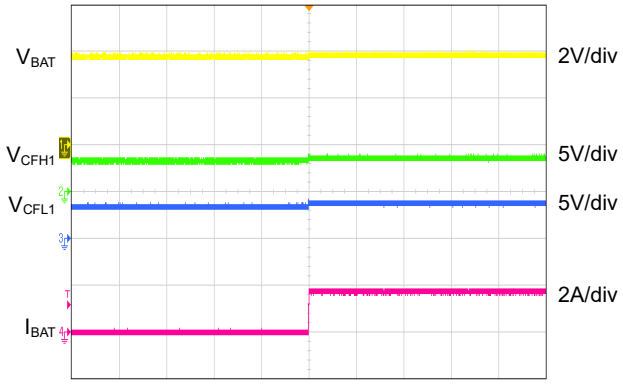
VAC_ADC Accuracy vs. VAC Voltage



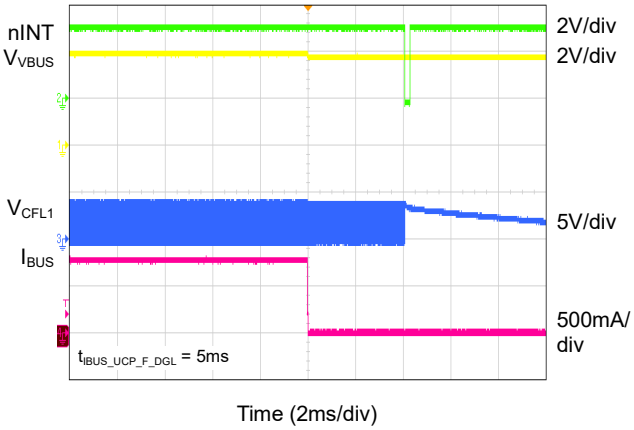
2:1 Charge Mode Power-Up



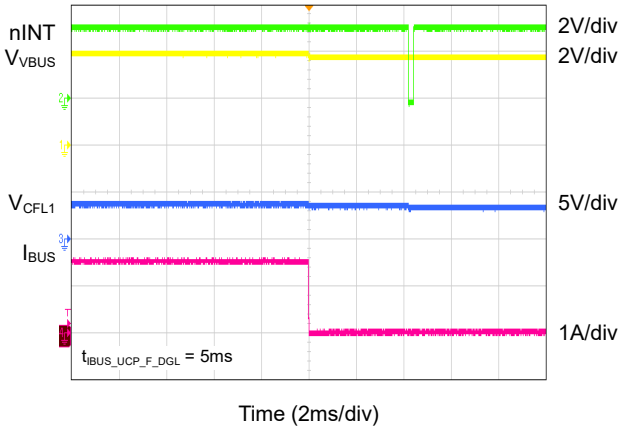
1:1 Charge Mode Power-Up



Adapter Unplug in 2:1 Charge Mode



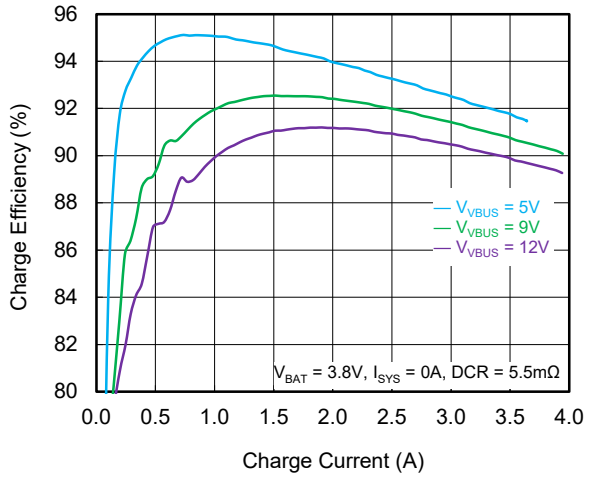
Adapter Unplug in 1:1 Charge Mode



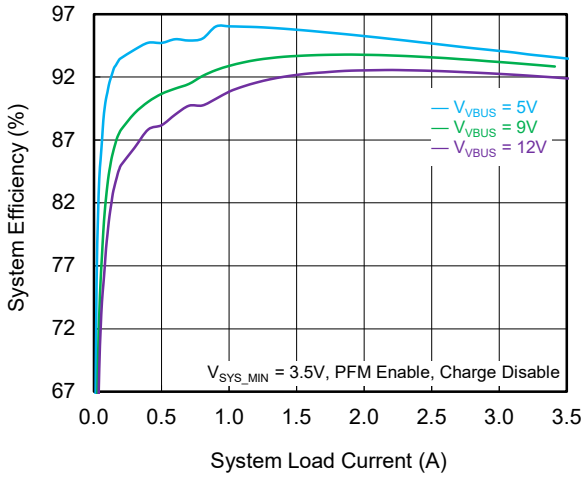
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Switched Mode Buck Charger

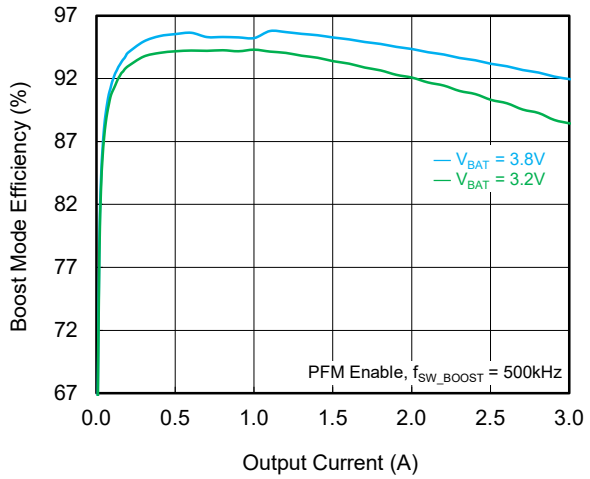
Charge Efficiency vs. Charge Current



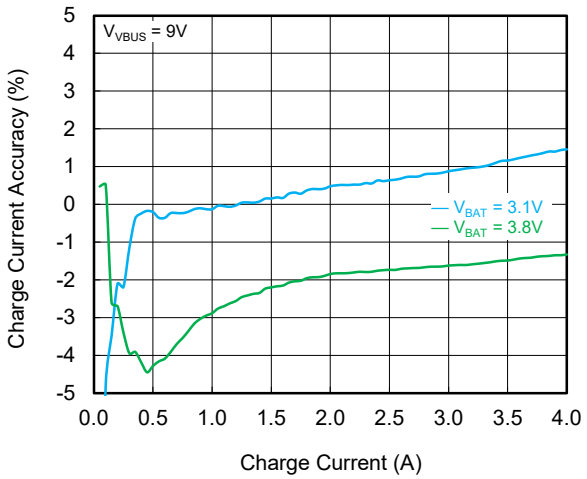
System Efficiency vs. System Load Current



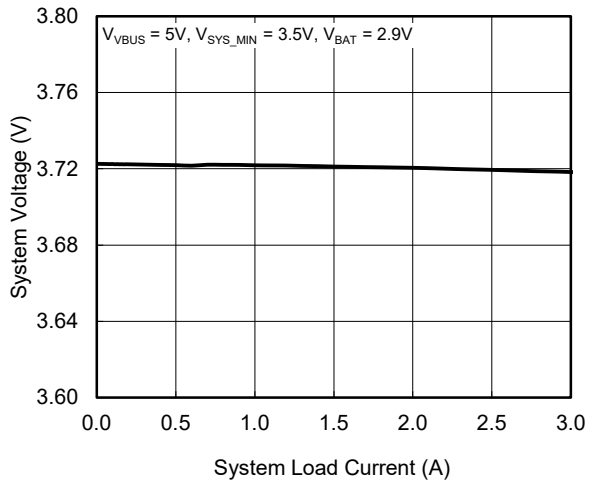
Boost Mode Efficiency vs. Output Current



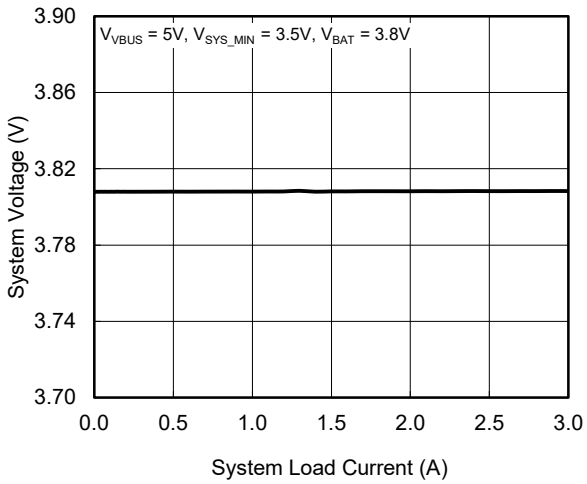
Charge Current Accuracy vs. Charge Current (I²C Setting)



System Voltage vs. System Load Current

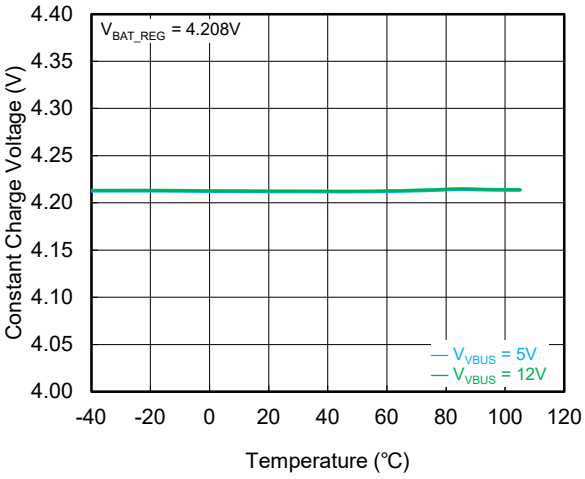


System Voltage vs. System Load Current

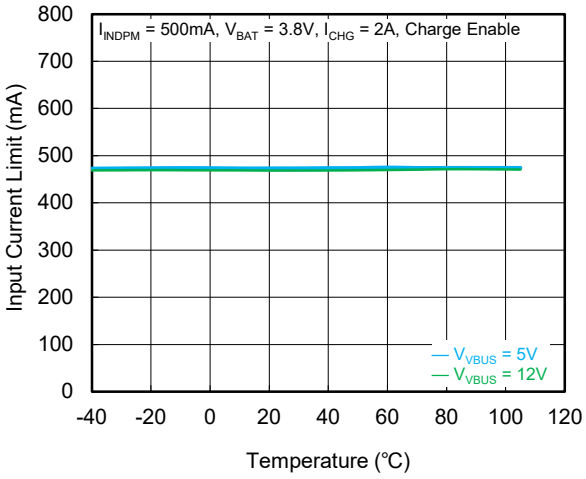


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

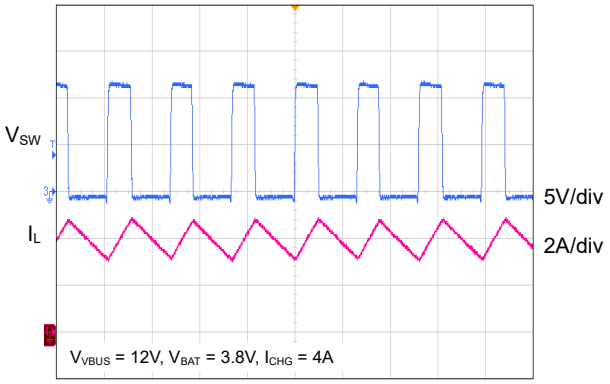
Constant Charge Voltage vs. Temperature



Input Current Limit vs. Temperature

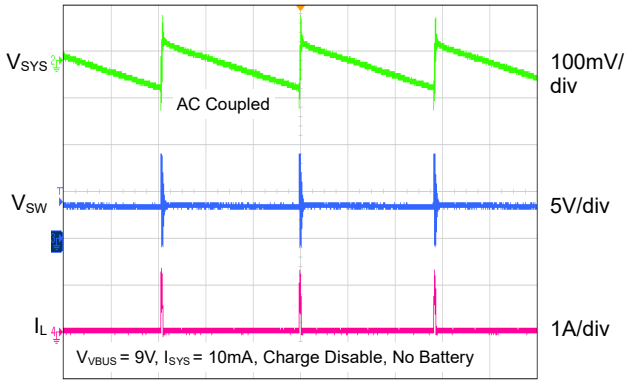


PWM Switching Waveform



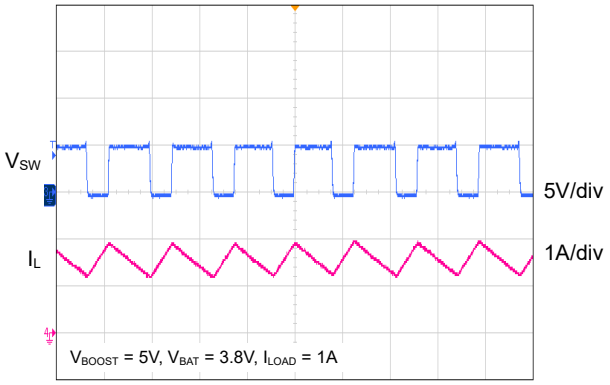
Time (500ns/div)

PFM Switching Waveform



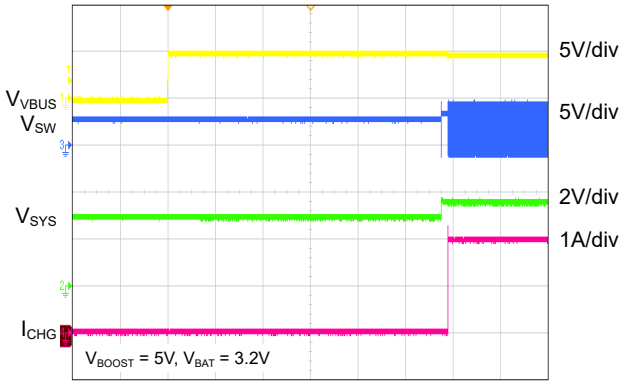
Time (20μs/div)

Boost Mode Switching Waveform



Time (500ns/div)

Power-Up with Charge Enable

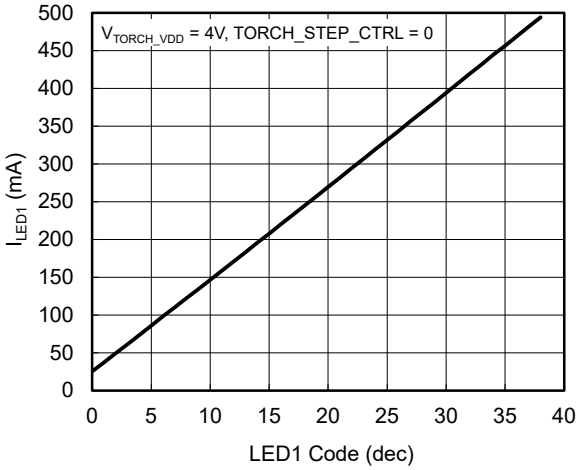


Time (100ms/div)

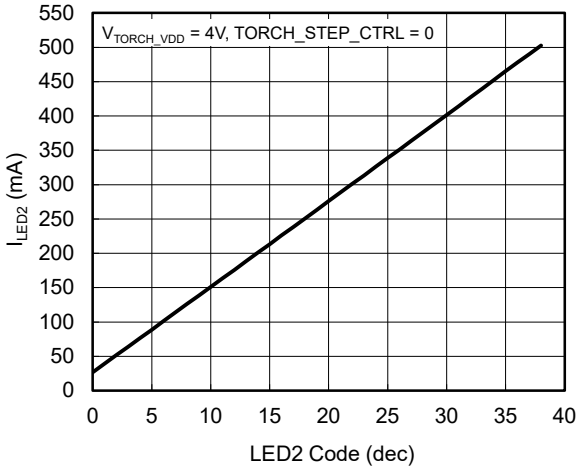
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Dual-Channel LED Driver

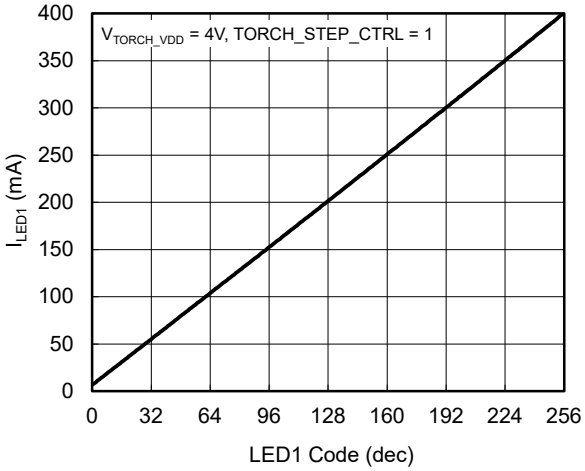
LED1 Torch Current vs. LED1 Torch Brightness Code



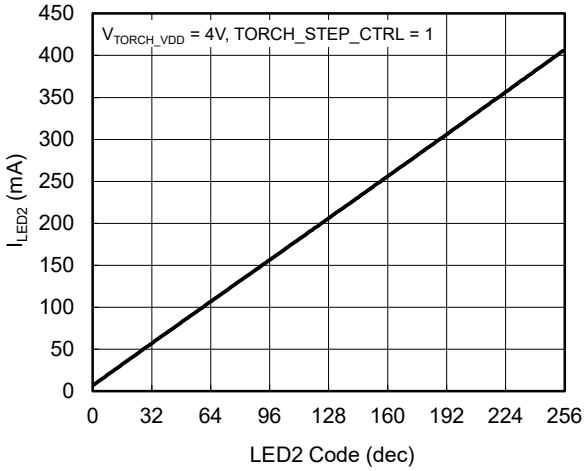
LED2 Torch Current vs. LED2 Torch Brightness Code



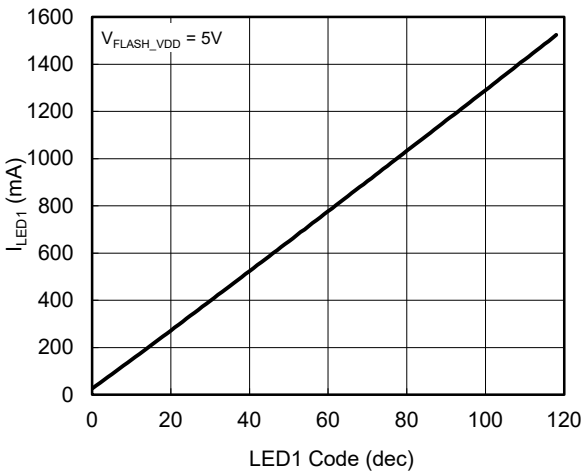
LED1 Torch Current vs. LED1 Torch Brightness Code



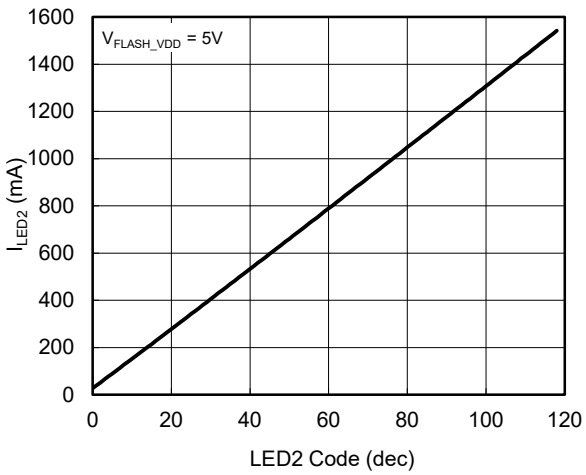
LED2 Torch Current vs. LED2 Torch Brightness Code



LED1 Flash Current vs. LED1 Flash Brightness Code

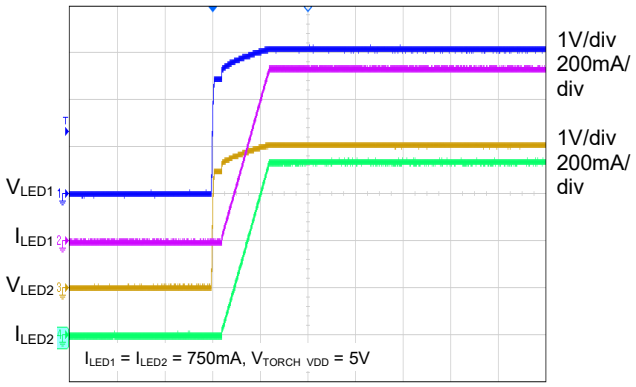


LED2 Flash Current vs. LED2 Flash Brightness Code



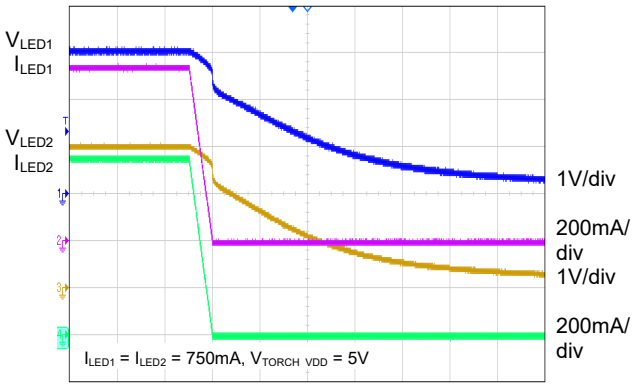
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Flash Mode Startup



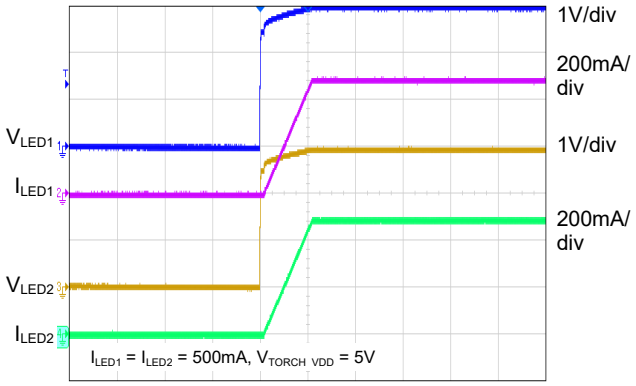
Time (500μs/div)

Flash Mode Ramp Down



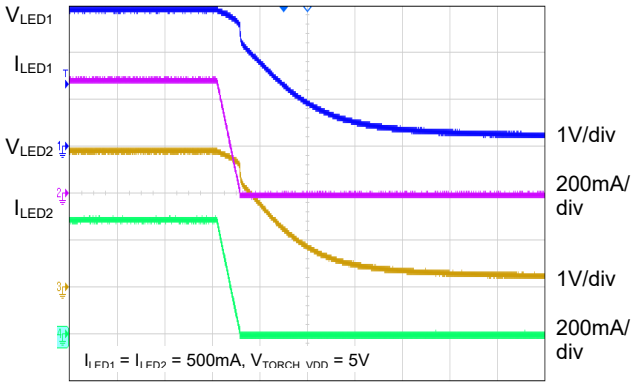
Time (1ms/div)

Torch Mode Startup



Time (1ms/div)

Torch Mode Ramp Down



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

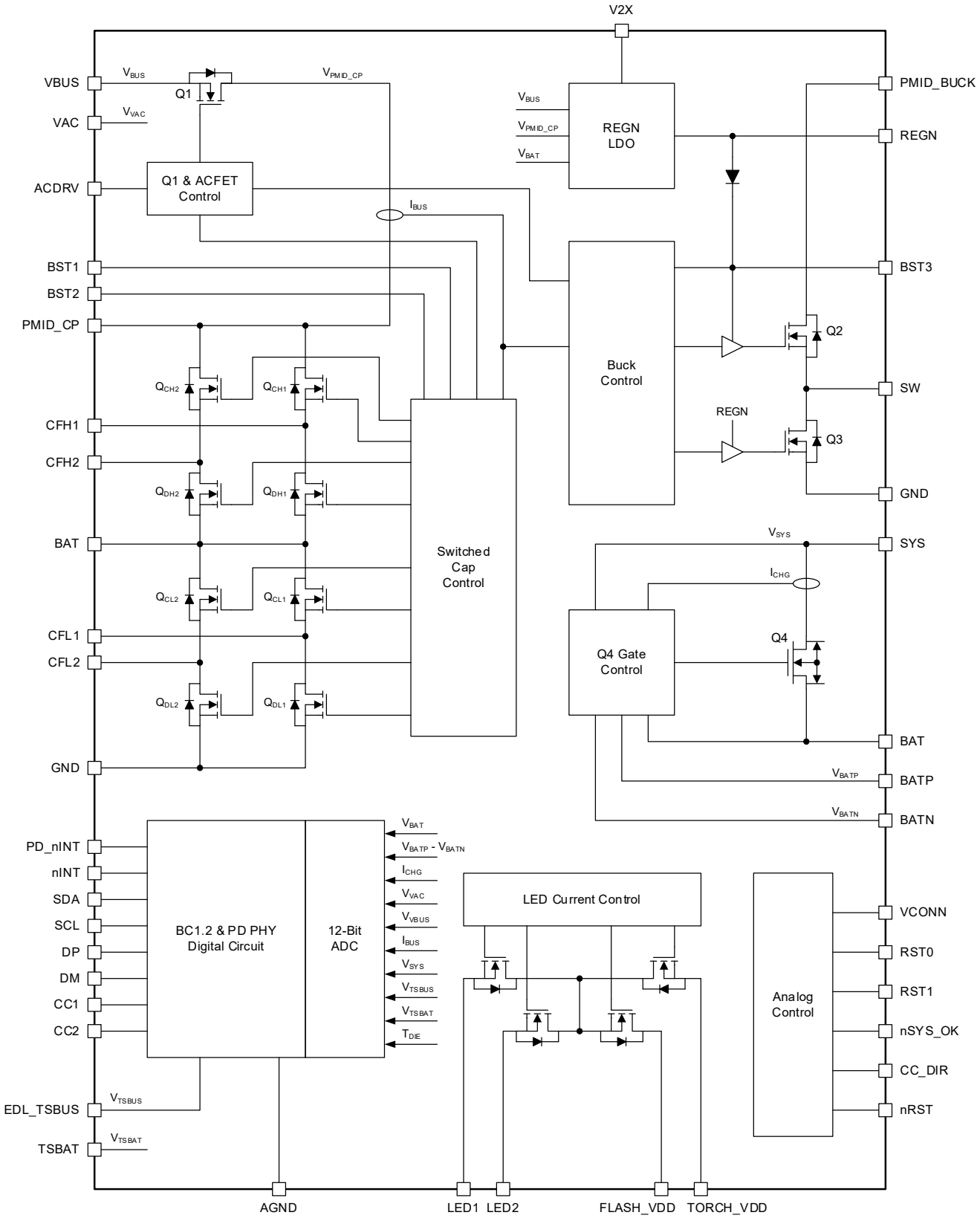


Figure 4. Functional Block Diagram

DETAILED DESCRIPTION

4A Switched Mode Buck Charger

The SGM41620 integrates a 4A switched mode Buck charger for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The Buck charger can accommodate a wide range of input sources including USB, wall adapter and car chargers. It is optimized for 5V input (USB voltage) but is capable of operating with input voltages from 3.9V to 13.5V. It also supports JEITA profile for battery charging safety at high or low temperatures. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT), or both, is another feature of the device. Battery charge current is programmable and can reach to a maximum of 4A. In the Boost mode, the battery voltage is boosted to power the VAC pin (3.25A MAX) when it is a power receiving node (USB OTG) that is typically regulated to 4.9V (VBOOST[4:0] = 01010).

The device may operate in several different modes:
In HIZ mode, the reverse blocking FET (Q1), internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it is supplying DC power to the system through BATFET Q4.

In the sleep mode, the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VBUS}) is not high enough for charging the battery. In other words, V_{VBUS} is smaller than V_{BAT} + V_{SLEEP_BUCK} (where V_{SLEEP_BUCK} is a small threshold) and Buck converter is not able to charge, even at its maximum duty cycle. The Boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VBUS} is almost equal to or smaller than VBAT).

In supplement mode, the input source power is not enough to supply system demanded power and the battery assists by discharging to the system in parallel, providing the deficit.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between VAC, VBUS, BAT and V2X (only power the chip when other power sources are absent). When the voltage of the selected source goes above its UVLO level (V_{VAC} > V_{VAC_UVLO}, V_{VBUS} > V_{VBUS_UVLO} or V_{BAT} > V_{BAT_UVLO} or V_{V2X} > V_{V2X_UVLO}), a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I²C interface will also be ready for communication and all registers reset to their default values.

The V2X has the lowest priority to power the internal circuit compared with VAC, VBUS and BAT. Only when other power sources are absent, V2X can power the internal circuit and keep the chip status, and all the registers can be accessed through I²C interface. Under that conditions, chip consumes very small current (< 25μA), and only the nRST, RST0, RST1 related functions are enabled. The details usage of V2X is shown in Figure 2 or Figure 3.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage (V_{BAT}) is above depletion threshold (VBAT_DPL rising), the BATFET turns on and connects the battery to the system. The quiescent current is minimum value because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time. When only V2X is presented as a source and its voltage (V_{V2X}) is above present rising threshold (4V), nRST pulls high in default status or low if in ship mode and nRST_DIS = 0.

The discharge current through BATFET is continuously monitored. In the supplement mode, if a system overload (or short) occurs (I_{BAT} > I_{BAT_OCP}), the BATFET is turned off immediately and BATFET_DIS bit is set to 1. The BATFET will not enable until the input source is applied or one of the BATFET Enable mode (exit ship mode) methods (explained later) is used to activate the BATFET.

Power-Up Process from the Input Source

Upon connection of an input source (VBUS), its voltage sensed from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (no matter if the battery is present or not). The input current limit is determined and set before the Buck converter is started. The sequences of actions when VBUS as input source is powered up are shown below:

1. REGN LDO power-up.
2. Poor source detection (qualification).
3. Input source type detection. (Based on D+/D- input, it is used to set the default input current limit (IINDPM[5:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET, LSFET gate drivers, TSBAT rail (thermistor pin). The REGN enables when V_{VBUS} > $V_{VBUS\_PRESENT}$ is satisfied and remain valid for a 64ms delay time. Otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

In HIZ state, if switched cap fast charger is not enabled, the quiescent current drawn from VBUS is very small. System is only powered by the battery in HIZ mode.

Whenever REGN voltage is over 3V for 1ms deglitch, REGN_OK_STAT bit and REGN_OK_FLAG bit are set to 1, an INT is sent if not masked.

Poor Source Detection (Qualification)

When REGN LDO is powered, the input source (Adapter) is checked for its type and current capacity. To start the Buck converter, the input (VBUS) must meet the following conditions:

1. V_{VBUS} < V_{VBUS_OVP}.
2. V_{VBUS} > V_{VBUS_MIN} during t_{BADSRC} test period (28ms TYP) in which the I_{BAD_SINK} (25mA TYP) current is pulled from VBUS.

If the test is failed, the conditions are repeatedly checked every 2 seconds. As soon as the input source passes qualification, the VBUS_GOOD_STAT bit in status register is set to 1 and a pulse is sent to the nINT pin to inform the host. Type detection will start as next step.

Input Source Type Detection

The input source detection will run through the D+/D- lines while REGN LDO is powered and after the VBUS_GOOD_STAT bit is set. The Buck charger can detect the input source types which include SDP/CDP/DCP and non-standard adapter through the D+/D- pins following USB BC1.2 specification. INPUT_DET_DONE_FLAG bit is set to 1 and a pulse is sent to nINT pin to inform the host when the input source type detection is completed. Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINDPM[5:0]) is changed to set current limit.
2. VBUS_STAT[2:0] bits are updated to indicate USB or adapter input source types.

The input current is always limited by the IINDPM[5:0] bits and the limit can be updated by the host if needed.

Input Current Limit by D+/D- Detection

The Buck charger integrates a D+/D- based input source detection to set the input current limit when VBUS is plugged in. When input source is plugged in, the device starts USB BC1.2 detection and set the SDP/CDP/DCP related input current limit. And if the data contact detection timer expires, the non-standard adapter detection starts and then sets the input current limit. Please refer to Table 2 and Table 3.

Table 1. USB or Adapter Input Source Types by D+/D- Detection

VBUS_STAT[2:0]	USB or Adapter Input Source Types	Input Current Limit (A)
000	No Input	--
001	USB Host SDP	0.5
010	USB CDP	1.5
011	USB DCP	3.25
100	HVDCP	3.25
101	Unknown Adapter	0.5
110	Non-Standard Adapter	1/2/2.1/2.4
111	OTG	--

Table 2. Non-Standard Adapter Detection

Non-Standard Adapter	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V2P7	V_{D-} within V2P0	2.1
Divider 2	V_{D+} within V1P2	V_{D-} within V1P2	2
Divider 3	V_{D+} within V2P0	V_{D-} within V2P7	1
Divider 4	V_{D+} within V2P7	V_{D-} within V2P7	2.4

Table 3. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (I_{INDPM})
USB SDP (USB500)	500mA
USB CDP	1.5A
USB DCP	2.4A
Divider 1	2.1A
Divider 2	2A
Divider 3	1A
Divider 4	2.4A
Unknown 5V Adapter	500mA

DETAILED DESCRIPTION (continued)

Force Detection and Auto Indetification of Input Current Limit

The host can set FORCE_INDET bit to 1 in host mode to force the device to run the input source detection, and the FORCE_INDET bit returns to 0 by itself and input result is updated after the detection is completed. If AUTO_INDET_EN bit is set to 1, and then VBUS meets the input source detection conditions, Buck charger starts process automatically.

D+/D- Output Voltage Setting

When SET_DPDM_DRIVE_EN = 1, the host can set D+/D- output voltages by DP_DRIVE[2:0] and DP_DRIVE[2:0] to HIZ, 0V, 0.6V or 3.3V etc.

Table 4. DP/DM Output Setting

DP_DRIVE[2:0] or DM_DRIVE[2:0]	DP/DM Output
000	HIZ (default)
001	20kΩ pull-down
010	0.6V
011	2V
100	2.7V
101	3.3V
110	3kΩ pull-up resistor to internal 3.3V
111	Reserved

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

A wide voltage range (4V to 4.8V, 7.6V, 8.2V, 8.4V, 8.6V, 10V, 10.5V, 10.7V) is supported for the input voltage limit setting in VINDPM[3:0]. 4.5V is the default for USB.

The device supports dynamic tracking of the battery voltage (VINDPM). VINDPM_VBAT[1:0] bits can be used to enable tracking (11 to disable tracking) and set the tracking offset value. When the tracking is enabled, the input voltage limit will be set to the larger value between the VINDPM[3:0] and V_{BAT} + VINDPM_VBAT[1:0]. The VINDPM_VBAT[1:0] tracking offset can be set to 150mV, 200mV, or 250mV. And this function only takes effect when VINDPM_VBAT[1:0] is not equal to 11.

DC/DC Converter Power-Up

The switching converter composed of LSFET and HSFET is enabled and can start switching when the input current limit is set. Converter is initiated with a soft-start when the system voltage is ramped up. When SYS is greater than V_{SYS_REG} × 90% for $t_{nSYS\_OK\_DGL}$ (150ms TYP) deglitch, nSYS_OK pulls low to notify the host that the system voltage is ready. If the SYS voltage is less than V_{SYS_SHORT}, the input current is limited to 200mA or IINDPM[5:0] or the peak of inductor current, whichever is smaller. Otherwise, the limit is set to IINDPM[5:0].

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

When converter operates with 1.5MHz switching frequency (default value, can be adjust to 500kHz or 1MHz or 2MHz by setting BUCK_FREQ[1:0]) for battery charging, it acts as an efficient, fixed frequency synchronous Buck converter regardless of the input/output voltages and currents. However, it is capable of switching to PFM mode at light load when charging is disabled or when the detected battery voltage is less than minimum system voltage setting. PFM operation can be enabled or prevented in either Buck or Boost mode using the PFM_DIS_BUCK or PFM_DIS_BOOST bit. By default, Buck charger works in PFM mode to reduce the power loss at light load whenever in Buck or Boost mode.

Boost Mode

The Buck charger supports USB On-The-Go. When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (Boost mode) with 1.5MHz switching frequency (default value, can be adjust to 500kHz or 1MHz or 2MHz by setting BOOST_FREQ[1:0]) to supply power from the battery to that load. When RBFET is turn on and VAC or VBUS is used for power the external device, the USB OTG output current limit requirement is achieved by setting IBOOST_LIM[2:0]. The maximum current limit is 3.25A. Converter will be set to Boost mode if at least 30ms is passed from enabling this mode (BOOST_EN bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{BAT\_LOW\_OTG}$.
2. $V_{VBUS} < V_{BAT} + V_{SLEEP\_BUCK}$ (in sleep mode) and $V_{VBUS} < V_{VBUS\_PRESENT}$.
3. Acceptable voltage range at TSBAT pin ($V_{BHOT} < V_{TSBAT} < V_{BCOLD}$).

The output voltage is set to V_{PMID} = 4.9V and is maintained as long as V_{BAT} is above $V_{BAT\_LOW\_OTG}$. In Boost mode, the RBFET Q1 is in off state by default, which can be turned on by setting QB_EN bit to 1, and then VBUS can be connected with PMID directly. The VBUS_STAT[2:0] status register bits are set to 111 in Boost mode (OTG).

As stated before, the converter works in PFM mode by default, and PFM can be avoided by using PFM_DIS_BOOST bit in Boost mode.

DETAILED DESCRIPTION (continued)

Host Mode and Default Mode Operation with the Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as if the watchdog timer is expired. When the host is in sleep mode or there is no host, the device stays in the default mode in which the Buck charger operates as an autonomous charger. The battery is charged for 13 hours (default value for the fast charging safety timer). Then the charge stops while Buck converter continues to operate to power the system load. In the default mode, WD_TIMEOUT_FLAG bit is high.

Most of the flexibility features of the Buck charger become available in the host mode when the device is controlled by a host with I²C. By setting the WD_TIMER_RST bit to 1, the charger mode changes from default mode to host mode. In this mode the WD_TIMEOUT_FLAG bit is low and all device parameters can be programmed by the host. To prevent device watchdog reset that results in going back to default mode, the host must disable the watchdog timer by setting WD_TIMEOUT[2:0] = 000, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_TIMER_RST to prevent the setting of WD_TIMEOUT_FLAG bit. Every time a 1 is written to the WD_TIMER_RST, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WD_TIMEOUT_FLAG bit = 1), the device returns to default mode and all registers are reset to their default values except for IINDPM[5:0], PFM_DIS_BOOST, VSYS_MIN[2:0], VBOOST[4:0], VINDPM[3:0], VINDPM_VBAT[1:0], BATFET_DIS, BATFET_DLY and REG_RST bits that keep their values unchanged.

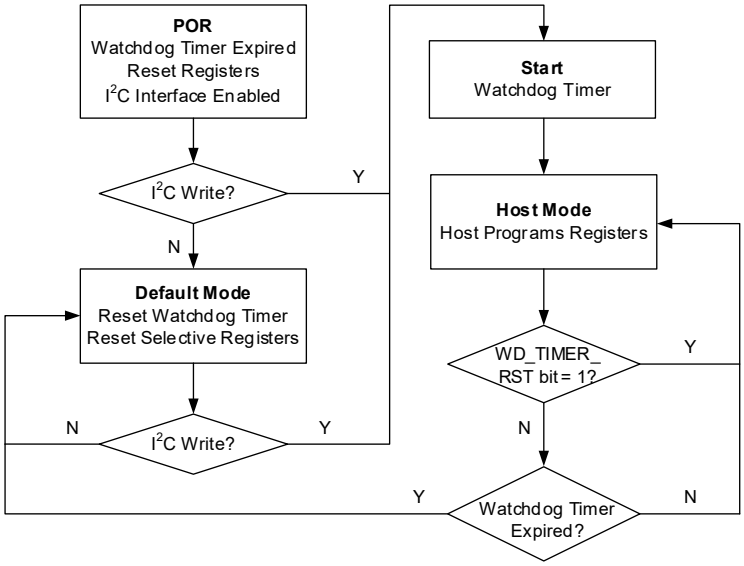


Figure 5. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The switched mode Buck charger is designed for charging single-cell Li-Ion or Li-poly batteries with a charge current up to 4A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path features low on-resistance (15mΩ) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if CHG_EN = 1. In default mode, the Buck charger runs a charge cycle with the default parameters itemized in Table 5. At any moment, the host can control the charging operations by writing the registers.

Table 5. Charging Parameter 1 Default Setting

Default Mode	Buck Charger
Charging Voltage (V_{BAT_REG})	4.208V
Charging Current (I_{CHG})	2.0A
Pre-Charge Current (I_{PRE_CHG})	150mA
Termination Current (I_{TERM})	200mA
Temperature Profile	JEITA
Safety Timer	13 hours

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

- NTC temperature fault is not asserted (TSBAT pin).
- Safety timer fault is not asserted.
- BATFET is not forced off (BATFET_DIS bit = 0).
- Charging enabled
  (2 conditions: CHG_EN bit = 1, ICHG_CC[6:0] is not 0mA).
- Battery voltage is below the programmed full charge level (V_{BAT_REG}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{BAT_REG} - 100mV to V_{BAT_REG} - 400mV configured by VRECHG[1:0] bits). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the CHG_EN bit.

Normally a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or Dynamic Power Management (DPM) mode.

Charge Status Report

The CHG_STAT[2:0] status register reports the present charging phase and status by three bits: 000 = charging disabled, 001 = in trickle-charge, 010 = in pre-charge, 011 = in fast-charge (CC mode), 100 = in fast-charge (CV mode), 101 = in charge termination.

A negative pulse is sent on nINT pin to inform the host when the charging status changes.

Battery Charging Profile

The Buck charger features a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested and appropriate current and voltage regulation levels are selected as shown in Table 6. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are trickle charge (V_{BAT} < 2.1V), pre-charge and fast-charge (constant current and constant voltage).

Table 6. Charging Current Setting Based on V_{BAT}

V_{BAT}	Selected Charging Current	Default Value in the Register	CHG_STAT[2:0]
< 2.1V	I_{TRICK}	90mA	001
2.1V to 3V	I_{PRE_CHG}	150mA	010
> 3V	I_{CHG}	2.0A	011 or 100

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: The charge current will be less than the value in the register; termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

DETAILED DESCRIPTION (continued)

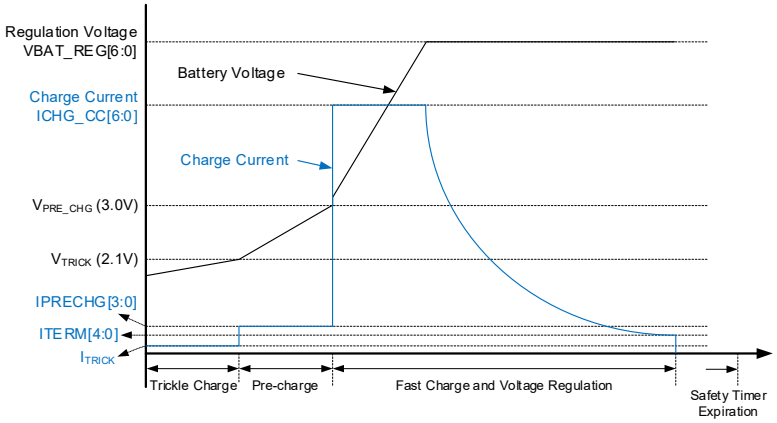


Figure 6. Battery Charging Profile

Termination

A charge cycle is terminated when the battery voltage is above the recharge threshold and the current falls below the programmed termination current. Unless there is a high power demand for system and need to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck converter continues to operate to supply power to the system.

CHG_STAT[2:0] is set to 101 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current or input voltage or junction temperature instead of charge current, termination will be temporarily prevented. TERM_EN bit is termination control bit and can be set to 0 to disable termination before it happens.

At low termination currents (200mA TYP), the offset in the internal comparator may give rise to a higher (+10mA to +20mA) actual termination current.

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines. There is no battery temperature protection when battery is discharging to the system (either boosting or not charging). The temperature protection defined by JEITA guidelines is disabled by default, and can be enabled by setting TSBAT_JEITA_EN to 1.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should to be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside normal operating temperatures (typically 0℃ and 60℃). This functionality can be disabled if not needed. Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} (V_{COLD}) to V_{T4} (V_{HOT}). Due to the sensor negative resistance, a higher temperature results in a lower voltage on TSBAT pin. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TSBAT voltage within V_{T1} (V_{COLD}) to V_{T4} (V_{HOT}) window limits. If during the charge, battery gets too cold or too hot and TSBAT voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V.

DETAILED DESCRIPTION (continued)

The Buck charger exceeds the JEITA requirement by its flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage is set to the lower of V_{BAT_REG} and V_{BAT_REG} - 50mV or V_{BAT_REG} -150mV or V_{BAT_REG} - 200mV set by JEITA_VSET_WARM[1:0], and the charge current can be reduced down to 0% or 20% or 50% or 100% of fast charging current by the JEITA_ISET_WARM[1:0] bits. At cool temperatures (T1 - T2), the current setting can be reduced down to 0% or 20% or 50% or 100% of fast charging current selectable by the JEITA_ISET_COOL[1:0]. Additional, the cool threshold T2 and warm threshold T3 can be changed through JEITA_COOL[1:0] and JEITA_WARM[1:0].

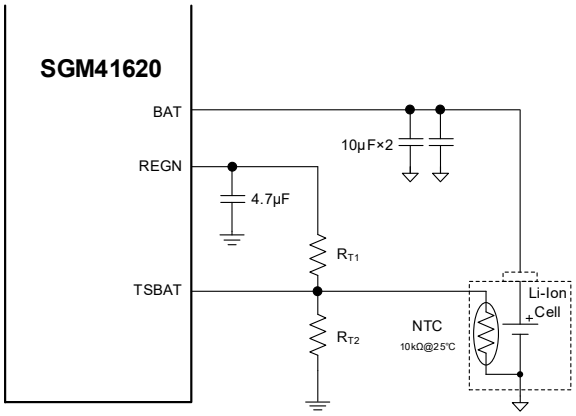


Figure 7. Battery Thermistor Connection and Bias Network

A 103AT-2 type thermistor is recommended for use with the Buck charger. Other thermistors may be used and bias network (Figure 7) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

where V_{T1} (V_{COLD}) and V_{T4} (V_{HOT}) are cold (T1) and hot (T4) temperature threshold voltage on TS pin as percentage to V_{REGN}, and R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired cold and hot temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor, R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ that results in: R_{T1} = 5.33kΩ and R_{T2} = 31.51kΩ. The standard value of R_{T1} is 5.23kΩ and that of R_{T2} is 30.9kΩ.

Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable to monitor the battery temperature for safety during the Boost mode. The temperature must remain within the V_{BCOLD} to V_{BHOT} thresholds otherwise the Boost mode will be suspended and VBUS_STAT[2:0] bits are set to 111. Moreover, TSBAT_HOT_STAT or TSBAT_COLD_STAT bit is updated to report Boost mode cold or hot condition. Once the temperature returns within the window, the Boost mode is resumed and TSBAT_HOT_STAT or TSBAT_COLD_STAT bit is cleared to 0.

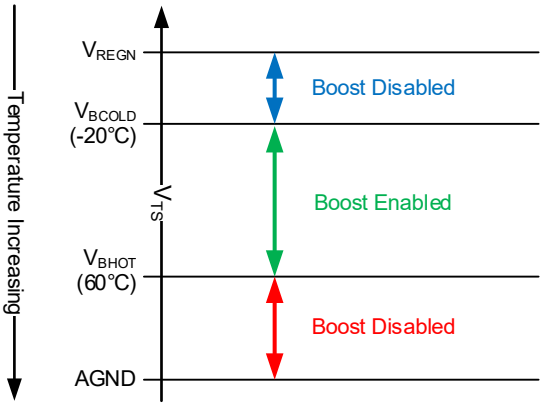


Figure 8. TSBAT Pin Thermistor Temperature Window Settings in Boost Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, CHG_TIMEOUT_STAT and CHG_TIMEOUT_FLAG bit are set to 1 and a negative pulse is sent to nINT pin. By default the charge time limit is 4 hours if the battery voltage does not rise above V_{PRE_CHG} threshold and 13 hours if it goes above V_{PRE_CHG}. This feature is optional and can be disabled by clearing CHG_TIMER_EN bit. The 13 hours limit can also be changed to 5, 8.8, 25 hours by setting CHG_TIMER[1:0] bits to 00, 01, and 11 respectively.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation, JEITA cool or thermal regulation because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 5 hours and the charger is regulating the input current (IINDPM_STAT bit = 1) in the whole charging cycle, the actual safety time will be 10 hours. Clearing the TMR2X_EN bit will disable the half clock rate feature.

DETAILED DESCRIPTION (continued)

The safety timer is paused if a fault occurs or charger is in supplement mode, charging is suspended. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling CHG_EN bit, the timer resets and restarts a new timing.

Narrow Voltage DC (NVDC) Design

The Buck charger features an NVDC design using the BATFET that connects the system and battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Buck converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. VSYS_MIN[2:0] register sets the minimum system voltage (default 3.5V). If the system is in minimum system voltage regulation, VSYSMIN_REG_STAT bit is set.

The BATFET operates in linear region when the battery voltage is below the minimum system voltage setting. The system voltage is regulated to 250mV (TYP) above the minimum system voltage setting. The battery gradually gets charged and its voltage rises above the minimum system voltage and lets BATFET to change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 60mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. Charging is disabled and the battery voltage is above the minimum system voltage setting.

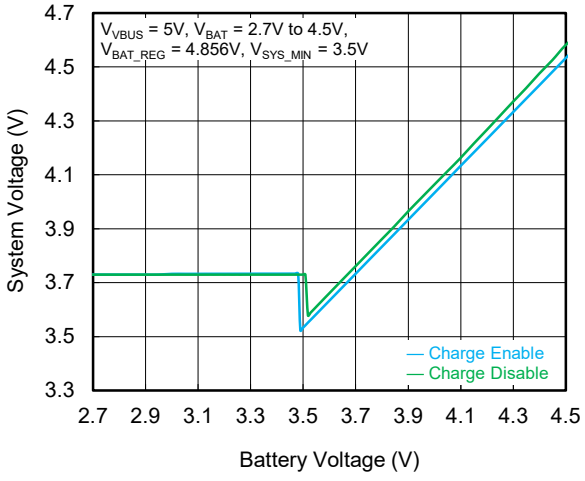


Figure 9. System Voltage vs. Battery Voltage

Dynamic Power Management (DPM)

The Buck charger features a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specs. Overloading an input source may results in either current trying to exceed the input current limit (I_{INDPM}) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the V_{SYS} regulated to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased to and reached zero, but the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and to provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during IINDPM or VINDPM, respectively. Figure 10 summarizes the DPM behavior (IINDPM type) for a design example with a 9V/1.2A adapter, 3.2V battery, 2.8A charge current setting, and 3.4V minimum system voltage setting.

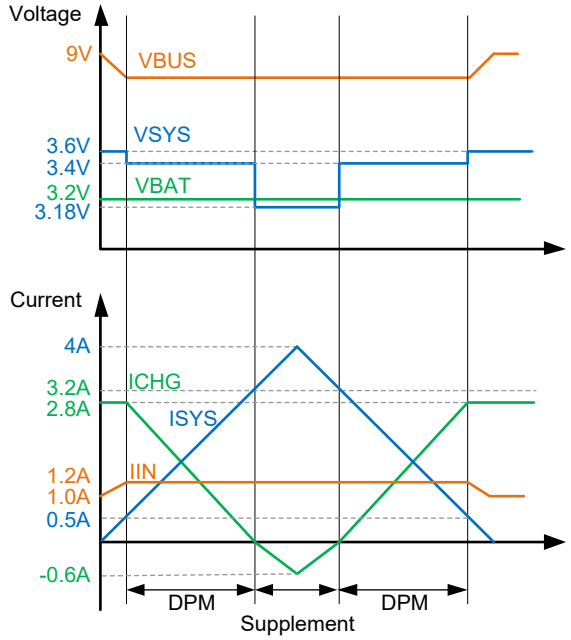


Figure 10. DPM Behavior Plot

DETAILED DESCRIPTION (continued)

Supplement Mode

If the system voltage drops below the battery voltage, the BATFET gradually starts to turn on. The threshold margin is 160mV if V_{SYS_MIN} setting is less than V_{BAT} and 50mV if V_{SYS_MIN} setting is larger than $V_{BAT.}$ At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation) such that the BATFET V_{DS} stays at 20mV. At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by R_{DSON} × I_{BAT}). Use of the MOSFET linear mode at lower currents prevents swinging oscillation of entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 11. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

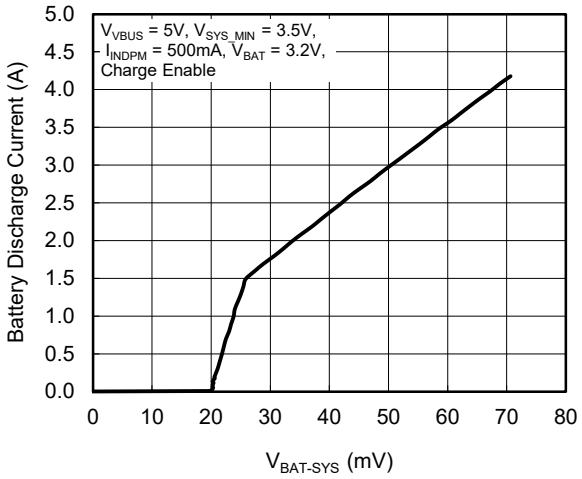


Figure 11. BATFET Gate Regulation V-I Curve

nRST and BATFET Control for System Power Reset and Ship Mode

Ship Mode (BATFET Disable)

Ship mode is usually used when the system is stored or in idle state for a long time or is in shipping. In such conditions, it is better to completely disconnect battery and make system voltage zero to minimize the leakage and extend the battery life. To enter ship mode, the BATFET has to be forced off by setting BATFET_DIS bit to 1. The BATFET turns off immediately if BATFET_DLY bit is 0, or turns off after a t_{SM_DLY} delay (20 seconds) if BATFET_DLY bit is set, and the nRST switches from high to low at the same time. In ship mode, the greater one of V2X and VBAT is selected to power the chip, and SGM41620 consumes the minimum current under this condition.

Exit Ship Mode (BATFET Enable)

To exit the ship mode and enable the BATFET, one of the following methods can be applied:

With the chip no powered by VBUS:
1. Connect the adapter to the input with a valid voltage to the VBUS input.
2. Pull RST0 pin from logic high to low to enable BATFET for example by shorting RST0 to GND. The negative pulse width should be at least a $t_{SHIPMODE}$ (2s TYP) for deglitching. Once the action for exiting ship mode is asserted, nRST output high level, V2X or VBAT continues to power the chip until any one of other power is valid.

With the chip already powered by VBUS:
1. Clear BATFET_DIS bit using host and I²C.
2. Set REG_RST to 1 to reset all registers.
3. Apply a negative pulse to RST0 pin (same as 2).

Full System Reset with BATFET Using RST0 and RST1

When the input source is not present, the BATFET can act as a load on/off switch between the system and battery. This feature can be used to apply a power-on reset to the system. Host can toggle BATFET_DIS bit to cycle power off/on and reset the system. Two push-buttons connected to both RST0 and RST1 pin respectively or negative pulse on both pins can also be used to manually force a system power cycle when BATFET is ON (BATFET_DIS bit = 0). For this function, a negative logic pulse with a minimum width of t_{SYS_RST} (10s TYP) must be applied to both RST0 and RST1 pin that results in a temporary BATFET turn off for t_{BATFET_RST} (200ms TYP) that automatically turns on afterward. Setting BATFET_RST_EN to 0 can disable the function.

Full system reset function either with or without adapter present. If BATFET_RST_WVBUS = 1, the system reset function starts after t_{SYS_RST} when both RST0 and RST1 pin are pulled low. Once the reset process starts, the device first get into HIZ mode to turn off the converter, and then turn off BATFET for t_{BATFET_RST}. If BATFET_RST_WVBUS = 0, the system reset function doesn't start till t_{SYS_RST} after both RST0 and RST1 pin are pulled low and adapter is removed.

In summary the RST0 or RST1 pin controls BATFET and system reset in two different ways:

DETAILED DESCRIPTION (continued)

1. Enable BATFET: Applying an RST0 logic high to low transition with longer than $t_{SHIPMODE}$ deglitch time (negative pulse) turns on BATFET to exit ship mode (left). When exiting shipping mode, HIZ is enabled (HIZ_EN = 1) as well. HIZ can be disabled (HIZ_EN = 0) by the host after exiting shipping mode. OTG cannot be enabled (BOOST_EN = 1) until HIZ is disabled.

2. Reset BATFET: By applying a logic low for a duration of at least t_{SYS_RST} to both RST0 and RST1 pin and BATFET is allowed to turn on (BATFET_DIS bit = 0), the BATFET turns off for t_{BATFET_RST} and then it is re-enabled resulting in a system power-on reset (right); At the same time, RESET_FLAG is asserted to 1, and sent INT to notify the host by nINT pin. This function can be disabled by clearing BATFET_RST_EN bit.

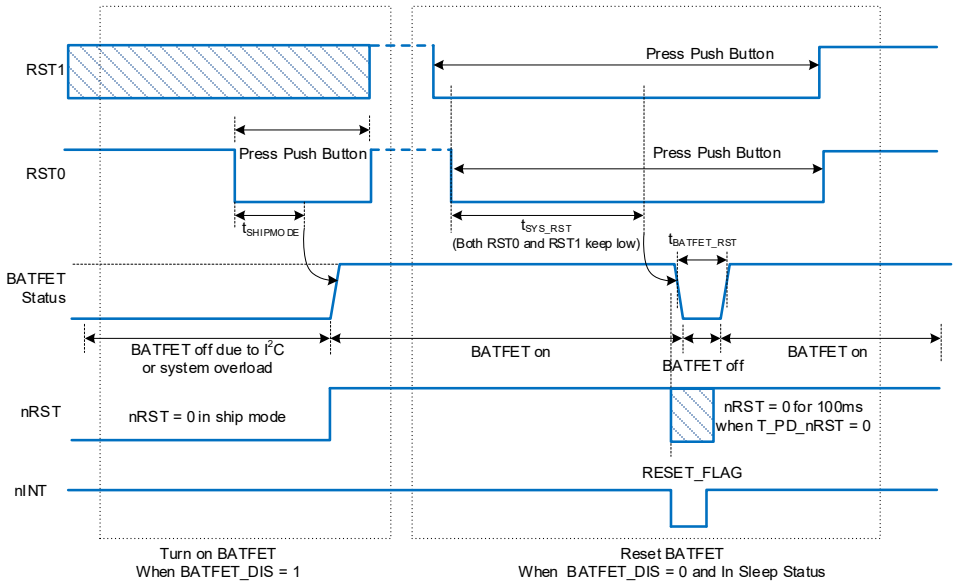


Figure 12. RST0 and RST1 Enable and Reset BATFET Timing

A typical push button circuit for RST0 is given in Figure 13.

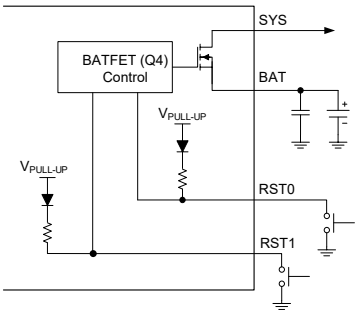


Figure 13. RST0 and RST1 Manual Operation Circuit

DETAILED DESCRIPTION (continued)

Status Outputs (nSYS_OK and nINT)

System Ready Indication

The nSYS_OK pin has open drain configuration, which is pull low if the following conditions is satisfied.

• V_{VBUS} is in the operating range: $V_{VBUS\_PRESENT}$ < V_{VBUS} < V_{VBUS_OVP}.

• Buck charger soft-start is finished

The signal can be used to notify the host the system power is ready.

INT

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt it can react and check the charger situation on time. For avoiding sending INT to host frequently, when a previous 256μs negative pulse is over, even if a new event happens quickly, Buck charger still needs to wait for 256μs to send a new 256μs negative pulse.

The details in the FLAG registers indicate that an event occurred, and INT flag bit is not reset in until the host reads it. A new fault will not assert a new INT pulse until the previous faults are cleared.

Buck Charger Protection Features

Monitoring of Voltage and Current

During the converter operation the input and system voltages (VBUS and VSYS) and switch currents are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as will be explained below.

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage (VBUSOVP)

Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OVP} over-voltage limit that is programmable by VBUS_OVP[1:0] in REG04. It is selectable among 6V, 10V, 12V, and 14V (default).

Each time VBUS exceeds the OVP limit, VBUS_OVP_STAT and VBUS_OVP_FLAG bits are set to 1, an INT pulse is asserted. As long as the over-voltage persists, the VBUS_OVP_STAT bit is set to 1 in REG0C. Flag bit will be cleared to 0 if the host reads the flag register. Charger resumes its normal operation when the voltage comes back below OVP limit.

2. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold can be set from 104% to 110% (programmable by VSYSOVP_TH[1:0]) of system regulation voltage. Once a SYSOVP occurs, switching stops to clamp any overshoot and a 25mA sink current is applied to SYS to pull the voltage down.

Boost Mode Voltage and Current Monitoring

In Boost mode the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Soft-Start on VBUS

Boost mode begins with a soft-start to prevent large inrush currents when it is enabled.

2. Output Short Protection for VBUS

Short circuit protection is provided for VBUS output in Boost mode when RBFET Q1 is turn on by QB_EN bit. To accept different types of load connected to VBUS and OTG adaptation, an accurate constant current regulation control is implemented for Boost mode. In case of a short circuit on PMID_BUCK pin, the Q1 turns off and retries 7 times at 480ms interval (Hiccup). In the Hiccup state, OTG_HICCUP_FLAG and OTG_HICCUP_STAT bits are set to 1, an INT pulse is asserted. If short is not removed after retries, the OTG will be disabled by clearing BOOST_EN bit.

3. Output Over-Voltage Protection for VPMID_BUCK

In Boost mode, converter stops switching and exits Boost mode (by clearing BOOST_EN bit) if PMID_BUCK voltage rises above regulation and exceeds the V_{PMID_OVP} over-voltage limit (6.2V TYP). VPMID_OVP_OTG_FLAG is set to 1, and an INT pulse is sent.

DETAILED DESCRIPTION (continued)

Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of 120℃ is considered for maximum IC surface temperature in Buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to 120℃ (thermal regulation mode) and sets the TDIE_REG_FLAG and TDIE_REG_STAT bits to 1, and an INT pulse is sent. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the temperature exceeds T_{SHUT} (150℃), thermal shutdown protection arises in which the converter is turned off, TSHUT_STAT and TSHUT_FLAG bits are set to 1, and an INT pulse is sent. When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

Boost Mode Thermal Protections

Similar to Buck mode, T_J is monitored in Boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (150℃), Boost mode will be disabled (BOOST_EN bit clears). BATFET will resume if T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}). Boost can recover again by re-enabling BOOST_EN bit by host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 4% above the battery regulation voltage setting. In case of a BATOVP, charging or external direct charging stops right away, the VBAT_OVP_BUCK_STAT and VBAT_OVP_BUCK_FLAG bits are set to 1 and an INT pulse is sent.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level (V_{BAT_DPL} falling), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{TRICK} current (90mA TYP) first as long as $V_{BAT} < V_{TRICK}$. When battery voltage is increased and $V_{TRICK} < V_{BAT} < V_{PRE\_CHG}$, the charge current will increase to the pre-charge current level programmed in the register REG0x36 IPRECHG[3:0] bits.

Battery Over-Current Protection for System

The BATFET will latch off, if its current limit is exceeded due to a short or large overload on the system ($I_{BAT} > I_{BAT\_OCP}$). To reset this latch off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

DETAILED DESCRIPTION (continued)

8A Switched Cap Fast Charger

The SGM41620 integrated an efficient 8A switched cap fast charger that can operate in voltage divider mode or in bypass mode. A two-channel switched capacitor core is integrated in the device to minimize the ripples and improve efficiency in the voltage divider mode. A FET control output for protection, a reverse blocking NFET and all other necessary protection features for safe charging are included.

Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. The basic principle of operation is shown in Figure 14. In period 1, Q_{CH} and Q_{CL} are tuned on and V_{PMID_CP} charges the C_{FLY} and the battery (in series) such that:

$$V_{CFLY} = V_{PMID\_CP} - V_{BAT} \quad (3)$$

In period 2, Q_{DH} and Q_{DL} are turned on and C_{FLY} appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \quad (4)$$

Ignoring the small fluctuation of the capacitor and battery voltages in period 1 and 2 in steady state operation, Equation 3 and 4 can be combined to calculate capacitor voltage:

$$V_{CFLY} = V_{BAT} = V_{PMID\_CP}/2 \quad (5)$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID\_CP} \times I_{BUS} = V_{BAT} \times I_{BAT} \quad (6)$$

or

$$I_{BUS} = I_{BAT}/2 \quad (7)$$

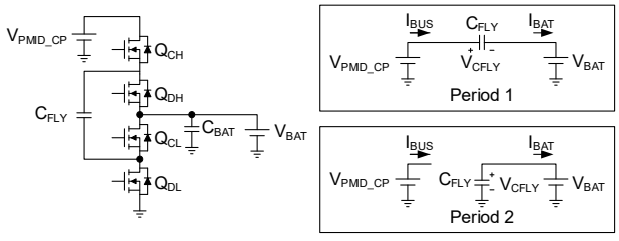


Figure 14. Voltage Divider Charger Operating Principle

Assuming no charge leakage path and considering R_{EFF} as the effective input to output resistance (due to the switch on-resistances and C_{FLY} losses), the divider can be modeled as shown in Figure 15. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The voltage divider has two channels of such architecture operating at f_{SW} frequency with 180° phase difference. Each channel provides $I_{BAT}/2$ at the BAT node, so:

$$V_{BAT} = ½V_{PMID\_CP} - ½R_{EFF} \times I_{BAT} \quad (8)$$

At low switching frequencies, the capacitor charge sharing losses are dominant and $R_{EFF} \approx 1/(4f_{SW}C_{FLY})$. As frequency increases, R_{EFF} finally approaches $(R_{DS\_QCH} + R_{DS\_QDH} + R_{DS\_QCL} + R_{DS\_QDL})/2$.

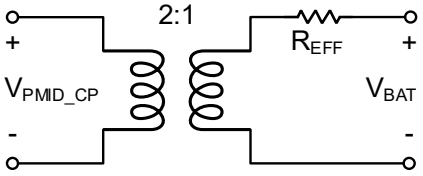


Figure 15. Model of Voltage Divider

The two-channel interleaved operation ensures a smooth input current and simplifies the noise filtering. The VBAT ripple can be estimated by first order approximation of C_{FLY} voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time.

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

DETAILED DESCRIPTION (continued)

Bypass Mode

The switched cap fast charger can operate in bypass mode when V_{BUS} is close to the V_{BAT}. When such valid voltage is present on VBUS, the device enters bypass mode and all switches between VBUS and VBAT are fully turned on while the other switches are kept off. When V_{BUS} is near V_{BAT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 6A (Maximum 6A continuous current is recommended in this mode).

The output voltage is close to the V_{BUS} minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two channels in parallel. So the R_{EFF} in bypass mode is:

$$R_{EFF}\ (\text{Bypass mode}) \approx (R_{DS\_QCH1} + R_{DS\_QDH1}) \,||\, (R_{DS\_QCH2} + R_{DS\_QDH2}) \quad (9)$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

Charge System

The SGM41620 is a slave charger device and needs a host. The host must set up all protection functions and disable the switched mode Buck charger before enabling the switched capacitor charger. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 16 shows the block diagram of a charge system using the SGM41620 along with other devices. In this system, the SGM41620 can be used to detect the presence of adapter by the integrated PD PHY, which is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the 4A switching mode Buck charger and the 8A switched capacitor fast charger separately that provides high current charging. The communication between those devices is through I²C interface.

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 17. During the trickle charge and pre-charge, the charging is controlled by the Buck switching charger. Once the battery voltage reaches $V_{BAT\_MIN\_CP}$ (2.9V TYP), the adapter can negotiate for a higher bus voltage and enable the switched cap fast charger for charging (bypass or voltage divider mode). Once the battery voltage reaches the V_{BAT_REG} point, the SGM41620 provides feedback to the adapter to reduce the current. This will eventually reduce and ramp down the bus current below I_{BUS_UCP} falling threshold.

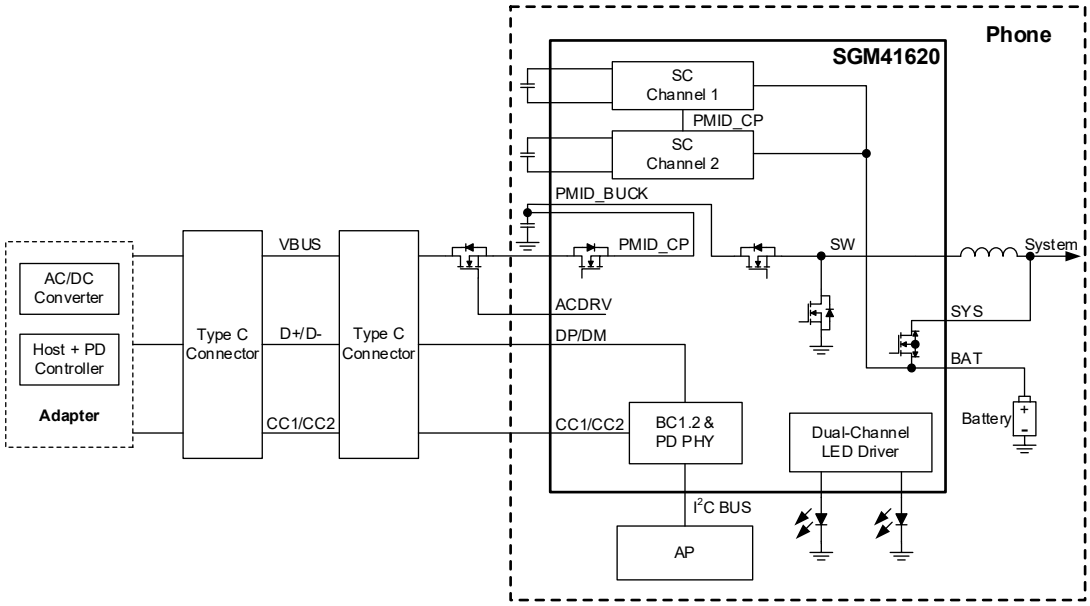


Figure 16. Simplified Charge System

DETAILED DESCRIPTION (continued)

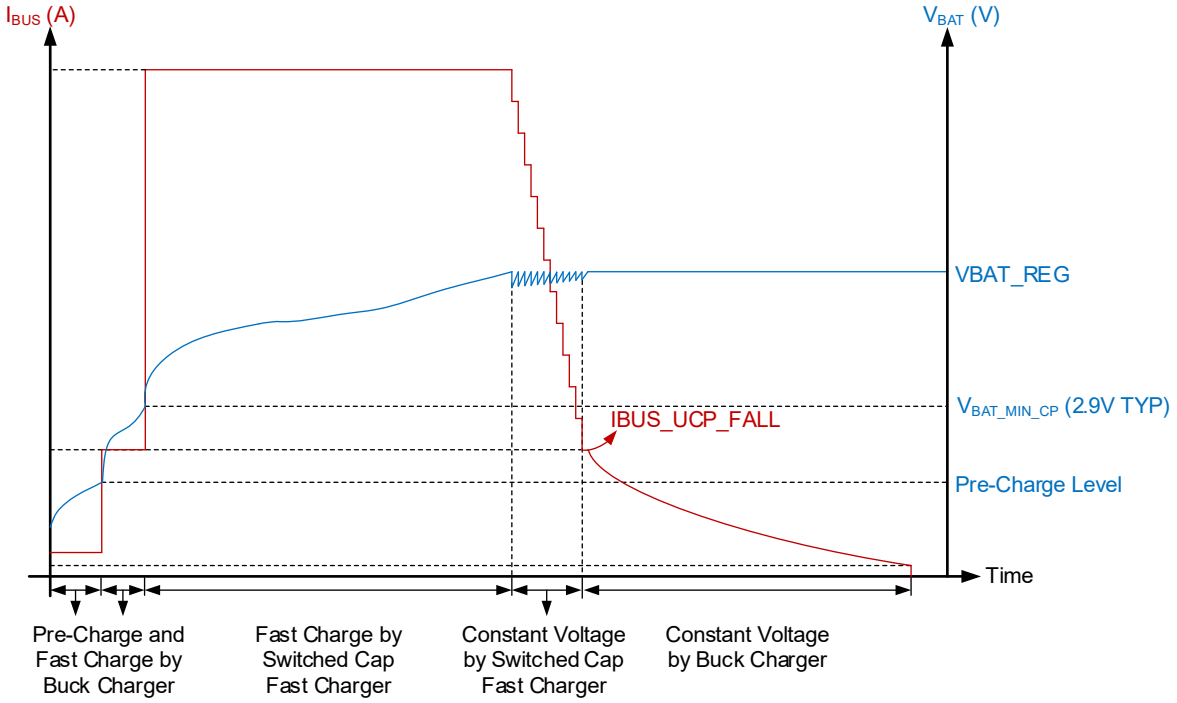


Figure 17. SGM41620 System Charging Profile

Device Power-Up

The fast charger is powered by the greater of VBUS or BAT (battery). The voltage must be greater than the $V_{VBUS\_PRESENT}$ or $V_{BAT\_MIN\_CP}$ rising thresholds to be a valid supply. However, once the voltage rises above the V_{VBUS_UVLO} or V_{BAT_UVLO} rising thresholds, the device begins to consume power.

The device has a watchdog timer (REG0x07), which is enabled by default. If the WD_TIMER_RST bit is not written to 1 before the watchdog expires, the part will stop switching. The first read of the watchdog timer flag will always read 1. During initial device power-up, after address pin detection is completed, an INT pulse is triggered to indicate a watchdog timeout. The host should not attempt to read or write before this initial nINT signal.

The device will not charge when first powered up because the default charging state is never enabled. The ADC is available before charging is enabled, so the host knows the system parameters before charging is enabled. The charger cannot be enabled if the VBAT voltage is not greater than $V_{BAT\_MIN\_CP}$ (2.9V TYP).

VBUS In-Range (VBUS_ERROR_LO and VBUS_ERROR_HI)

The VBUS_ERROR_LO and VBUS_ERROR_HI functions are included to avoid problems due to wrong VBUS setting for charging. If V_{VBUS} is less than (V_{BAT} × 2.04) or above (V_{BAT} × 2.4) in voltage divider mode, the device remains in charge initiation operation. If the bypass mode is selected, the range is from (V_{BAT} × 1.02) to (V_{BAT} × 1.2). Charging will start once V_{VBUS} is within the charge range. VBUS_ERROR_LO and VBUS_ERROR_HI functions is enabled only when VBUS_IN_RANGE_DIS = 0.

DETAILED DESCRIPTION (continued)

Charging Start-Up

The host needs to set all protections to the desired thresholds before enabling charging. The available protections are VBAT_OVP, VBATSNS_OVP, IBUS_OCP, IBUS_UCP, PMID2BAT_OVP, PMID2BAT_UVP, VAC_OVP, BUS_OVP, TSBUS_FAULT and TSBAT_FAULT. These can be found in registers REG0x04 to REG0x06 and REG0x60 to REG0x63. The *_OVP, *_UVP, *_UCP and *_OCP registers set the related thresholds, if these conditions are met, the charger will stop switching, and an INT will be sent to host if the mask bit is enabled.

It is recommended to start with VBUS close to (V_{BAT} × 2.04) in voltage divider mode or (V_{BAT} × 1.02) in bypass mode when charging is enabled. When charging is enabled, if no protection such as OVP, OTP, VBUS_ERROR_LO, VBUS_ERROR_HI happens, fast charger starts to switching, then SCC_SWITCHING_STAT bit is set to 1, SS_TIMEOUT timer starts to count if not disabled, finally current will start flowing to the battery. Raising the bus voltage will increase the battery charging current. If a current limit source is used, the voltage can be boosted until the current limit is reached. The bus current I_{BUS} must reach the $I_{BUS\_UCP\_R}$ threshold within SS_TIMEOUT[2:0] setting. These parameters can be set in register REG0x65. If $I_{BUS\_UCP\_R}$ threshold is not met within SS_TIMEOUT[2:0] setting, the charging stops and the startup sequence must be performed again.

nINT Pin related Registers

The nINT pin is an open-drain pin and needs to be pulled up to a voltage using a pull-up resistor. nINT is normally high and is set low during t_{INT} when the device needs to alert the host of a fault or state change. The behavior of the nINT pin is determined by registers. Details in the STAT register show the current state of the device and are updated as the state changes.

The details in the FLAG register indicate that an event occurred, and the bits are cleared when read. If the event still exists after reading and clearing the FLAG register, another nINT signal will not be sent unless the status is released and triggered again. Details in the MASK register allow the user to disable interrupts on the nINT pin, but the STAT and FLAG registers are still updated even if nINT is not pulled low.

Triggering any of these protection faults will cause the Q1 (or RBFET) to be shut down. Masking a fault does not disable the protection. It just prevents the INT from being triggered by the event. Disabling faults will keep this state and flag bits reset and prevent interrupts from occurring.

VAC Over-Voltage Protection (VAC_OVP)

The SGM41620 monitors the adapter voltage on the VAC pin to control the external OVPFET using ACDRV output. The VAC over-voltage protection circuit is powered by VAC and is enabled if V_{VAC} rises above $V_{VAC\_PRESENT\_R}$. If V_{VAC} is above $V_{VAC\_PRESENT}$ rising threshold, fast chargers start to pull down 100mA at VBUS for 15.5ms. After 15.5ms deglitch, a 4.75V gate voltage is sent to the ACDRV output to turn on the external OVPFET. If the V_{VAC} is over the $V_{VAC\_OVP\_R}$ threshold, the gate voltage drop quickly to VBUS and finally discharge to 0V slowly, and then the OVPFET is fully turned off. The V_{VAC_OVP} threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC pin and the external OVPFET.

Input Short-Circuit Protection (BUS_SCP, PMID2BAT_UVP and IBUS_RCP)

The BUS_SCP function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFET is turned on or if V_{VBUS} rises above $V_{VBUS\_PRESENT}$ rising threshold. If the V_{VBUS} falls below 2.4V, the OVPFET is turned off, and charging is stopped, SCC_EN bit is reset to 0.

During charging process, if $V_{PMID\_CP}/2 - V_{BAT}$ in voltage divider mode or $V_{PMID\_CP} - V_{BAT}$ in bypass mode is less than $V_{PMID2BAT\_UVP}$ (set by PMID2BAT_UVP[2:0] bits) for 100ns or the Q1 reverse current rises above 1A for 1μs (IBUS_RCP), the Q1 is turned off immediately, and charging is stopped, SCC_EN bit is reset to 0, the related flag bit will set to 1 and an INT pulse is generated if not masked.

Input and Battery Over-Voltage Protection (VBUS_OVP and VBATSNS_OVP)

The VBUS_OVP and VBATSNS_OVP functions detect input and battery voltage conditions. If either input or output voltage is higher than the protection threshold, the charger is turned off and SCC_EN bit is reset to 0. The VBATSNS_OVP uses BATP and BATN remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a series 100Ω resistor on the BATP/BATN pin is required. The VBUS_OVP and VBATSNS_OVP thresholds can be set by I²C serial interface.

DETAILED DESCRIPTION (continued)

Input Over-Current Protection (IBUS_OCP)

The IBUS_OCP function monitors the input current via Q1. If SCC_EN bit is set to enable charge, the Q1 is turned on and the IBUS_OCP function starts detecting the input current. If the I_{BUS} reaches I_{BUS_OCP} threshold, the device stops charging and resets SCC_EN bit is reset to 0. The IBUS_OCP thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q1. After charging is started, a maximum 10s timer (set by the SS_TIMEOUT[2:0] bits in REG0x65) is enabled and I_{BUS} current is compared with $I_{BUS\_UCP\_R}$ threshold. If I_{BUS} cannot exceed I_{BUS_UCP} rising threshold within the SS_TIMEOUT period, the charging will be stopped and SCC_EN bit is reset to 0. If I_{BUS} exceeds I_{BUS_UCP} rising threshold within the SS_TIMEOUT period, the timer is stopped and reset, and then if I_{BUS} falls below the $I_{BUS\_UCP\_F}$ threshold, the charging will be stopped and SCC_EN bit is reset to 0.

VBAT Short-Circuit and Over-Voltage Protection (VBAT_SCP, PMID2BAT_OVP and VBAT_OVP)

The VBAT_SCP function monitors the BAT pin for short-circuit protection. This function is only enabled during charging. If V_{BAT} falls below 2.6V for 100ns deglitch, the charger is turned off and SCC_EN bit is reset to 0. Also, the VBAT_SCP_FLAG bit is set to 1, and an INT pulse is generated if not masked. During charging process, if $V_{PMID\_CP}/2$ - V_{BAT} in voltage divider mode or V_{PMID_CP} - V_{BAT} in bypass mode is less than $V_{PMID2BAT\_OVP}$ (set by PMID2BAT_OVP[2:0] bits), the Q1 is turned off, and charging is stopped. SCC_EN bit is reset to 0, the flag bit will set to 1 and an INT pulse is generated if not masked.

The VBAT_OVP function monitors the BAT pin for over-voltage protection, which is enabled during charging, if V_{BAT} rise above 5V threshold for 6μs deglitch, the charger is turned off and SCC_EN bit is reset to 0. Also, the VBAT_OVP_CP_FLAG bit is set to 1 and an INT pulse is generated if not masked.

CFLY Short-Circuit Protection (CFLY_SCP)

The CFLY_SCP function identifies the health of flying capacitors before and during voltage divider switching (charging state). The device initialization process is started after SCC_EN bit is set to 1 and SCC_MODE bit is set to 0. When V_{VBUS} is in the charge range, the flying capacitors (C_{FLY}) in both channels are pre-charged. A C_{FLY} short-circuit is detected if they cannot be charged, and the voltage between V_{CFHx} and V_{CFLx} remains below V_{BAT} - 0.6V. If so, the initialization process is stopped and SCC_EN bit is reset to 0. Even if C_{FLY} capacitors pass the short-circuit test in the initialization process, the CFLY_SCP function remains active and whenever a V_{CFLY} voltage falls below V_{BAT} - 0.6V, the charger is turned off and SCC_EN bit is reset to 0. The PIN_DIAG_FAIL_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY_SCP event, other protection events such as IBUS_OCP, VBAT_OVP or CONV_OCP may occur.

Converter Over-Current Protection (CONV_OCP)

The CONV_OCP function monitors the converter switches operating currents cycle by cycle. If the Q_{CHx} and Q_{DLx} current reach switching OCP threshold during voltage divider mode, the CONV_OCP_FLAG bit is set to 1 and an INT pulse is generated, the charging is stopped and SCC_EN bit is reset to 0.

TDIE Over-Temperature Protection, TSBUS, and TSBAT Temperature Monitoring

The TDIE_OTP function prevents charging in over-temperature condition. The die temperature is monitored and if the +150℃ threshold is reached, the charging is stopped and SCC_EN bit is reset to 0. The startup sequence cannot be initiated again until the die temperature falls down to +120℃.

DETAILED DESCRIPTION (continued)

The device features three temperature sensing mechanisms to protect the device and system during charging: TSBUS (or EDL_TSBUS) to monitor cable connector temperature, TSBAT to monitor battery temperature, and TDIE to monitor device internal junction temperature. TSBUS and TSBAT operate only with active input power. Both TSBUS and TSBAT rely on a resistor divider with an external pull-up voltage to REGN. Connect a negative coefficient thermistor in parallel with the low-side resistor. Faults on the TSBUS and TSBAT pins are triggered on the falling edge of the voltage threshold, indicating a "hot" temperature. Adjust the threshold using the TSBUS_FAULT and TSBAT_FAULT registers. If the percentage is below of the fault setting, a TSBUS_TSBAT_FAULT interrupt will be sent. If TSBUS_TSBAT_FLT_EN is set to 0, the TSBUS_FAULT and TSBAT_FAULT interrupts will not be triggered. The R_{LO} (low side of the resistor divider) and R_{HI} (high side of the resistor divider) resistors should be chosen according to the NTC used. If using 10kΩ NTC, use 10kΩ resistors for R_{LO} and R_{HI}. If using 100kΩ NTC, use 100kΩ resistors for R_{LO} and R_{HI}. The ratio of V_{TSBUS}/V_{REGN} or V_{TSBAT}/V_{REGN} can be set from 0% to 50%, the voltage of TSBUS or TSBAT pin is determined by the following formula.

$$V_{TSBUS} \text{ or } V_{TSBAT}\,(V) = \frac{\dfrac{1}{\left(\dfrac{1}{R_{NTC}}+\dfrac{1}{R_{LO}}\right)}}{R_{HI}+\dfrac{1}{\left(\dfrac{1}{R_{NTC}}+\dfrac{1}{R_{LO}}\right)}} \times V_{REGN} \quad (10)$$

The percentage of the TSBUS or TSBAT pin voltage is determined by the following equation.

$$\text{TSBUS or TSBAT}\,(\%) = \frac{\dfrac{1}{\left(\dfrac{1}{R_{NTC}}+\dfrac{1}{R_{LO}}\right)}}{R_{HI}+\dfrac{1}{\left(\dfrac{1}{R_{NTC}}+\dfrac{1}{R_{LO}}\right)}} \quad (11)$$

The TSBUS_FLT and TSBAT_FLT are disabled by fault. Setting the TSBUS_TSBAT_FLT_EN bit to 1 can enable these functions. If the TSBUS_FLT, TSBAT_FLT thresholds are reached, the SCC_EN bit is set to 0 and the start-up sequence must be followed to resume charging.

Dual-Channel LED Driver

Dual-channel LED driver can be used to drive the flash LED and torch LED simultaneously. The maximum driving current for flash LED can reach 1.5A; the maximum driving current for torch LED can reach 0.5A. Except the normal control, LED driver integrates the multiple status monitoring and protections. The LED1 and LED2 work independently and have the same current capability, both of which can be configure as flash mode or torch mode, it's not recommended that configure the LED1 and LED2 as flash mode simultaneously for the thermal consideration.

LED driver is in shutdown status by default, host need to enable the LED driver by setting the LED_EN bit to 1 firstly. Once LED driver is enabled, the flash mode, torch mode, status and flag and so on are active.

FLASH Mode

In flash mode, the LED current sources (LED1/2) provide 119 target current levels from 25mA to 1500mA. Once the Flash sequence is activated (setting FLED1/2_EN bit to 1), the current source (LED) ramps up to the programmed flash current (FLED1/2_BR[6:0] bits) by from 0mA to the programmed current with 128 steps, the ramping up/down time is set by FRPT[2:0]. When the device is enabled in flash mode through the enable bit (FLED1/2_EN), the corresponding mode bit is cleared after a flash timeout event. Particularly, flash mode can only be activated when VBAT is higher than $V_{MINVBAT\_EN\_FLASH}$ rising threshold and FLASH_VDD voltage is higher than TORCH_VDD voltage.

Torch Mode

By default, the LED current sources (LED1/2) provide 39 target current levels from 25mA to 500mA with 12.5mA step. The Torch currents are adjusted via the LED1 and LED2 torch brightness registers (TLED1_BR_CTR, TLED2_BR_CTR). Torch mode is activated by the Enable bit (TLED1_EN or TLED2_EN). Once the Torch sequence is activated the active current sources (LED1/2) ramps up to the programmed Torch current by stepping from 0mA to the programmed current with 128 steps. The rate at which the current ramps is determined by TRPT[2:0] bits. When TORCH_STEP_CTRL bit = 1, the LED current sources (LED1/2) provide 256 target current levels from 6.25mA to 404.6875mA with 1.5625mA step.

DETAILED DESCRIPTION (continued)

Fault Operation

If the LED driver enters a fault condition such as flash timeout, LED short, UVLO, and OVP, the device sets the appropriate flag in the LED_FLAG register (0x89), and places the device into standby by clearing the corresponding FLEDx_EN or TLEDx_EN bit. The driver remains in standby until an I²C read of the LED_FLAG register is completed. Upon clearing the flags/faults, the device can be restarted.

Flash Timeout

The flash timeout period sets the amount of time that the flash current is being sourced from the current sources (LED1/2). The LED driver has 16 timeout levels ranging from 50ms to 1200ms setting by FTIMEOUT[3:0] bits and 8 ramps up/down levels from 512μs to 64ms. When flash timeout happens, the driver sets the FTIMEOUTx_FLAG and FTIMEOUTx_STAT bits to 1, and sends an INT to host if bit is not masked.

Over-Voltage Protection (OVP)

The FLASH_VDD and TORCH_VDD are the power supply input for the LED driver. When FLASH_VDD rises above 5.5V (TYP), the over-voltage comparator trips for deglitch time setting by FLASH_FLED_OVP_DEG[1:0] bits, and then turns off the internal NFET. When TORCH_VDD reaches 5.45V (TYP), the over-voltage comparator trips and turns off the internal NFET, the corresponding enable bits (TLEDx_EN and FLEDx_EN) are cleared, and the OVP flag and status bits are set.

Under-Voltage Lockout (UVLO)

The LED driver monitors the FLASH_VDD and TORCH_VDD voltage to check whether the voltage is below the UVP threshold (2.5V for the FLASH_VDD and 2V for the TORCH_VDD). When FLASH_VDD or TORCH_VDD is below the UVP, the corresponding status and flag are set to 1, and an INT will be sent to host. Moreover, the driver will not start up and stay in standby until UVP status is released.

Thermal Shutdown (TSD)

When the die temperature reaches +150℃, the thermal shutdown detection circuit trips, forcing the LED driver into standby status, TSHUT_FLAG and TSHUT_STAT bits are set to 1, and an INT will be sent to host. Upon restart, if the die temperature is still in thermal shutdown status (TSHUT_STAT = 1), the chip is in standby status.

LED Short Fault

The LED Fault flags (LEDx_SHORT_FLAG) read back a 1 if the device is active in flash or torch mode and either active LED output experiences a short condition. An LED short condition is determined if the voltage at LED1 or LED2 goes below 500mV (TYP) while the device is in torch or flash mode. There is a deglitch time of 100μs before the LED short flag is valid. The LED short flag can be reset to 0 by read the corresponding register bit. The mode enable bits are also cleared upon an LED short fault.

Miscellaneous (ADC, DPDM, PD PHY)

ADC

The SGM41620 integrates a high accuracy 10 channels 12-bit ADC converter to monitor VAC, VBUS, IBUS, IBAT (charging current through BATFET Q4), VSYS, VBAT, VBATSNS, TSBUS, TSBAT and the junction temperature. Note that the ADC operates independent of Buck charger and fast charger, and then host can use it to get the voltage, current, temperature information of the charging system. The ADC is controlled by the HK_CTRL3 register. Setting the ADC_EN bit to 1 enables the ADC, and setting the ADC_EN bit to 0 to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC operates independent of the faults, unless the host sets the ADC_EN bit to 0.

The ADC can operate if V_{VAC} > $V_{VAC\_PRESENT\_R}$ or V_{VBUS} > $V_{VBUS\_PRESENT\_R}$ or V_{BAT} > $V_{BAT\_MIN\_CP}$ condition is valid. Otherwise the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the HK_CTRL3 and ADC_FUNC_DIS registers. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

DETAILED DESCRIPTION (continued)

DPDM

The SGM41620 has multiple registers to control the DP and DM pin for special usage.

For the BC1.2 detection, the DPDM function block provides extra option for some parameters such as V_{DAT_REF} and I_{DP_SINK} for backward compatibility.

PD PHY

USB_PD

The PD function of the PD PHY complies with USB Power Delivery spec 3.0 and Type-C Port Controller Interface spec 1.0. Some “Not support” functions are listed in the register table.

Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the CC1, CC2 pins. This status information provides the host processor all of the information required to determine attach and detach status of the cable. The USB_PD has three threshold comparators matching the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device. These comparators can automatically trigger interrupts to occur when there is a state change.

Detection through Autonomous DRP Toggles

The PD PHY has the capability to do autonomous DRP toggles. In DRP toggles, the PD PHY implements DRP toggle between SRC (source) and SNK (sink). It can also present as a SRC or SNK only and monitor CC1, CC2 status.

Dead Battery Mode

PD PHY that supports being charged by USB whose VDD’s DC/DC is off shall apply Rd to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default VBUS. Circuitry to present Rd in this case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide VBUS.

VCONN

The VCONN is provided the power supply (valid range: 3.3V to 5.5V) by the external DC/DC or LDO. When host sets the EN_VCONN bit to 1 and power role is Source or DRP, PD PHY turns on the correct switch with over-current protection (value is setting by VCONN_OCP[2:0] bits) between VCONN and CC1 or CC2, finally the cables with electronics in the plug can be powered by VCONN.

CC Logic and CC_DIR

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

1. Detect attach of USB ports, e.g. a Source to a Sink
2. Resolve cable orientation and twist connections to output CC_DIR signal
3. Discover and configure VBUS: USB Type-C Current modes or USB Power Delivery
4. Configure VCONN

When SGM41620 is connected to source or sink with USB Type-C cable, CC_DIR can output the orientation by sensing the CC pin voltage. When CC line in the cable (frequently-used Type-C cable has one CC line) is connected to CC1, CC_DIR outputs low level (push-pull). When CC line in the cable is connected to CC2, CC_DIR outputs high level.

DETAILED DESCRIPTION (continued)

EDL_TSBUS

EDL_TSBUS pin has two functions:

1) Monitor the BUS temperature when configure as voltage input.

2) Reset the host when configure as voltage output.

The descriptions for the first function can be found at chapter TDIE Over-Temperature Protection, TSBUS, and TSBAT Temperature Monitoring. For the second function, the detail usages are: SGM41620 is configured to pull down CC1 & CC2 with Rd, and the adapter with Type-C debug cable is plug in. Then once CC logic circuit found the special connection (please see Table 7) with 100ms debounce, the EDL_TSBUS pin will output low/high (decided by EDL_ACTIVE_ LEVEL bit) level to reset the host. It's added that the EDL_TSBUS high level can be configure to 1.8V (by default) or 1.2V by INTERNAL_PU_BUFFER bit.

Table 7. Charging Parameter 2 Default Setting

CC1	CC2	EDL_TSBUS Status
Open	Open	HIZ
Rp	Open	HIZ
Open	Rp	HIZ
Rp-3A	Rp-1.5A	HIZ
Rp-1.5A	Rp-default	0
Rp-3A	Rp-default	0
Rp-1.5A	Rp-3A	HIZ
Rp-default	Rp-1.5A	0
Rp-default	Rp-3A	0
Rp-default	Rp-default	HIZ
Rp-1.5A	Rp-1.5A	HIZ
Rp-3A	Rp-3A	HIZ

I²C_25ms Timeout

In I²C communication, some issues happen sometimes: 1) I²C device pulls SDA forever to ground caused by ground noise or supply power noise. 2) SCL clock disappears sometimes because of host interrupt or power down. For SGM41620, I²C circuit monitors the SCL and SDA line all the time once I²C interface is alive, when the low level is kept over than 25ms for SCL or SDA, I²C circuit will return to the idle state and release the SCL & SDA line unconditionally.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

NOTE: Excepted for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.

The SGM41620 integrates multiple functional blocks, each of which has a separate address as shown in Table 8.

Table 8. Slave Address and Registers Range for I²C Interface

Slave Address (7-Bit)	Register Address (8-Bit)	Functional Block
0b1010001 (0x51)	0x00-0x29	House Keeping
	0x30-0x59	Switched Mode Buck Charger
	0x60-0x71	Switched Cap Fast Charger
	0x90-0x9A	DPDM Control
0b1010010 (0x52)	0x00-0xA5	PD PHY
0b1010011 (0x53)	0x00-0x6E	UFCS PHY
0b1010100 (0x54)	0x80-0x8C	Dual-Channel LED Control

Table 9. Register Functional List for Different Block

FUNCTION	Symbol	STAT	FLAG	MASK	THRESHOLD_ MODE SETTING	ENABLE
House Keeping						
ACDRV Enable	ACDRV_EN	--	--	--	--	0x07[5]
ACDRV Mode	ACDRV_MODE	--	--	--	0x07[4]	--
Watchdog Timer	WDT	--	0x0D[6]	0x0E[6]	0x07[2:0]	0x07[2:0]
Watchdog Timer Reset	WDT_RST	--	--	--	--	0x07[3]
Chip Register Reset	REG_RST	--	--	--	--	0x08[7]
VBUS Pull-Down Enable	VBUS_PD_EN	--	--	--	--	0x08[6]
VAC Pull-Down Enable	VAC_PD_EN	--	--	--	--	0x08[5]
PMID Pull-Down Enable	PMID_PD_EN	--	--	--	--	0x08[4]
Thermal Shutdown	TSHUT	0x0C[5]	0x0D[5]	0x0E[5]	--	0x08[1]
JEITA TSBAT HOT	TSBAT_HOT	0x0C[4]	0x0D[4]	0x0E[4]	--	0x3A[3]
JEITA TSBAT COLD	TSBAT_COLD	0x0C[3]	0x0D[3]	0x0E[3]	--	0x3A[3]
VAC OVP	VAC_OVP	0x0C[0]	0x0D[0]	0x0E[0]	0x04[6:4]	0x04[7]
VBUS OVP	VBUS_OVP	0x0C[1]	0x0D[1]	0x0E[1]	0x04[1:0]	0x04[2]
TSBAT Hot	TSBAT_HOT	0x0C[4]	0x0D[4]	0x0E[4]	--	0x3A[3]
TSBAT Cold	TSBAT_COLD	0x0C[3]	0x0D[3]	0x0E[3]	--	0x3A[3]
TSBUS Fault	TSBUS_FAULT	0x0C[2]	0x0D[2]	0x0E[2]	0x05[7:0]	0x08[0]
POR	POR	--	0x0A[6]	0x0B[6]	--	--

REGISTER MAPS (continued)

Table 9. Register Functional List for Different Block (continued)

FUNCTION	Symbol	STAT	FLAG	MASK	THRESHOLD_ MODE SETTING	ENABLE
RST0/1 System Reset	RESET	--	0x0A[5]	0x0B[5]	--	--
ADC DONE	ADC_DONE	0x09[4]	0x0A[4]	0x0B[4]	--	--
REGN OK	REGN_OK	0x09[3]	0x0A[3]	0x0B[3]	--	--
VAC Present	VAC_PRESENT	0x09[0]	0x0A[0]	0x0B[0]	--	--
VBUS Present	VBUS_PRESENT	0x09[1]	0x0A[1]	0x0B[1]	--	--
VBAT Present	VBAT_PRESENT	0x09[2]	0x0A[2]	0x0B[2]	--	--
V2X Present	V2X_PRESENT	0x09[7]	0x0A[7]	0x0B[7]	--	--
ADC Enable and Mode	ADC_CTRL	--	--	--	0x0F[6]	0x0F[7]
ADC Channel Enable	ADC_FUNC_DIS	--	--	--	--	0x0F[2:0] 0x10[6:0]
EDL Enable	EDL_TSBUS_SEL	--	--	--	--	0x27[0]
EDL Active Level	EDL_ACTIVE_LEVEL	--	--	--	0x27[1]	--
EDL Pull-Up Level	INTERNAL_PU_BUFFER	--	--	--	0x27[7]	--
Buck Charger Block						
VSYSMIN Regulation	VSYS_MIN	0x42[3]	0x45[3]	0x48[3]	0x30[2:0]	--
VBAT Regulation	VBAT_REG	0x42[7:5]	--	--	0x31[6:0]	0x31[7]
Constant Charge Current	ICHG_CC	0x42[7:5]	--	--	0x32[6:0]	0x32[6:0] = 0
VIN DPM	VINDPM	0x43[0]	0x46[0]	0x49[0]	0x33[3:0]	0x33[4]
VINDPM Track VBAT	VINDPM_VBAT	--	--	--	0x33[6:5]	--
IIN DPM	IINDPM	0x43[1]	0x46[1]	0x49[1]	0x34[5:0]	0x34[7]
Input Current Optimizer	ICO	0x43[3:2]	0x46[2]	0x49[2]	0x35[5:0]	0x35[6]
Force ICO	FORCE_ICO	--	--	--		0x35[7]
Pre-charge Current	IPRECHG	0x42[7:5]	--	--	0x36[3:0]	--
Pre-charge VBAT Threshold	VBAT_PRECHG	--	--	--	0x36[7]	--
Termination Current	ITERM	0x42[7:5]	--	--	0x37[4:0]	0x37[7]
Re-charge Enable	RECHG_DIS	--	--	--	--	0x38[4]
Re-charge Deglitch	RECHG_DEG	--	--	--	0x38[3:2]	--
Re-charge VBAT Threshold	VRECHG	--	--	--	0x38[1:0]	--
Boost Output	VBOOST	--	--	--	0x39[7:3]	--
Boost Output Current Limit	IBOOST_LIM	--	--	--	0x39[2:0]	--
TSBAT JEITA Enable	TSBAT_JEITA_EN	--	--	--	--	0x3A[3]
IBAT OCP Enable	IBAT_OCP_DIS	--	--	--	--	0x3A[2]
PMID OVP OTG Enable	VPMID_OVP_OTG_DIS	--	--	--	--	0x3A[1]
VBAT OVP Buck Enable	VBAT_OVP_BUCK_DIS	--	--	--	--	0x3A[0]
BATFET Reset System	T_BATFET_RST	--	--	--	0x3B[5]	--
nRST Pull-Down Time at BATFET Reset	T_PD_nRST	--	--	--	0x3B[4]	--
BATFET Reset Enable	BATFET_RST_EN	--	--	--	--	0x3B[3]
BATFET Turn-off Delay before Ship Mode	BATFET_DLY	--	--	--	0x3B[2]	--
BATFET Enable	BATFET_DIS	--	--	--	--	0x3B[1]
nRST Force Level in Ship Mode	nRST_DIS	--	--	--	--	0x3B[0]

REGISTER MAPS (continued)

Table 9. Register Functional List for Different Block (continued)

FUNCTION	Symbol	STAT	FLAG	MASK	THRESHOLD_ MODE SETTING	ENABLE
VBUS High Impedance Enable	HIZ_EN	--	--	--	--	0x3C[7]
RBFET ON Control	QB_ON	0x42[2]	0x45[2]	0x48[2]	--	0x3C[2]
Boost Enable	BOOST_EN	--	--	--	--	0x3C[1]
Charge Enable	CHG_EN	--	--	--	--	0x3C[0]
IBAT Discharge OCP	IBAT_OCP	0x50[1]	0x52[1]	0x54[1]	0x3D[4:3]	0x3A[2]
VSYS OVP	VSYS_OVP	0x50[3]	0x52[3]	0x54[3]	0x3D[1:0]	0x3D[2]
JEITA ISET COOL	JEITA_ISET_COOL	--	--	--	0x56[7:6]	--
JEITA VSET WARM	JEITA_VSET_WARM	--	--	--	0x57[1:0]	--
TMR2X Enable	TMR2X_EN	--	--	--	0x3F[7]	--
TDIE Regulation	TDIE_REG	0x43[6]	0x46[6]	0x49[6]	0x3F[2:1]	0x3F[3]
PFM Enable	PFM_DIS_BOOST	--	--	--	--	0x3F[0]
	PFM_DIS_BUCK	--	--	--	--	0x58[5]
Boost Frequency Setting	BOOST_FREQ	--	--	--	0x40[4:3]	--
Buck Frequency Setting	BUCK_FREQ	--	--	--	0x40[2:1]	--
System Short Protection	VSYS_SHORT	0x41[4]	0x44[4]	0x47[4]	--	--
BUCK Sleep	VSLEEP_BUCK	0x41[3]	0x44[3]	0x47[3]	--	--
Battery Depletion	VBAT_DPL	0x41[2]	0x44[2]	0x47[2]	--	--
VBAT BOOST Threshold	VBAT_LOW_BOOST	0x41[1]	0x44[1]	0x47[1]	--	--
VBUS Good	VBUS_GOOD	0x41[0]	0x44[0]	0x47[0]	--	--
Charging State	CHG_STAT	0x42[7:5]	0x45[5]	0x48[5]	--	--
Boost OK	BOOST_OK	0x42[4]	0x45[4]	0x48[4]	--	--
Battery Cool Indication	TSBAT_COOL	0x43[5]	0x46[5]	0x49[5]	0x56[3:2]	0x3A[3]
Battery Warm Indication	TSBAT_WARM	0x43[4]	0x46[4]	0x49[4]	0x56[1:0]	0x3A[3]
Converter OCP	CONV_OCP	0x50[4]	0x52[4]	0x54[4]	--	--
BUCK VBAT OVP	VBAT_OVP_BUCK	0x50[0]	0x52[0]	0x54[0]	--	0x3A[0]
HICCUP (OTG)	OTG_HICCUP	0x51[3]	0x53[3]	0x55[3]	--	--
Charger Safety Timeout	CHG_TIMEOUT	0x51[2]	0x53[2]	0x55[2]	0x3F[5:4]	0x3F[6]
PMID SHORT	VPMID_SHORT	0x51[1]	0x53[1]	0x55[1]	--	--
PMID OVP (OTG)	VPMID_OVP_OTG	0x51[0]	0x53[0]	0x55[0]	--	0x3A[1]
Charge Pump Block						
VBATSNS OVP	VBATSNS_OVP	0x69[0]	0x6B[0]	0x6D[0]	0x60[5:0]	0x60[7]
IBUS OCP	IBUS_OCP	0x69[2]	0x6B[2]	0x6D[2]	0x61[4:0]	0x65[2]
PMID2BAT OVP	PMID2BAT_OVP	0x6A[2]	0x6C[2]	0x6E[2]	0x62[2:0]	0x62[7]
PMID2BAT UVP	PMID2BAT_UVP	0x6A[1]	0x6C[1]	0x6E[1]	0x63[2:0]	0x63[7]
SS Timer	SS_TIMEOUT	--	--	--	0x65[7:5]	0x65[7:5] = 0
IBUS UCP Rising	IBUS_UCP_RISE	0x66[5]	0x67[5]	0x68[5]	--	0x65[3]
IBUS UCP Falling	IBUS_UCP_FALL	0x69[3]	0x6B[3]	0x6D[3]	--	0x65[3]
IBUS_RCP	IBUS_RCP	--	0x70[4]	0x70[3]	--	0x70[5]
CP Converter Status	SCC_SWITCHING_STAT	0x66[0]	0x67[0]	0x68[0]	--	--

REGISTER MAPS (continued)

Table 9. Register Functional List for Different Block (continued)

FUNCTION	Symbol	STAT	FLAG	MASK	THRESHOLD_ MODE SETTING	ENABLE
VBUS Error High	VBUS_ERROR_HI	0x66[2]	0x67[2]	0x68[2]	--	--
VBUS Error Low	VBUS_ERROR_LO	0x66[1]	0x67[1]	0x68[1]	--	--
CFLY Short Detection	PIN_DIAG_FAIL	0x6A[0]	0x6C[0]	0x6E[0]	--	--
VBAT Fast SCP	VBAT_SCP	--	0x71[1]	0x71[0]	--	0x71[2]
CP Converter OCP	CONV_OCP	--	0x70[1]	0x70[0]	--	0x70[2]
CP Converter RCP	CONV_RCP	--	0x70[4]	0x70[3]	--	0x70[5]
VBAT OVP	VBAT_OVP	0x69[1]	0x6B[1]	0x6D[1]	--	--
Frequency Setting	FREQ_SET	--	--	--	0x64[7:5]	--
Frequency Shift	FREQ_SHIFT	--	--	--	0x64[4:3]	--
SCC Mode	SCC_MODE	--	--	--	0x64[1]	--
SCC Enable	SCC_EN	--	--	--	--	0x64[0]
LED Block						
LED1 Flash Timeout	FTIMIEOUT1	0x88[7]	0x89[7]	0x8A[7]	0x83[3:0]	0x83[7]
LED2 Flash Timeout	FTIMIEOUT2	0x88[6]	0x89[6]	0x8A[6]	0x83[3:0]	0x83[7]
LED1 Torch Mode	LED1_TORCH	0x87[1]	--	--	--	0x80[5]
LED2 Torch Mode	LED2_TORCH	0x87[0]	--	--	--	0x80[4]
LED1 Flash Mode	LED1_FLASH	0x87[3]	--	--	--	0x80[7]
LED2 Flash Mode	LED2_FLASH	0x87[2]	--	--	--	0x80[6]
FLASH Over Torch	FLASH_OVER_TORCH	0x8C[3]	--	--	--	--
FLASH_VDD UVP	FLASH_VDD_UVP	0x8C[2]	0x8C[1]	0x8C[0]	--	--
FLASH_VDD OVP	FLASH_FLED_OVP	0x88[5]	0x89[5]	0x8A[5]	--	--
LED1 Short	LED1_SHORT	0x88[4]	0x89[4]	0x8A[4]	--	--
LED2 Short	LED2_SHORT	0x88[3]	0x89[3]	0x8A[3]	--	--
TORCH_VDD UVP	TORCH_VDD_UVP	0x88[2]	0x89[2]	0x8A[2]	--	--
TORCH_VDD OVP	TORCH_VDD_OVP	0x88[1]	0x89[1]	0x8A[1]	--	--
Low VBAT for Flash	VBAT_MIN_FLED	0x88[0]	0x89[0]	0x8A[0]	0x86[4:2]	--
Low VBAT for Flash Deglitch	VBAT_MIN_FLED_DEG	--	--	--	0x86[6:5]	--
FLASH OVP Deglitch	FLASH_FLED_OVP_DEG	--	--	--	0x86[1:0]	--
LED1 Torch Brightness	TLED1_BR_CTR	--	--	--	0x84[7:0] & 0x8C[7]	--
LED2 Torch Brightness	TLED2_BR_CTR	--	--	--	0x85[7:0] & 0x8C[7]	--
LED1 FLASH Brightness	FLED1_BR_CTR	--	--	--	0x81[6:0]	--
LED2 FLASH Brightness	FLED2_BR_CTR	--	--	--	0x82[6:0]	--
LED FLASH On/Off Ramp Time	FRPT	--	--	--	0x83[6:4]	--
LED Torch On/Off Ramp Time	TRPT	--	--	--	0x80[2:0]	--

REGISTER MAPS (continued)

Slave Address with Address 0x51

House Keeping

REG0x00: DEVICE_ID Register [Reset = 0x95]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DEVICE_ID	1001 0101	R	Device ID	N/A

REG0x01: RESERVED Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved	N/A

REG0x02: HK_GEN_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	UFCS_FLAG	0	RC	Flag Occurred in UFCS Module Event Flag Bit 0 = No flag has occurred in UFCS module 1 = Flag has occurred in UFCS module. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	Reserved	0	R	Reserved	N/A
D[3]	DPDM_FLAG	0	RC	Flag Occurred in DPDM Module Event Flag Bit 0 = No flag has occurred in DPDM module 1 = Flag has occurred in DPDM module. It generates an interrupt on nINT pin if unmasked. When the flag bits in DPDM module have been read clear, reading this bit will reset it to 0.	N/A
D[2]	LED_FLAG	0	RC	Flag Occurred in LED Module Event Flag Bit 0 = No flag has occurred in LED module 1 = Flag has occurred in LED module. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	CP_FLAG	0	RC	Flag Occurred in Charge Pump Module Event Flag Bit 0 = No flag has occurred in charge pump module 1 = Flag has occurred in charge pump module. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	BUCK_FLAG	0	RC	Flag Occurred in Buck Module Event Flag Bit 0 = No flag has occurred in Buck module 1 = Flag has occurred in Buck module. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x03: HK_GEN_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	UFCS_MASK	0	R/W	Mask Flag Occurred in UFCS Module Event Interrupt 0 = Flag occurred in UFCS module event interrupt can work (default) 1 = Mask flag occurred in UFCS module event interrupt. UFCS_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	Reserved	0	R	Reserved	N/A
D[3]	DPDM_MASK	0	R/W	Mask Flag Occurred in DPDM Module Event Interrupt 0 = Flag occurred in DPDM module event interrupt can work (default) 1 = Mask flag occurred in DPDM module event interrupt. DPDM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	LED_MASK	0	R/W	Mask Flag Occurred in LED Module Event Interrupt 0 = Flag occurred in LED module event interrupt can work (default) 1 = Mask flag occurred in LED module event interrupt. LED_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	CP_MASK	0	R/W	Mask Flag Occurred in Charge Pump Module Event Interrupt 0 = Flag occurred in charge pump module event interrupt can work (default) 1 = Mask flag occurred in charge pump module event interrupt. CP_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	BUCK_MASK	0	R/W	Mask Flag Occurred in Buck Module Event Interrupt 0 = Flag occurred in Buck module event interrupt can work (default) 1 = Mask flag occurred in Buck module event interrupt. BUCK_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x04: VAC_VBUS_OVP Register [Reset = 0x23]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC_OVP_DIS	0	R/W	VAC_OVP Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST
D[6:4]	VAC_OVP[2:0]	010	R/W	VAC Over-Voltage Protection Setting Bits. When the VAC voltage reaches the programmed threshold, OVPGATE turns off the OVPFET. 000 = 6.5V 001 = 11V 010 = 12V (default) 011 = 13V 100 = 14V 101 = 15V 110 = 16V 111 = 17V	REG_RST
D[3]	Reserved	0	R	Reserved	N/A
D[2]	VBUS_OVP_DIS	0	R/W	VBUS_OVP Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST
D[1:0]	VBUS_OVP[1:0]	11	R/W	VBUS Over-Voltage Protection Threshold Setting Bits 00 = 6V 01 = 10V 10 = 12V 11 = 14V (default)	REG_RST

REG0x05: TSBUS_FAULT Register [Reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_FAULT[7:0]	0001 0101	R/W	TSBUS Percentage Fault Threshold. When the TSBUS pin voltage goes below the programmed threshold, an INT is sent to nINT pin. Fixed offset: 0% Bit step size: 0.19531% Range: 0% (00000000) - 50% (11111111) Default: 4.1% (00010101)	REG_RST

REGISTER MAPS (continued)

REG0x06: TSBAT_FAULT Register [Reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_FAULT[7:0]	0001 0101	R/W	TSBAT Percentage Fault Threshold. When the TSBAT pin voltage goes below the programmed threshold, an INT is sent to nINT pin. Fixed offset: 0% Bit step size: 0.19531% Range: 0% (00000000) – 50% (11111111) Default: 4.1% (00010101)	REG_RST

REG0x07: HK_CTRL1 Register [Reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ACDRV_ON_DEG	0	R/W	ACDRV Turn-on Deglitch Time Setting Bit in Auto Mode 0 = 20ms (default) 1 = 120ms	REG_RST WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	ACDRV_EN	0	R/W	ACDRV Control Bit. Only effect when ACDRV_MANUAL_EN = 1. 0 = Disable OVPGATE (default) 1 = Enable OVPGATE	REG_RST WDT_RST
D[4]	ACDRV_MANUAL_EN	0	R/W	0 = Auto-mode (default) 1 = Manual-mode	
D[3]	WD_TIMER_RST	0	R/WC	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset watchdog timer (Return to 0 after timer reset)	
D[2:0]	WD_TIMEOUT[2:0]	101	R/W	I²C Watchdog Timer Setting Bits 000 = Disable watchdog timer 001 = 0.5s 010 = 1s 011 = 2s 100 = 20s 101 = 40s (default) 110 = 80s 111 = 160s	

REG0x08: HK_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset Bit 0 = Keep current register setting (default) 1 = Reset to default register value and reset safety timer	REG_RST WDT_RST
D[6]	VBUS_PD_EN	0	R/W	VBUS Pull-Down Current Enable Bit When this bit is enabled, it pulls down the VBUS with 100mA. 0 = Disable (default) 1 = Enable	REG_RST
D[5]	VAC_PD_EN	0	R/W	VAC Pull-Down Current Enable Bit When the bit is enabled, pull down VAC with 50mA for 400ms and return to 0 automatically. 0 = Disable (default) 1 = Enable	REG_RST
D[4]	PMID_PD_EN	0	R/W	PMID_CP Pull-Down Resistor Enable Bit 0 = Disable PMID pull-down resistor (default) 1 = Enable PMID pull-down resistor	REG_RST
D[3:2]	Reserved	00	R	Reserved	N/A
D[1]	TSHUT_DIS	0	R/W	TSHUT Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST WDT_RST
D[0]	TSBUS_TSBAT_FLT_EN	0	R/W	TSBUS and TSBAT Fault Protection Enable Bit 0 = Disable the TSBUS and TSBAT fault protection (default) 1 = Enable the TSBUS and TSBAT fault protection	

REGISTER MAPS (continued)

REG0x09: HK_INT_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_PRESENT_STAT	0	R	V2X Present Status Bit 0 = The V2X voltage is lower than V2X_PRESENT falling threshold 1 = The V2X voltage is higher than V2X_PRESENT rising threshold	N/A
D[6:5]	Reserved	00	R	Reserved	N/A
D[4]	ADC_DONE_STAT	0	R	ADC Done Event Status Bit Indicates the ADC conversion is completed in 1-shot mode only	N/A
D[3]	REGN_OK_STAT	0	R	REGN_OK Status Bit 0 = The REGN voltage is lower than VREGN_OK falling threshold (2.8V TYP) 1 = The REGN voltage is higher than VREGN_OK rising threshold (3V TYP)	N/A
D[2]	VBAT_PRESENT_STAT	0	R	VBAT Present Status Bit 0 = The VBAT voltage is lower than VBAT_PRESENT falling threshold 1 = The VBAT voltage is higher than VBAT_PRESENT rising threshold	N/A
D[1]	VBUS_PRESENT_STAT	0	R	VBUS Present Status Bit 0 = The VBUS voltage is lower than VBUS_PRESENT falling threshold 1 = The VBUS voltage is higher than VBUS_PRESENT rising threshold	N/A
D[0]	VAC_PRESENT_STAT	0	R	VAC Present Status Bit 0 = The VAC voltage is lower than VAC_PRESENT falling threshold 1 = The VAC voltage is higher than VAC_PRESENT rising threshold	N/A

REGISTER MAPS (continued)

REG0x0A: HK_INT_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_PRESENT_FLAG	0	RC	V2X Present Event Flag Bit 0 = No V2X present event 1 = V2X present event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	POR_FLAG	0	RC	Power-On Reset Event Flag Bit 0 = No power-on reset event 1 = Power-on reset event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	RESET_FLAG	0	RC	RST0/RST1 Reset Event Flag Bit 0 = No reset event 1 = Reset event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	ADC_DONE_FLAG	0	RC	ADC Conversion Complete Event Flag Bit In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = ADC conversion is not complete in 1-shot conversion mode 1 = ADC conversion complete in 1-shot conversion mode. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	REGN_OK_FLAG	0	RC	REGN OK Event Flag Bit 0 = No REGN OK event 1 = REGN OK event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	VBAT_PRESENT_FLAG	0	RC	VBAT Present Status Change Event Flag Bit 0 = No VBAT present status change event 1 = VBAT present status change event has occurred when VBAT_PRESENT_STAT bit changes. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBUS_PRESENT_FLAG	0	RC	VBUS Present Status Change Event Flag Bit 0 = No VBUS present status change event 1 = VBUS present status change event has occurred when VBUS_PRESENT_STAT bit changes. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VAC_PRESENT_FLAG	0	RC	VAC Present Event Flag Bit 0 = No VAC present event 1 = VAC present event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x0B: HK_INT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	V2X_PRESENT_MASK	0	R/W	Mask V2X Present Event Interrupt 0 = V2X present event interrupt can work (default) 1 = Mask V2X present event interrupt. V2X_PRESENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	POR_MASK	0	R/W	Mask Power-On Reset Event Interrupt 0 = Power-on reset event interrupt can work (default) 1 = Mask power-on reset event interrupt. POR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	RESET_MASK	0	R/W	Mask Reset Event Interrupt 0 = Reset event interrupt can work (default) 1 = Mask reset event interrupt. RESET_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	ADC_DONE_MASK	0	R/W	Mask ADC Complete Event Interrupt 0 = ADC complete event interrupt can work (default) 1 = Mask ADC complete event interrupt. ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	REGN_OK_MASK	0	R/W	Mask REGN OK Event Interrupt 0 = REGN OK event interrupt can work (default) 1 = Mask REGN OK event interrupt. REGN_OK_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	VBAT_PRESENT_MASK	0	R/W	Mask VBAT Present Event Interrupt 0 = VBAT present event interrupt can work (default) 1 = Mask VBAT present event interrupt. VBAT_PRESENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VBUS_PRESENT_MASK	0	R/W	Mask VBUS Present Event Interrupt 0 = VBUS present event interrupt can work (default) 1 = Mask VBUS present event interrupt. VBUS_PRESENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VAC_PRESENT_MASK	0	R/W	Mask VAC Present Event Interrupt 0 = VAC present event interrupt can work (default) 1 = Mask VAC present event interrupt. VAC_PRESENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x0C: HK_FLT_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	TSHUT_STAT	0	R	Thermal Shutdown Fault Status Bit 0 = Normal 1 = Device is in TSHUT status	N/A
D[4]	TSBAT_HOT_STAT	0	R	TSBAT_HOT Fault Status Bit 0 = Normal 1 = Device is in TSBAT_HOT status (> T4)	N/A
D[3]	TSBAT_COLD_STAT	0	R	TSBAT_COLD Fault Status Bit 0 = Normal 1 = Device is in TSBAT_COLD status (< T1)	N/A
D[2]	TSBUS_FLT_STAT	0	R	TSBUS Fault Status Bit 0 = Normal 1 = Device is in TSBUS_FLT status	N/A
D[1]	VBUS_OVP_STAT	0	R	VBUS_OVP Fault Status Bit 0 = Normal 1 = Device is in VBUS_OVP status	N/A
D[0]	VAC_OVP_STAT	0	R	VAC_OVP Fault Status Bit 0 = Normal 1 = Device is in VAC_OVP status	N/A

REGISTER MAPS (continued)

REG0x0D: HK_FLT_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	WD_TIMEOUT_FLAG	0	RC	Watchdog Timeout Fault Flag Bit 0 = No watchdog timeout fault 1 = Watchdog timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	TSHUT_FLAG	0	RC	Thermal Shutdown Fault Flag Bit 0 = No thermal shutdown fault 1 = Thermal shutdown has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	TSBAT_HOT_FLAG	0	RC	TSBAT_HOT Fault Flag Bit 0 = No TSBAT_HOT fault 1 = TSBAT_HOT fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	TSBAT_COLD_FLAG	0	RC	TSBAT_COLD Fault Flag Bit 0 = No TSBAT_COLD fault 1 = TSBAT_COLD fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	TSBUS_FLT_FLAG	0	RC	TSBUS Fault Flag Bit 0 = No TSBUS fault 1 = TSBUS fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBUS_OVP_FLAG	0	RC	VBUS OVP Fault Flag Bit 0 = No VBUS OVP fault 1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VAC_OVP_FLAG	0	RC	VAC OVP Fault Flag Bit 0 = No VAC OVP fault 1 = VAC OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x0E: HK_FLT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	WD_TIMEOUT_MASK	0	R/W	Mask Watchdog Timeout Fault Interrupt 0 = Watchdog timeout fault interrupt can work (default) 1 = Mask watchdog timeout fault interrupt. WD_TIMEOUT_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	TSHUT_MASK	0	R/W	Mask Thermal Shutdown Fault Interrupt 0 = Thermal shutdown fault interrupt can work (default) 1 = Mask thermal shutdown fault interrupt. TSHUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	TSBAT_HOT_MASK	0	R/W	Mask TSBAT_HOT Fault Interrupt 0 = TSBAT_HOT fault interrupt can work (default) 1 = Mask TSBAT_HOT fault interrupt. TSBAT_HOT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	TSBAT_COLD_MASK	0	R/W	Mask TSBAT_COLD Fault Interrupt 0 = TSBAT_COLD fault interrupt can work (default) 1 = Mask TSBAT_COLD fault interrupt. TSBAT_COLD_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	TSBUS_FLT_MASK	0	R/W	Mask TSBUS Fault Interrupt 0 = TSBUS fault interrupt can work (default) 1 = Mask TSBUS fault interrupt. TSBUS_FLT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VBUS_OVP_MASK	0	R/W	Mask VBUS OVP Fault Interrupt 0 = VBUS OVP fault interrupt can work (default) 1 = Mask VBUS OVP fault interrupt. VBUS_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VAC_OVP_MASK	0	R/W	Mask VAC OVP Fault Interrupt 0 = VAC OVP fault interrupt can work (default) 1 = Mask VAC OVP fault interrupt. VAC_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x0F: HK_CTRL3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	Enable ADC 0 = Disabled 1 = Enabled	REG_RST WDT_RST
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control Bit 0 = Continuous conversion 1 = One-shot	REG_RST
D[5:3]	Reserved	000	R	Reserved	N/A
D[2]	IBUS_ADC_DIS	0	R/W	0 = Enable Conversion (default) 1 = Disable Conversion	REG_RST
D[1]	VBUS_ADC_DIS	0	R/W		REG_RST
D[0]	VAC_ADC_DIS	0	R/W		REG_RST

REGISTER MAPS (continued)

REG0x10: ADC_FUNC_DIS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	VBATSNS_ADC_DIS	0	R/W	0 = Enable Conversion (default) 1 = Disable Conversion	REG_RST
D[5]	VBAT_ADC_DIS	0	R/W		
D[4]	IBAT_ADC_DIS	0	R/W		
D[3]	VSYS_ADC_DIS	0	R/W		
D[2]	TSBUS_ADC_DIS	0	R/W		
D[1]	TSBAT_ADC_DIS	0	R/W		
D[0]	TDIE_ADC_DIS	0	R/W		

REG0x11: IBUS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBUS_ADC[11:8]	0000	R	High Byte of the ADC IBUS Data D[3:0]: 5120mA, 2560mA, 1280mA, 640mA	N/A

REG0x12: IBUS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	0000 0000	R	Low Byte of the ADC IBUS Data D[7:0]: 320mA, 160mA, 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA	N/A

REG0x13: VBUS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBUS_ADC[11:8]	0000	R	High Byte of the ADC VBUS Data D[3:0]: 7680mV, 3840mV, 1920mV, 960mV	N/A

REG0x14: VBUS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	0000 0000	R	Low Byte of the ADC VBUS Data D[7:0]: 480mV, 240mV, 120mV, 60mV, 30mV, 15mV, 7.5mV, 3.75mV	N/A

REG0x15: VAC_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VAC_ADC[11:8]	0000	R	High Byte of the ADC VAC Data D[3:0]: 10240mV, 5120mV, 2560mV, 1280mV	N/A

REG0x16: VAC_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC_ADC[7:0]	0000 0000	R	Low Byte of the ADC VAC Data D[7:0]: 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV, 5mV	N/A

REGISTER MAPS (continued)

REG0x17: VBATSNS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBATSNS_ADC[11:8]	0000	R	High Byte of the ADC VBATSNS Data D[3:0]: 2560mV, 1280mV, 640mV, 320mV	N/A

REG0x18: VBATSNS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBATSNS_ADC[7:0]	0000 0000	R	Low Byte of the ADC VBATSNS Data D[7:0]: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	N/A

REG0x19: VBAT_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT_ADC[11:8]	0000	R	High Byte of the ADC VBAT Data D[3:0]: 2560mV, 1280mV, 640mV, 320mV	N/A

REG0x1A: VBAT_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	0000 0000	R	Low Byte of the ADC VBAT Data D[7:0]: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	N/A

REG0x1B: IBAT_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBAT_ADC[11:8]	0000	R	High Byte of the ADC IBAT Data D[3:0]: 2560mA, 1280mA, 640mA, 320mA	N/A

REG0x1C: IBAT_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	0000 0000	R	Low Byte of the ADC IBAT Data D[7:0]: 160mA, 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA, 1.25mA	N/A

REG0x1D: VSYS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VSYS_ADC[11:8]	0000	R	High Byte of the ADC VSYS Data D[3:0]: 2560mV, 1280mV, 640mV, 320mV	N/A

REG0x1E: VSYS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VSYS_ADC[7:0]	0000 0000	R	Low Byte of the ADC VSYS Data D[7:0]: 160mV, 80mV, 40mV, 20mV, 10mV, 5mV, 2.5mV, 1.25mV	N/A

REGISTER MAPS (continued)

REG0x1F: TSBUS_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1:0]	TSBUS_ADC[9:8]	00	R	High Byte of the ADC TSBUS Data TSBUS Pin Voltage as a Percentage of REGN D[1:0]: 50%, 25%	N/A

REG0x20: TSBUS_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_ADC[7:0]	0000 0000	R	Low Byte of the ADC TSBUS Data TSBUS Pin Voltage as a Percentage of REGN D[7:0]: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%	N/A

REG0x21: TSBAT_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1:0]	TSBAT_ADC[9:8]	00	R	High Byte of the ADC TSBAT Data TSBAT Pin Voltage as a Percentage of REGN D[1:0]: 50%, 25%	N/A

REG0x22: TSBAT_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_ADC[7:0]	0000 0000	R	Low Byte of the ADC TSBAT Data TSBAT Pin Voltage as a Percentage of REGN D[7:0]: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%	N/A

REG0x23: TDIE_ADC1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000 000	R	Reserved	N/A
D[0]	TDIE_ADC[8]	0	R	High Byte of the ADC TDIE Data DIE Temperature = TDIE_ADC[8:0] × 0.5℃ D[0]: 128℃	N/A

REG0x24: TDIE_ADC0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	0000 0000	R	Low Byte of the ADC TDIE Data D[7:0]: 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃, 0.5℃	N/A

REGISTER MAPS (continued)

REG0x27: EDL_BUFFER Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	INTERNAL_PU_BUFFER	0	R/W	Internal Pull-Up Buffer Voltage for EDL and CC_DIR 0 = 1.2V (default) 1 = 1.8V	REG_RST WDT_RST
D[6:2]	Reserved	0 0000	R	Reserved	N/A
D[1]	EDL_ACTIVE_LEVEL	1	R/W	Setting Bit for the EDL Pull High or Low to indicate Active Status 0 = Active high 1 = Active low (default)	N/A
D[0]	EDL_TSBUS_SEL	0	R/W	EDL_TSBUS Pin Function Setting Bit 0 = EDL_TSBUS Pin works as EDL output function (default) 1 = EDL_TSBUS Pin works as TSBUS ADC input function	REG_RST

REG0x28: MISC_CTRL1 Register [Reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	I2C_25ms_TMO_DIS	0	R/W	I²C Bus 25ms Timeout Disable Bit 0 = Enabled (default) 1 = Disabled	N/A
D[4:3]	Reserved	01	R	Reserved	N/A
D[2]	TSBAT_FLT_STAT	0	R	TSBAT_FLT Fault Status Bit 0 = Normal 1 = Device is in TSBAT_FLT status	N/A
D[1]	TSBAT_FLT_FLAG	0	RC	TSBAT Fault Flag Bit 0 = No TSBAT fault 1 = TSBAT fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	TSBAT_FLT_MASK	0	R/W	Mask TSBAT Fault Interrupt 0 = TSBAT fault interrupt can work (default) 1 = Mask TSBAT fault interrupt. TSBAT_FLT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x29: RESERVED Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved	N/A

REGISTER MAPS (continued)

Switched Mode Buck Charger

REG0x30: VSYS_MIN Register [Reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2:0]	VSYS_MIN[2:0]	101	R/W	Minimum System Voltage 000 = 2.6V 001 = 2.8V 010 = 3V 011 = 3.2V 100 = 3.4V 101 = 3.5V (default) 110 = 3.6V 111 = 3.7V	REG_RST

REG0x31: VBAT_REG Register [Reset = 0x2E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATSNS_EN	0	R/W	BATP/BATN Sense Enable 0 = Disable BATP/BATN sense (default) 1 = Enable BATP/BATN sense Select either BATP/BATN pin or BAT pin to regulate battery voltage.	REG_RST WDT_RST
D[6:0]	VBAT_REG[6:0]	010 1110	R/W	Constant Charge Voltage Limit Fixed offset: 3.84V Bit step size: 8mV Range: 3.84V (0000000) – 4.856V (1111111) Default: 4.208V (0101110)	REG_RST WDT_RST

REG0x32: ICHG_CC Register [Reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:0]	ICHG_CC[6:0]	010 1000	R/W	Fast Charge Current Limit Fixed offset: 0mA Bit step size: 50mA Range: 0mA (0000000) – 4000mA (1010000 ~ 1111111) Default: 2000mA (0101000) NOTE: ICHG_CC[6:0] = 0000000 (0mA) disables charge	REG_RST WDT_RST

REG0x33: VINDPM Register [Reset = 0x65]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:5]	VINDPM_VBAT[1:0]	11	R/W	Dynamic VINDPM Tracking Setting Bits 00 = 150mV 01 = 200mV 10 = 250mV 11 = Disable (default) Sets V_{INDPM} to track BAT voltage control bit (Reset to default value after VBUS plug-in.). Actual V_{INDPM} is the higher of VINDPM[3:0] value and V_{BAT} + VINDPM_VBAT[1:0] value.	REG_RST Rising edge of VBUS_PRESENT_FLAG
D[4]	VINDPM_DIS	0	R/W	VINDPM Function Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[3:0]	VINDPM[3:0]	0101	R/W	Absolute VINDPM Threshold Setting Bits Fixed offset: 4V Range: 4V (0000) – 4.8V (1000) ~100mV/step, 7.6V (1001), 8.2V (1010), 8.4V (1011), 8.6V (1100), 10V (1101), 10.5V (1110), 10.7V (1111) Default: 4.5V (0101)	REG_RST

REGISTER MAPS (continued)

REG0x34: IINDPM Register [Reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IINDPM_DIS	0	R/W	IINDPM Function Disable 0 = Enable (default) 1 = Disable	REG_RST WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5:0]	IINDPM[5:0]	00 1000	R/W	Input Current Limit Fixed offset: 100mA Bit step size: 50mA Range: 100mA (000000) – 3.25A (111111) Default: 001000 (500mA) IINDPM[5:0] bits are changed automatically after input source type detection is completed USB Host SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2A/2.1A/2.4A	REG_RST

REG0x35: ICO_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_ICO	0	R/WC	Force Start Input Current Optimizer (ICO) 0 = Do not force ICO (default) 1 = Force ICO This bit returns to 0 after ICO starts	REG_RST WDT_RST
D[6]	ICO_EN	0	R/W	Input Current Optimizer (ICO) Enable 0 = Disable ICO Algorithm (default) 1 = Enable ICO Algorithm	REG_RST
D[5:0]	IINDPM_ICO[5:0]	00 0000	R	Input Current Limit in Effect while Input Current Optimizer (ICO) is enabled Fixed offset: 100mA (default) Bit step size: 50mA Range: 100mA (000000) – 3.25A (111111)	N/A

REG0x36: PRECHARGE_CTRL Register [Reset = 0x82]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_PRECHG	1	R/W	Battery Precharge to Fast Charge Threshold 0 = 2.7V 1 = 3.0V (default)	REG_RST WDT_RST
D[6:4]	Reserved	000	R	Reserved	N/A
D[3:0]	IPRECHG[3:0]	0010	R/W	Precharge Current Limit Fixed offset: 50mA Bit step size: 50mA Range: 50mA (0000) – 800mA (1111) Default: 150mA (0010)	REG_RST WDT_RST

REG0x37: TERMINATION_CTRL Register [Reset = 0x82]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TERM_EN	1	R/W	Charging Termination Enable 0 = Disable 1 = Enable (default)	REG_RST WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	TERM_DEG	0	R/W	Charging Termination Deglitch Time Setting 0 = 256ms (default) 1 = 48ms	REG_RST WDT_RST
D[4:0]	ITERM[4:0]	0 0010	R/W	Termination Current Limit Fixed offset: 100mA Bit step size: 50mA Range: 100mA (00000) – 1650mA (11111) Default: 200mA (00010)	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x38: RECHARGE_CTRL Register [Reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	RECHG_DIS	0	R/W	Recharging Function Disable 0 = Enable (default) 1 = Disable	REG_RST WDT_RST
D[3:2]	RECHG_DEG[1:0]	10	R/W	Recharging Deglitch Time Setting 00 = 64ms 01 = 256ms 10 = 1024ms (default) 11 = 2048ms	REG_RST WDT_RST
D[1:0]	VRECHG[1:0]	00	R/W	Battery Recharge Threshold Offset (below Charge Voltage Limit) 00 = 100mV (V_{RECHG}) below VBAT_REG (default) 01 = 200mV (V_{RECHG}) below VBAT_REG 10 = 300mV (V_{RECHG}) below VBAT_REG 11 = 400mV (V_{RECHG}) below VBAT_REG	REG_RST WDT_RST

REG0x39: VBOOST_CTRL Register [Reset = 0x53]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	VBOOST[4:0]	01010	R/W	Boost Mode Regulation Voltage Fixed offset: 3.9V Bit step size: 100mV Range: 3.9V - 5.7V (00000 ~ 10010), 5.8V (10011 ~ 11111) Default: 4.9V (01010)	REG_RST
D[2:0]	IBOOST_LIM[2:0]	011	R/W	Boost Output Current Limit through RBFET 000 = 0.5A 001 = 0.9A 010 = 1.3A 011 = 1.5A (default) 100 = 2.1A 101 = 2.5A 110 = 2.9A 111 = 3.25A	REG_RST WDT_RST

REG0x3A: PROTECTION_DIS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CONV_OCP_DIS	0	R/W	Buck/Boost Converter OCP Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST WDT_RST
D[3]	TSBAT_JEITA_EN	0	R/W	TSBAT_JEITA Protection Enable Bit, including COLD, COOL, WARM and HOT 0 = Disable protection (default) 1 = Enable protection	REG_RST WDT_RST
D[2]	IBAT_OCP_DIS	0	R/W	IBAT_OCP Protection Disable Bit 0 = Enable IBAT_OCP protection (default) 1 = Disable IBAT_OCP protection	REG_RST WDT_RST
D[1]	VPMID_OVP_OTG_DIS	0	R/W	VPMID_OVP_OTG Protection Disable Bit 0 = Enable VPMID_OVP_OTG protection (default) 1 = Disable VPMID_OVP_OTG protection	REG_RST WDT_RST
D[0]	VBAT_OVP_BUCK_DIS	0	R/W	VBAT_OVP_BUCK Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x3B: RESET_CTRL Register [Reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	T_BATFET_RST	0	R/W	BATFET Turn-Off Time during Reset Function 0 = 200ms (default) 1 = 700ms	N/A
D[4]	T_PD_nRST	0	R/W	nRST Pull-Down Time during Reset Function 0 = 100ms (default) 1 = No pull-down	N/A
D[3]	BATFET_RST_EN	1	R/W	BATFET Reset Function Enable Bit 0 = Disable BATFET reset function 1 = Enable BATFET reset function (default)	REG_RST
D[2]	BATFET_DLY	1	R/W	BATFET Turn-Off Delay Control Bit 0 = Turn off BATFET immediately when BATFET_DIS bit is set to 1. 1 = Turn off BATFET after t_{SM_DLY} (20s TYP) when BATFET_DIS bit is set 1. (default)	REG_RST
D[1]	BATFET_DIS	0	R/W	Force BATFET Off to Enable Ship Mode 0 = Allow BATFET turn on (default) 1 = Turn off BATFET	REG_RST
D[0]	nRST_DIS	0	R/W	Force nRST to Pull Low for Ship Mode 0 = Pull low for ship mode (default) 1 = nRST no reaction for ship mode Register bit is reset to default value when input source is plugged-in.	REG_RST

REG0x3C: CHG_CTRL1 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	HIZ_EN	0	R/W	HIZ Mode Enable Configuration 0 = Disable HIZ mode (default) 1 = Enable HIZ mode The bit is reset to default value when input source is plugged-in.	REG_RST WDT_RST
D[6]	PERFORMANCE_EN	0	R/W	Performance-Mode Enable Configuration 0 = Disable Performance-Mode (default) 1 = Enable Performance-Mode When Enterprise needs to enter into charge-pump fast charging, AP should set PERFORMANCE_EN = 1 and DIS_BUCKCHG_PATH = 1, then set SCC_EN = 1. Register bit is reset to default value when input source is plugged-in.	REG_RST WDT_RST
D[5]	DIS_BUCKCHG_PATH	0	R/W	Disable Buck Charging Operation (disable the PWM and keep battery in discharge status, VBUS present and POWER good are present, BC1.2 is present) 0 = No action (default) 1 = Stop the PWM and turn on BATFET Register bit is reset to default value when input source is plugged-in	REG_RST WDT_RST
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	QB_EN	0	R/W	QB ON/OFF Control Bit 0 = QB OFF (default) 1 = QB ON This bit is only valid in Boost mode.	REG_RST WDT_RST
D[1]	BOOST_EN	0	R/W	Boost Mode Configuration 0 = Boost Mode Disable (default) 1 = Boost Mode Enable	REG_RST WDT_RST
D[0]	CHG_EN	1	R/W	Charge Enable Configuration 0 = Charge Disable 1 = Charge Enable (default)	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x3D: CHG_CTRL2 Register [Reset = 0x09]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VBAT_TRACK	0	R/W	VBAT Tracking Voltage for SYS Regulation (V_{BAT_TRACK}) I_{SYS} = 0A, V_{BAT} > V_{SYSMIN} and Charging Disable. V_{SYS_REG} = V_{BAT} + V_{BAT_TRACK} 0 = 60mV (default) 1 = 240mV	REG_RST WDT_RST
D[4:3]	IBATOCP[1:0]	01	R/W	System Over-Current Protection Threshold to Turn Off BATFET 00 = 10A 01 = 12A (default) 10 = 14A 11 = 16A	REG_RST WDT_RST
D[2]	VSYSOVP_DIS	0	R/W	VSYS_OVP Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST WDT_RST
D[1:0]	VSYSOVP_TH[1:0]	01	R/W	VSYS_OVP Threshold Setting, over System Regulation Target 00 = 104% 01 = 106% (default) 10 = 108% 11 = 110%	REG_RST WDT_RST

REG0x3E: RESERVED Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0010	R	Reserved	N/A

REG0x3F: CHG_CTRL4 Register [Reset = 0xE6]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TMR2X_EN	1	R/W	Safety Timer Setting during DPM or Thermal Regulation 0 = Safety timer not slowed by 2X during input DPM or thermal regulation or JEITA COOL 1 = Safety timer slowed by 2X during input DPM or thermal regulation or JEITA (default)	REG_RST WDT_RST
D[6]	CHG_TIMER_EN	1	R/W	Charging Safety Timer Enable 0 = Disable 1 = Enable (default)	REG_RST WDT_RST
D[5:4]	CHG_TIMER[1:0]	10	R/W	Fast Charge Timer Setting 00 = 5hrs 01 = 8.8hrs 10 = 13hrs (default) 11 = 25hrs	REG_RST WDT_RST
D[3]	TDIE_REG_DIS	0	R/W	Die Thermal Regulation Loop Disable Bit 0 = Enable die thermal loop (default) 1 = Disable die thermal loop	REG_RST WDT_RST
D[2:1]	TDIE_REG[1:0]	11	R/W	Die Thermal Regulation Threshold 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)	REG_RST WDT_RST
D[0]	PFM_DIS_BOOST	0	R/W	PFM Disable in Boost Mode 0 = Enable PFM (default) 1 = Disable PFM	REG_RST

REGISTER MAPS (continued)

REG0x40: CHG_CTRL5 Register [Reset = 0x94]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	100	R	Reserved	N/A
D[4:3]	BOOST_FREQ[1:0]	10	R/W	Boost Mode Frequency Selection 00 = 500kHz 01 = 1MHz 10 = 1.5MHz (default) 11 = 2MHz	REG_RST WDT_RST
D[2:1]	BUCK_FREQ[1:0]	10	R/W	Buck Mode Frequency Selection 00 = 500kHz 01 = 1MHz 10 = 1.5MHz (default) 11 = 2MHz	REG_RST WDT_RST
D[0]	BAT_LOAD_EN	0	R/WC	Battery load(10mA/10ms) Enable Bit (Return to 0 after pull down 10mA for 10ms): 0 = Disable (default) 1 = Enable	N/A

REG0x41: CHG_INT_STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	VSYS_SHORT_STAT	0	R	VSYS Short Status Bit 0 = The VSYS voltage is higher than VSYS_SHORT rising threshold 1 = The VSYS voltage is lower than VSYS_SHORT falling threshold	N/A
D[3]	VSLEEP_BUCK_STAT	0	R	Buck Sleep Mode Status Bit 0 = The VBUS-VBAT voltage is higher than VSLEEP_BUCK rising threshold 1 = The VBUS-VBAT voltage is lower than VSLEEP_BUCK falling threshold	N/A
D[2]	VBAT_DPL_STAT	0	R	Battery Depletion Status Bit 0 = The VBAT voltage is higher than VBAT_DPL rising threshold 1 = The VBAT voltage is lower than VBAT_DPL falling threshold	N/A
D[1]	VBAT_LOW_BOOST_STAT	0	R	Battery Voltage Exiting Boost Mode Status Bit 0 = The VBAT voltage is higher than VBAT_LOW_BOOST rising threshold 1 = The VBAT voltage is lower than VBAT_LOW_BOOST falling threshold	N/A
D[0]	VBUS_GOOD_STAT	0	R	Poor Source Detection Status Bit 0 = VBUS does not pass poor source detection 1 = VBUS passes poor source detection	N/A

REGISTER MAPS (continued)

REG0x42: CHG_INT_STAT2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	CHG_STAT[2:0]	000	R	Charging Status: 000 = Not charging 001 = Trickle charging 010 = Pre-charging 011 = Fast charging (CC mode) 100 = Fast charging (CV mode) 101 = Charge Termination 110 - 111 = Reserved	N/A
D[4]	BOOST_OK_STAT	0	R	BOOST Operation Status 0 = BOOST is not ready 1 = BOOST is ready	N/A
D[3]	VSYSMIN_REG_STAT	0	R	VSYS Regulation Status (Forward Mode) 0 = Not in VSYSMIN regulation (BAT > VSYSMin) 1 = In VSYSMIN regulation (BAT < VSYSMin)	N/A
D[2]	QB_ON_STAT	0	R	QB ON/OFF Status 0 = QB is OFF 1 = QB is ON	N/A
D[1:0]	BATFET_STAT[1:0]	00	R	BATFET Status 00 = BATFET is not in supplement mode 01 = BATFET is in supplement mode	N/A

REG0x43: CHG_INT_STAT3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TDIE_REG_STAT	0	R	IC Thermal Regulation Status 0 = Normal 1 = Device in thermal regulation status	N/A
D[5]	TSBAT_COOL_STAT	0	R	TSBAT Temperature in Cool Range Status (between T1 and T2) 0 = TSBAT status is not in cool range 1 = TSBAT status is in cool range	N/A
D[4]	TSBAT_WARM_STAT	0	R	TSBAT Temperature in Warm Range Status (between T3 and T4) 0 = TSBAT status is not in warm range 1 = TSBAT status is in warm range	N/A
D[3:2]	ICO_STAT[1:0]	00	R	Input Current Optimizer Status 00 = ICO disabled 01 = ICO optimization in progress 10 = Maximum input current detected 11 = Reserved	N/A
D[1]	IINDPM_STAT	0	R	IINDPM Status 0 = Not in IINDPM 1 = IINDPM	N/A
D[0]	VINDPM_STAT	0	R	VINDPM Status 0 = Not in VINDPM 1 = VINDPM	N/A

REGISTER MAPS (continued)

REG0x44: CHG_INT_FLAG1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	VSYS_SHORT_FLAG	0	RC	VSYS Short Fault Flag Bit 0 = No VSYS short fault 1 = VSYS short fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	VSLEEP_BUCK_FLAG	0	RC	VSLEEP_BUCK Event Flag Bit 0 = No VSLEEP_BUCK event 1 = VSLEEP_BUCK event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	VBAT_DPL_FLAG	0	RC	VBAT Depletion Event Flag Bit 0 = No VBAT depletion event 1 = VBAT depletion event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBAT_LOW_BOOST_FLAG	0	RC	VBAT_LOW_BOOST Event Flag Bit 0 = No VBAT_LOW_BOOST event 1 = VBAT_LOW_BOOST event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VBUS_GOOD_FLAG	0	RC	VBUS_GOOD_STAT Change Event Flag Bit 0 = No VBUS_GOOD_STAT change event 1 = VBUS_GOOD_STAT change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x45: CHG_INT_FLAG2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	CHG_FLAG	0	RC	Charging Status Change Event Flag Bit 0 = No charging status change event 1 = Charging status change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	BOOST_OK_FLAG	0	RC	BOOST Operation Event Flag Bit 0 = No BOOST operation event 1 = BOOST operation event has occurred, or the BOOST_OK status bit is reset from ‘1’ to ‘0’ when the device exits Boost mode. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	VSYSMIN_REG_FLAG	0	RC	VSYSMIN Regulation Event Flag Bit 0 = No VSYSMIN regulation event 1 = VSYSMIN regulation event has occurred, or the VSYSMIN_REG status bit is reset from ‘1’ to ‘0’ when the device exits VSYSMIN regulation state. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	QB_ON_FLAG	0	RC	QB_ON Event Flag Bit 0 = No QB_ON event 1 = QB_ON event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x46: CHG_INT_FLAG3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TDIE_REG_FLAG	0	RC	Thermal Regulation Event Flag Bit 0 = No thermal regulation event 1 = Thermal regulation event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	TSBAT_COOL_FLAG	0	RC	TSBAT_COOL Event Flag Bit 0 = No TSBAT_COOL event 1 = TSBAT_COOL event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	TSBAT_WARM_FLAG	0	RC	TSBAT_WARM Event Flag Bit 0 = No TSBAT_WARM event 1 = TSBAT_WARM event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2]	ICO_FLAG	0	RC	ICO Status Change Event Flag Bit 0 = No ICO status change event 1 = ICO status change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	IINDPM_FLAG	0	RC	IINDPM Event Flag Bit 0 = No IINDPM event 1 = IINDPM event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VINDPM_FLAG	0	RC	VINDPM Event Flag Bit 0 = No VINDPM event 1 = VINDPM event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x47: CHG_INT_MASK1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	VSYS_SHORT_MASK	0	R/W	Mask VSYS Short Fault Interrupt 0 = VSYS short fault interrupt can work (default) 1 = Mask VSYS short fault interrupt. VSYS_SHORT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	VSLEEP_BUCK_MASK	0	R/W	Mask VSLEEP_BUCK Event Interrupt 0 = VSLEEP_BUCK event interrupt can work (default) 1 = Mask VSLEEP_BUCK event interrupt. VSLEEP_BUCK_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	VBAT_DPL_MASK	0	R/W	Mask VBAT Depletion Event Interrupt 0 = VBAT depletion event interrupt can work (default) 1 = Mask VBAT depletion event interrupt. VBAT_DPL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VBAT_LOW_BOOST_MASK	0	R/W	Mask VBAT_LOW_BOOST Event Interrupt 0 = VBAT_LOW_BOOST event interrupt can work (default) 1 = Mask VBAT_LOW_BOOST event interrupt. VBAT_LOW_BOOST_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VBUS_GOOD_MASK	0	R/W	Mask VBUS_GOOD Event Interrupt 0 = VBUS_GOOD event interrupt can work (default) 1 = Mask VBUS_GOOD event interrupt. VBUS_GOOD_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER MAPS (continued)

REG0x48: CHG_INT_MASK2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	CHG_MASK	0	R/W	Mask Charging Status Change Event Interrupt 0 = Charging status change event interrupt can work (default) 1 = Mask charging status change event interrupt. CHG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	BOOST_OK_MASK	0	R/W	Mask BOOST Operation Event Interrupt 0 = BOOST operation event interrupt can work (default) 1 = Mask BOOST operation event interrupt. BOOST_OK_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	VSYSMIN_REG_MASK	0	R/W	Mask VSYSMIN Regulation Event Interrupt 0 = VSYSMIN regulation event interrupt can work (default) 1 = Mask VSYSMIN regulation event interrupt. VSYSMIN_REG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	QB_ON_MASK	0	R/W	Mask QB_ON Event Interrupt 0 = QB_ON event interrupt can work (default) 1 = Mask QB_ON event interrupt. QB_ON_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x49: CHG_INT_MASK3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TDIE_REG_MASK	0	R/W	Mask Thermal Regulation Event Interrupt 0 = Thermal regulation event interrupt can work (default) 1 = Mask thermal regulation event interrupt. TDIE_REG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	TSBAT_COOL_MASK	0	R/W	Mask TSBAT_COOL Event Interrupt 0 = TSBAT_COOL event interrupt can work (default) 1 = Mask TSBAT_COOL event interrupt. TSBAT_COOL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	TSBAT_WARM_MASK	0	R/W	Mask TSBAT_WARM Event Interrupt 0 = TSBAT_WARM event interrupt can work (default) 1 = Mask TSBAT_WARM event interrupt. TSBAT_WARM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	Reserved	0	R	Reserved	N/A
D[2]	ICO_MASK	0	R/W	Mask ICO Status Change Event Interrupt 0 = ICO status change event interrupt can work (default) 1 = Mask ICO status change event interrupt. ICO_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	IINDPM_MASK	0	R/W	Mask IINDPM Event Interrupt 0 = IINDPM event interrupt can work (default) 1 = Mask IINDPM event interrupt. IINDPM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VINDPM_MASK	0	R/W	Mask VINDPM Event Interrupt 0 = VINDPM event interrupt can work (default) 1 = Mask VINDPM event interrupt. VINDPM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER MAPS (continued)

REG0x50: CHG_FLT_STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CONV_OCP_STAT	0	R	Buck Converter OCP Fault Status Bit 0 = Normal 1 = Device is in CONV_OCP status	N/A
D[3]	VSYS_OVP_STAT	0	R	SYS OVP Fault Status Bit 0 = Normal 1 = Device is in VSYS_OVP status	N/A
D[2]	Reserved	0	R	Reserved	N/A
D[1]	IBAT_OCP_STAT	0	R	BATFET OCP Fault Status Bit 0 = Normal 1 = Device is in IBAT_OCP status	N/A
D[0]	VBAT_OVP_BUCK_STAT	0	R	Buck Battery OVP Fault Status Bit 0 = Normal 1 = Device is in VBAT_OVP_BUCK status	N/A

REG0x51: CHG_FLT_STAT2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	OTG_HICCUP_STAT	0	R	OTP Hiccup Status Bit 0 = Normal 1 = Device is in OTG_HICCUP status	N/A
D[2]	CHG_TIMEOUT_STAT	0	R	Charge Safety Timer Timeout Status Bit 0 = Normal 1 = Device is in CHG_TIMEOUT status	N/A
D[1]	VPMID_SHORT_STAT	0	R	PMID_BUCK Short Circuit Fault Status Bit 0 = Normal 1 = Device is in VPMID_SHORT status	N/A
D[0]	VPMID_OVP_OTG_STAT	0	R	PMID_BUCK OVP in Boost Mode Status Bit 0 = Normal 1 = Device is in VPMID_OVP_OTG status	N/A

REG0x52: CHG_FLT_FLAG1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CONV_OCP_FLAG	0	RC	CONV_OCP Fault Flag Bit 0 = No CONV_OCP fault 1 = CONV_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	VSYS_OVP_FLAG	0	RC	VSYS_OVP Fault Flag Bit 0 = No VSYS_OVP fault 1 = VSYS_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	Reserved	0	R	Reserved	N/A
D[1]	IBAT_OCP_FLAG	0	RC	BATFET OCP Fault Flag Bit 0 = No BATFET OCP fault 1 = BATFET OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VBAT_OVP_BUCK_FLAG	0	RC	VBAT_OVP_BUCK Fault Flag Bit 0 = No VBAT_OVP_BUCK fault 1 = VBAT_OVP_BUCK fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x53: CHG_FLT_FLAG2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	OTG_HICCUP_FLAG	0	RC	OTG_HICCUP Fault Flag Bit 0 = No OTG_HICCUP fault 1 = OTG_HICCUP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	CHG_TIMEOUT_FLAG	0	RC	Charger Safety Timeout Fault Flag Bit 0 = No charger safety timeout fault 1 = Charger safety timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VPMID_SHORT_FLAG	0	RC	PMID Short Circuit Fault Flag Bit 0 = No PMID short circuit fault 1 = PMID short circuit fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VPMID_OVP_OTG_FLAG	0	RC	VPIMD_OVP_OTG Fault Flag Bit 0 = No VPIMD_OVP_OTG fault 1 = VPIMD_OVP_OTG fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x54: CHG_FLT_MASK1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CONV_OCP_MASK	0	R/W	Mask CONV_OCP Fault Interrupt 0 = CONV_OCP fault interrupt can work (default) 1 = Mask CONV_OCP fault interrupt. CONV_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	VSYS_OVP_MASK	0	R/W	Mask VSYS_OVP Fault Interrupt 0 = VSYS_OVP fault interrupt can work (default) 1 = Mask VSYS_OVP fault interrupt. VSYS_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1]	IBAT_OCP_MASK	0	R/W	Mask BATFET OCP Fault Interrupt 0 = BATFET OCP fault interrupt can work (default) 1 = Mask BATFET OCP fault interrupt. IBAT_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VBAT_OVP_BUCK_MASK	0	R/W	Mask VBAT_OVP_BUCK Fault Interrupt 0 = VBAT_OVP_BUCK fault interrupt can work (default) 1 = Mask VBAT_OVP_BUCK fault interrupt. VBAT_OVP_BUCK_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER MAPS (continued)

REG0x55: CHG_FLT_MASK2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	OTG_HICCUP_MASK	0	R/W	Mask OTG_HICCUP Fault Interrupt 0 = OTG_HICCUP fault interrupt can work (default) 1 = Mask OTG_HICCUP fault interrupt. OTG_HICCUP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	CHG_TIMEOUT_MASK	0	R/W	Mask Charger Safety Timeout Fault Interrupt 0 = Charger safety timeout fault interrupt can work (default) 1 = Mask charger safety timeout fault interrupt. CHG_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VPMID_SHORT_MASK	0	R/W	Mask PMID Short Circuit Fault Interrupt 0 = PMID short circuit fault interrupt can work (default) 1 = Mask PMID short circuit fault interrupt. VPMID_SHORT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VPMID_OVP_OTG_MASK	0	R/W	Mask VPIMD_OVP_OTG Fault Interrupt 0 = VPIMD_OVP_OTG fault interrupt can work (default) 1 = Mask VPIMD_OVP_OTG fault interrupt. VPIMD_OVP_OTG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x56: JEITA_CTRL1 Register [Reset = 0x55]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	JEITA_ISET_COOL[1:0]	01	R/W	Charge Current Setting During JEITA Cool Temperature 00 = No Charge 01 = 20% of ICHG_CC (default) 10 = 50% of ICHG_CC 11 = 100% of ICHG_CC	REG_RST WDT_RST
D[5:4]	JEITA_ISET_WARM[1:0]	01	R/W	Charge Current Setting During JEITA Warm Temperature 00 = No Charge 01 = 20% of ICHG_CC (default) 10 = 50% of ICHG_CC 11 = 100% of ICHG_CC	
D[3:2]	JEITA_COOL[1:0]	01	R/W	JEITA Cool Temperature Threshold Setting 00 = 5℃, 70.75% of REGN voltage (rising threshold) 01 = 10℃ (default), 68.25% of REGN voltage (rising threshold) 10 = 15℃, 65.25% of REGN voltage (rising threshold) 11 = 20℃, 62.25% of REGN voltage (rising threshold)	
D[1:0]	JEITA_WARM[1:0]	01	R/W	JEITA Warm Temperature Threshold Setting 00 = 40℃, 48.15% of REGN voltage (falling threshold) 01 = 45℃ (default), 44.6% of REGN voltage (falling threshold) 10 = 50℃, 40.6% of REGN voltage (falling threshold) 11 = 55℃, 37.6% of REGN voltage (falling threshold)	

REGISTER MAPS (continued)

REG0x57: JEITA_CTRL2 Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	00 0000	R	Reserved	N/A
D[1:0]	JEITA_VSET_WARM[1:0]	10	R/W	Charge Voltage Setting During JEITA Warm Temperature 00 = Set Charge Voltage to V_{BAT_REG} during JEITA warm temperature 01 = Set Charge Voltage to V_{BAT_REG} - 50mV during JEITA warm temperature 10 = Set Charge Voltage to V_{BAT_REG} - 100mV during JEITA warm temperature (default) 11 = Set Charge Voltage to V_{BAT_REG} - 200mV during JEITA warm temperature	REG_RST WDT_RST

REG0x58: nSYS_OK_CTRL Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	BOOST_START_DELAY	0	R/W	Boost Mode Startup Delay Setting Bit 0 = Disable Boost mode delay time shortening function (default) 1 = Shorten the Boost mode startup time by no more than 15ms	REG_RST WDT_RST
D[5]	PFM_DIS_BUCK	0	R/W	PFM Disable in Buck Mode 0 = Enable PFM (default) 1 = Disable PFM	REG_RST WDT_RST
D[4]	SIGNAL_SEL_nSYSOK_TIMER	0	R/W	Signal Selection for Initiating nSYS_OK Deglitch Timer 0 = Soft-start finished (default) 1 = VBUS_GOOD	REG_RST WDT_RST
D[3:2]	Reserved	00	R	Reserved	N/A
D[1:0]	nSYS_OK_DEG[1:0]	01	R/W	nSYS_OK Output Deglitch Time after VBUS_GOOD Signal or Buck Charger Soft-Start Finished 00 = 50ms 01 = 150ms (default) 10 = 200ms 11 = 300ms	REG_RST WDT_RST

REG0x59: MISC_CHGR_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BATFET_RST_WVBUS	0	R/W	Enable System Reset when VBUS is Present 0 = Disable (default) 1 = Enable	N/A
D[6:2]	Reserved	0 0000	R	Reserved	N/A
D[1]	Q1_FULLON	0	R/W	RBFET Q1 Setting 0 = Use higher R_{DSON} if I_{INDPM} < 700mA (for better accuracy) (default) 1 = Use lower R_{DSON} always (fully ON for better efficiency) Used to control the on-resistance of Q1 (RBFET switch) for better input current measurement accuracy. In Boost mode, full FET is always used.	REG_RST
D[0]	DIS_HICCUP_RST	0	R/W	Enable 7 Times HICCUP Retry or HICCUP Retry Forever 0 = 7 times HICCUP retry (default) 1 = HICCUP retry forever	REG_RST

REGISTER MAPS (continued)

Switched Cap Fast Charger

REG0x60: VBATSNS_OVP Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBATSNS_OVP_DIS	0	R/W	VBATSNS_OVP Protection Disable Bit 0 = Enable protection (default) 1 = Disable protection	REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5:0]	VBATSNS_OVP[5:0]	10 0010	R/W	Battery Over-Voltage Protection Setting When the battery voltage goes above the programmed threshold, an INT is sent and SCC_EN bit is set to 0. Fixed Offset: 3.5V Bit step size: 25mV Range: 3.5V (000000) – 5.075V (111111) Default: 4.35V (100010)	REG_RST

REG0x61: IBUS_OCP_UCP Register [Reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:5]	IBUS_UCP_FALL_DEG_SET[1:0]	01	R/W	IBUS_UCP_FALL Deglitch Time Setting Bits 00 = 250μs 01 = 5ms (default) 10 = 40ms 11 = 160ms	REG_RST
D[4:0]	IBUS_OCP[4:0]	0 1000	R/W	Bus Over-Current Protection Setting When the bus current reaches the programmed threshold, an INT is sent and SCC_EN bit is set to '0'. Fixed Offset: 1A Bit step size: 250mA Range: 1A (00000) – 6.5A (10110 ~ 11111) Default: 3A (01000)	REG_RST

REG0x62: PMID2BAT_OVP Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2BAT_OVP_DIS	0	R/W	PMID2BAT_OVP Protection Disable Bit 0 = Enable PMID2BAT over-voltage protection (default) 1 = Disable PMID2BAT over-voltage protection	REG_RST
D[6:3]	Reserved	0000	R	Reserved	N/A
D[2:0]	PMID2BAT_OVP[2:0]	011	R/W	PMID/n-VBAT OVP Protection Threshold n = 1 for 1:1 charger mode, n = 2 for 2:1 charger mode Fixed offset: 250mV Bit step size: 50mV Range: 250mV (000) ~ 600mV (111) Default: 400mV (011)	REG_RST

REG0x63: PMID2BAT_UVP Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PMID2BAT_UVP_DIS	0	R/W	PMID2BAT_UVP Protection Disable Bit 0 = Enable PMID2BAT under-voltage protection (default) 1 = Disable PMID2BAT under-voltage protection	REG_RST
D[6:3]	Reserved	0000	R	Reserved	N/A
D[2:0]	PMID2BAT_UVP[2:0]	010	R/W	PMID/n-VBAT UVP Protection Threshold n = 1 for 1:1 charger mode, n = 2 for 2:1 charger mode Fixed offset: -50mV Bit step size: 25mV Range: -50mV (000) ~ -225mV (111) Default: -100mV (010)	REG_RST

REGISTER MAPS (continued)

REG0x64: CP_CTRL1 Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	FSW_SET[2:0]	100	R/W	Switched Capacitor Charger Switching Frequency Setting Bits 000 = 460kHz 001 = 520kHz 010 = 580kHz 011 = 640kHz 100 = 700kHz (default) 101 = 760kHz 110 = 820kHz 111 = 1000kHz	REG_RST
D[4:3]	FREQ_SHIFT[1:0]	00	R/W	Bits of Adjusting Switching Frequency for EMI 00 = Nominal frequency (default) 01 = +10% 10 = -10% 11 = Spread spectrum varies frequency ±10%	REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1]	SCC_MODE	0	R/W	Switched Capacitor Charge Operation Mode Control Bit 0 = 2:1 charger mode (default) 1 = 1:1 charger mode SCC_MODE bit is not allowed to change when SCC_EN = 1	REG_RST WDT_RST
D[0]	SCC_EN	0	R/W	Switched Capacitor Charger Enable Bit 0 = Switched capacitor disabled (default) 1 = Switched capacitor enabled	REG_RST WDT_RST

REG0x65: CP_CTRL2 Register [Reset = 0xE0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	SS_TIMEOUT[2:0]	111	R/W	Adjustable Timeout Setting Bits for IBUS to Rise to the IBUS_UCP_RISE_THRESHOLD 000 = SS Timeout Disabled 001 = 12.5ms 010 = 25ms 011 = 50ms 100 = 100ms 101 = 400ms 110 = 1.5s 111 = 10s (default)	REG_RST
D[4]	Reserved	0	R	Reserved	N/A
D[3]	IBUS_UCP_DIS	0	R/W	IBUS_UCP Protection Disable Bit 0 = Enable the IBUS_UCP protection (default) 1 = Disable the IBUS_UCP protection	REG_RST
D[2]	IBUS_OCP_DIS	0	R/W	IBUS_OCP Protection Disable Bit 0 = Enable the IBUS_OCP protection (default) 1 = Disable the IBUS_OCP protection	REG_RST
D[1]	VBUS_PD_100mA_1s_DIS	0	R/W	VBUS 100mA/1s Pull-Down Disable Bit 0 = Enable the 100mA/1s pull-down on VBUS once a SCC_EN signal falling edge is detected (default) 1 = Disable the 100mA/1s pull-down on VBUS once a SCC_EN signal falling edge is detected	REG_RST
D[0]	VBUS_IN_RANGE_DIS	0	R/W	VBUS_IN_RANGE Protection (include VBUS_ERROR_HI and VBUS_ERROR_LO) Disable Bit 0 = Enable the VBUS_IN_RANGE protection (default) 1 = Disable the VBUS_IN_RANGE protection	REG_RST

REGISTER MAPS (continued)

REG0x66: CP_INT_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	IBUS_UCP_RISE_STAT	0	R	IBUS_UCP_RISE Status Bit 0 = The IBUS is lower than IBUS_UCP_RISE rising threshold 1 = The IBUS is higher than IBUS_UCP_RISE rising threshold	N/A
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	VBUS_ERROR_HI_STAT	0	R	VBUS_ERROR_HI Status Bit 0 = Not in VBUS_ERROR_HI status 1 = In VBUS_ERROR_HI status	N/A
D[1]	VBUS_ERROR_LO_STAT	0	R	VBUS_ERROR_LO Status Bit 0 = Not in VBUS_ERROR_LO status 1 = In VBUS_ERROR_LO status	N/A
D[0]	SCC_SWITCHING_STAT	0	R	Switched Capacitor Charger Switching Status Bit 0 = Switched capacitor charger is not switching 1 = Switched capacitor charger is switching	N/A

REG0x67: CP_INT_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	IBUS_UCP_RISE_FLAG	0	RC	IBUS Higher than IBUS_UCP_RISE Event Flag Bit 0 = No IBUS higher than IBUS_UCP_RISE event 1 = IBUS higher than IBUS_UCP_RISE event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	VBUS_ERROR_HI_FLAG	0	RC	VBUS_ERROR_HI Fault Flag Bit 0 = No VBUS_ERROR_HI fault 1 = VBUS_ERROR_HI fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBUS_ERROR_LO_FLAG	0	RC	VBUS_ERROR_LO Fault Flag Bit 0 = No VBUS_ERROR_LO fault 1 = VBUS_ERROR_LO fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	SCC_SWITCHING_FLAG	0	RC	Switched Capacitor Charger Switching Event Flag Bit 0 = No switched capacitor charger switching event 1 = Switched capacitor charger switching event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x68: CP_INT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	IBUS_UCP_RISE_MASK	0	R/W	Mask IBUS Higher than IBUS_UCP_RISE Event Interrupt 0 = IBUS higher than IBUS_UCP_RISE event interrupt can work (default) 1 = Mask IBUS higher than IBUS_UCP_RISE event interrupt. IBUS_UCP_RISE_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	VBUS_ERROR_HI_MASK	0	R/W	Mask VBUS_ERROR_HI Fault Interrupt 0 = VBUS_ERROR_HI fault interrupt can work (default) 1 = Mask VBUS_ERROR_HI fault interrupt. VBUS_ERROR_HI_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[1]	VBUS_ERROR_LO_MASK	0	R/W	Mask VBUS_ERROR_LO Fault Interrupt 0 = VBUS_ERROR_LO fault interrupt can work (default) 1 = Mask VBUS_ERROR_LO fault interrupt. VBUS_ERROR_LO_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[0]	SCC_SWITCHING_MASK	0	R/W	Mask Switched Capacitor Charger Switching Event Interrupt 0 = Switched capacitor charger switching event interrupt can work (default) 1 = Mask switched capacitor charger switching event interrupt. SCC_SWITCHING_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A

REG0x69: CP_FLT_STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	SS_TIMEOUT_STAT	0	R	Soft-Start Timeout Fault Status Bit 0 = Normal 1 = Device is in SS_TIMEOUT status	N/A
D[3]	IBUS_UCP_FALL_STAT	0	R	IBUS_UCP_FALL Fault Status Bit 0 = Normal 1 = Device is in IBUS_UCP_FALL status	N/A
D[2]	IBUS_OCP_STAT	0	R	IBUS_OCP Fault Status Bit 0 = Normal 1 = Device is in IBUS_OCP status	N/A
D[1]	VBAT_OVP_CP_STAT	0	R	VBAT_OVP Fault Status Bit 0 = Normal 1 = Device is in VBAT_OVP_CP status	N/A
D[0]	VBATSNS_OVP_STAT	0	R	VBATSNS_OVP Fault Status Bit 0 = Normal 1 = Device is in VBATSNS_OVP status	N/A

REGISTER MAPS (continued)

REG0x6A: CP_FLT_STAT2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2]	PMID2BAT_OVP_STAT	0	R	PMID2BAT_OVP Fault Status Bit 0 = Normal 1 = Device is in PMID2BAT_OVP status	N/A
D[1]	PMID2BAT_UVP_STAT	0	R	PMID2BAT_UVP Fault Status Bit 0 = Normal 1 = Device is in PMID2BAT_UVP status	N/A
D[0]	PIN_DIAG_FAIL_STAT	0	R	PIN_DIAG_FAIL Fault Status Bit 0 = Normal 1 = Device is in PIN_DIAG_FAIL status	N/A

REG0x6B: CP_FLT_FLAG1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	SS_TIMEOUT_FLAG	0	RC	Soft-Start Timeout Fault Flag Bit 0 = No soft-start timeout fault 1 = Soft-start timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	IBUS_UCP_FALL_FLAG	0	RC	IBUS_UCP_FALL Fault Flag Bit 0 = No IBUS_UCP_FALL fault 1 = IBUS_UCP_FALL fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	IBUS_OCP_FLAG	0	RC	IBUS_OCP Fault Flag Bit 0 = No IBUS_OCP fault 1 = IBUS_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	VBAT_OVP_CP_FLAG	0	RC	VBAT_OVP Fault Flag Bit 0 = No VBAT_OVP fault 1 = VBAT_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VBATSNS_OVP_FLAG	0	RC	VBATSNS_OVP Fault Flag Bit 0 = No VBATSNS_OVP fault 1 = VBATSNS_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x6C: CP_FLT_FLAG2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2]	PMID2BAT_OVP_FLAG	0	RC	PMID2BAT_OVP Fault Flag Bit 0 = No PMID2BAT_OVP fault 1 = PMID2BAT_OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	PMID2BAT_UVP_FLAG	0	RC	PMID2BAT_UVP Fault Flag Bit 0 = No PMID2BAT_UVP fault 1 = PMID2BAT_UVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	PIN_DIAG_FAIL_FLAG	0	RC	PIN_DIAG_FAIL Fault Flag Bit 0 = No PIN_DIAG_FAIL fault 1 = PIN_DIAG_FAIL fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x6D: CP_FLT_MASK1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	SS_TIMEOUT_MASK	0	RC	Mask Soft-Start Timeout Fault Interrupt 0 = Soft-start timeout fault interrupt can work (default) 1 = Mask soft-start timeout fault interrupt. SS_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[3]	IBUS_UCP_FALL_MASK	0	RC	Mask IBUS_UCP_FALL Fault Interrupt 0 = IBUS_UCP_FALL fault interrupt can work (default) 1 = IBUS_UCP_FALL fault interrupt. IBUS_UCP_FALL_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[2]	IBUS_OCP_MASK	0	RC	Mask IBUS_OCP Fault Interrupt 0 = IBUS_OCP fault interrupt can work (default) 1 = IBUS_OCP fault interrupt. IBUS_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[1]	VBAT_OVP_CP_MASK	0	RC	Mask VBAT_OVP Fault Interrupt 0 = VBAT_OVP fault interrupt can work (default) 1 = Mask VBAT_OVP fault interrupt. VBAT_OVP_CP_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[0]	VBATSNS_OVP_MASK	0	RC	Mask VBATSNS_OVP Fault Interrupt 0 = VBATSNS_OVP fault interrupt can work (default) 1 = Mask VBATSNS_OVP fault interrupt. VBATSNS_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A

REG0x6E: CP_FLT_MASK2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2]	PMID2BAT_OVP_MASK	0	RC	Mask PMID2BAT_OVP Fault Interrupt 0 = PMID2BAT_OVP fault interrupt can work (default) 1 = Mask PMID2BAT_OVP fault interrupt. PMID2BAT_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[1]	PMID2BAT_UVP_MASK	0	RC	Mask PMID2BAT_UVP Fault Interrupt 0 = PMID2BAT_UVP fault interrupt can work (default) 1 = Mask PMID2BAT_UVP fault interrupt. PMID2BAT_UVP_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[0]	PIN_DIAG_FAIL_MASK	0	RC	Mask PIN_DIAG_FAIL Fault Interrupt 0 = PIN_DIAG_FAIL fault interrupt can work (default) 1 = Mask PIN_DIAG_FAIL fault interrupt. PIN_DIAG_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A

REGISTER MAPS (continued)

REG0x6F: CP_FLT_DIS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	PIN_DIAG_DIS	0	R/W	PIN_DIAG Function Disable Bit 0 = Enable function 1 = Disable function	REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1]	VBAT_OVP_CP_DIS	0	R/W	Switched Capacitor Charger VBAT_OVP Protection Disable Bit 0 = Enable function 1 = Disable function	REG_RST
D[0]	VSLEEP_CP_DIS	0	R/W	Minimum VBUS-VBAT Voltage Protection Disable Bit 0 = Enable function 1 = Disable function	REG_RST

REG0x70: CP_EXT_PROTECTION1 Register [Reset = 0x09]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	CP_IBUS_RCP_DIS	0	R/W	IBUS Reverse Current Protection Disable Bit 0 = Enable IBUS reverse current protection (default) 1 = Disable IBUS reverse current protection	REG_RST
D[4]	CP_IBUS_RCP_FLAG	0	RC	IBUS Reverse Current Fault Flag Bit 0 = No IBUS reverse current fault 1 = IBUS reverse current fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	CP_IBUS_RCP_MASK	1	R/W	Mask IBUS Reverse Current Fault Interrupt 0 = IBUS reverse current fault interrupt can work. 1 = Mask IBUS reverse current fault interrupt. CP_IBUS_RCP_FLAG bit is set after the event, but the interrupt signal is not generated. (default)	N/A
D[2]	CP_CONV_OCP_DIS	0	R/W	Converter OCP Protection Disable Bit 0 = Enable CP converter OCP protection (default) 1 = Disable CP converter OCP protection	REG_RST
D[1]	CP_CONV_OCP_FLAG	0	RC	CP Converter OCP Fault Flag Bit 0 = No CP converter OCP fault 1 = CP converter OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	CP_CONV_OCP_MASK	1	R/W	Mask CP Converter OCP Fault Interrupt 0 = CP converter OCP fault interrupt can work. 1 = Mask CP converter OCP fault interrupt. CP_CONV_OCP_FLAG bit is set after the event, but the interrupt signal is not generated. (default)	N/A

REGISTER MAPS (continued)

REG0x71: CP_EXT_PROTECTION2 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CP_CONV_OCP_BLK_TIME	0	R/W	Converter OCP Blanking Time Setting Bit 0 = 120ns (default) 1 = 50ns	N/A
D[6]	FSW_SET_OFFSET	0	R/W	Additional Positive Frequency Offset to FSW_SET[2:0] Setting 0 = No offset (default) 1 = 300kHz offset	N/A
D[5:3]	Reserved	000	R	Reserved	N/A
D[2]	VBAT_SCP_DIS	0	R/W	Battery Short Circuit Protection Disable Bit 0 = Enable CP VBAT SC protection (default) 1 = Disable CP VBAT SC protection	REG_RST
D[1]	VBAT_SCP_FLAG	0	RC	CP VBAT Short Circuit Fault Flag Bit 0 = No CP VBAT short circuit fault 1 = CP VBAT short circuit fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VBAT_SCP_MASK	1	R/W	Mask CP VBAT Short Circuit Fault Interrupt 0 = CP VBAT short circuit fault interrupt can work. 1 = Mask CP VBAT short circuit fault interrupt. VBAT_SCP_FLAG bit is set after the event, but the interrupt signal is not generated. (default)	N/A

REGISTER MAPS (continued)

DPDM Control

REG0x90: DPDM_EN Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_INDET	0	R/WC	Force D+/D- Detection 0 = Do not force D+/D- detection (default) 1 = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0	REG_RST WDT_RST
D[6]	AUTO_INDET_EN	1	R/W	Automatic D+/D- Detection Enable 0 = Disable D+/D- detection on a VBUS_PRESENT rising edge 1 = Enable D+/D- detection on a VBUS_PRESENT rising edge (default)	REG_RST WDT_RST
D[5]	HVDCP_EN	0	R/WC	High Voltage DCP Handshake when DCP is identified (Return to 0 when HVDCP handshake is done) 0 = Disable HVDCP handshake (default) 1 = Enable HVDCP handshake	REG_RST WDT_RST
D[4:1]	Reserved	0000	R	Reserved	N/A
D[0]	DPDM_FC_EN	0	R/W	DPDM_FC_CTRL Block Enable Bit 0 = Disable DPDM_FC_CTRL block (default) 1 = Enable DPDM_FC_CTRL block	REG_RST WDT_RST

REG0x91: DPDM_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	DP_DRIVE[2:0]	000	R/W	DP Pin Output Driver Voltage Setting Bits 000 = HIZ (default) 001 = 20kΩ pull down 010 = 0.6V 011 = 2V 100 = 2.7V 101 = 3.3V 110 = 3kΩ pull up to 3.3V 111 = Reserved	REG_RST WDT_RST
D[4:2]	DM_DRIVE[2:0]	000	R/W	DM Pin Output Driver Voltage Setting Bits 000 = HIZ (default) 001 = 20kΩ pull down 010 = 0.6V 011 = 2V 100 = 2.7V 101 = 3.3V 110 = 3kΩ pull up to 3.3V 111 = Reserved	REG_RST WDT_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x92: DPDM_FC_CTRL Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	FC3_MINUS	0	R/WC	0 = No action 1= Send FC3_MINUS sequence (return to 0 when task done)	REG_RST WDT_RST
D[2]	FC3_PLUS	0	R/WC	0 = No action 1= Send FC3_PLUS sequence (return to 0 when task done)	REG_RST WDT_RST
D[1:0]	FC2[1:0]	11	R/W	DPDM OUTPUT when DPDM_FC_EN = 1 (REG0x90 bit[0]); 00 = 9V: D+ = 3.3V, D- = 0.6V 01 = 12V: D+ = 0.6V, D- = 0.6V 10 = FC3.0: D+ = 0.6V, D- = 3.3V 11 = 5V: D+ = 0.6V, D- = Pull-Down (default)	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x94: DPDM_INT_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VBUS_STAT[2:0]	000	R	VBUS Status register 000 = No Input 001 = USB Host SDP 010 = USB CDP (1.5A) 011 = USB DCP (3.25A) 100 = HVDCP 101 = Unknown Adapter (500mA) 110 = Non-Standard Adapter (1A/2A/2.1A/2.4A) 111 = OTG NOTE: Software current limit is reported in IINDPM register	N/A
D[4]	Reserved	0	R	Reserved	N/A
D[3]	HVDCP_HANDSHAKE_DONE_FLAG	0	RC	HVDCP Handshake Event Flag Bit 0 = HVDCP handshake not complete 1 = HVDCP handshake done. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	INPUT_DET_DONE_FLAG	0	RC	BC1.2 Detect Event Flag Bit 0 = BC1.2 detect not complete 1 = BC1.2 detect done. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	DP_OVP_FLAG	0	RC	DP OVP Fault Flag Bit 0 = No DP OVP fault 1 = DP OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	DM_OVP_FLAG	0	RC	DM OVP Fault Flag Bit 0 = No DM OVP fault 1 = DM OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x95: DPDM_INT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	HVDCP_HANDSHAKE_DONE_MASK	0	R/W	Mask HVDCP Handshake Event Interrupt 0 = HVDCP handshake event interrupt can work (default) 1 = Mask HVDCP handshake event interrupt. HVDCP_HANDSHAKE_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[2]	INPUT_DET_DONE_MASK	0	R/W	Mask BC1.2 Detect Event Interrupt 0 = BC1.2 detect event interrupt can work (default) 1 = Mask BC1.2 detect event interrupt. INPUT_DET_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[1]	DP_OVP_MASK	0	R/W	Mask DP OVP Fault Interrupt 0 = DP OVP fault interrupt can work (default) 1 = DP OVP fault interrupt. DP_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[0]	DM_OVP_MASK	0	R/W	Mask DM OVP Fault Interrupt 0 = DM OVP fault interrupt can work (default) 1 = DM OVP fault interrupt. DM_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x96: FC3_INT_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1]	FC3_MINUS_DONE_FLAG	0	RC	Send FC3_MINUS Sequence Event Flag Bit 0 = Send FC3_MINUS sequence not complete 1 = Send FC3_MINUS sequence done. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	FC3_PLUS_DONE_FLAG	0	RC	Send FC3_PLUS Sequence Event Flag Bit 0 = Send FC3_PLUS sequence not complete 1 = Send FC3_PLUS sequence done. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REG0x97: FC3_INT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1]	FC3_MINUS_DONE_MASK	0	R/W	Mask Send FC3_MINUS Sequence Event Interrupt 0 = Send FC3_MINUS sequence event interrupt can work (default) 1 = Mask send FC3_MINUS sequence event interrupt. FC3_MINUS_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[0]	FC3_PLUS_DONE_MASK	0	R/W	Mask Send FC3_PLUS Sequence Event Interrupt 0 = Send FC3_PLUS sequence event interrupt can work (default) 1 = Mask send FC3_PLUS sequence event interrupt. FC3_PLUS_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST

REG0x98: DP_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DP_OVP_STAT	0	R	0 = Normal status 1 = DP OVP status	N/A
D[6:5]	Reserved	00	R	Reserved	N/A
D[4]	DP_IN4	0	R	3V	N/A
D[3]	DP_IN3	0	R	2.2V	N/A
D[2]	DP_IN2	0	R	1.35V	N/A
D[1]	DP_IN1	0	R	1V	N/A
D[0]	DP_IN0	0	R	0.325V	N/A

REGISTER MAPS (continued)

REG0x99: DM_STAT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DM_OVP_STAT	0	R	0 = Normal status 1 = DM OVP status	N/A
D[6:5]	Reserved	00	R	Reserved	N/A
D[4]	DM_IN4	0	R	3V	N/A
D[3]	DM_IN3	0	R	2.2V	N/A
D[2]	DM_IN2	0	R	1.35V	N/A
D[1]	DM_IN1	0	R	1V	N/A
D[0]	DM_IN0	0	R	0.325V	N/A

REG0x9A: BC1P2_EXT_CTRL Register [Reset = 0xA0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DCD_DELAY	1	R/W	DCD delay setting: 0 = 150ms 1 = 300ms (default)	REG_RST WDT_RST
D[6:5]	DCD_TIMER[1:0]	01	R/W	When VBUS is present and FORCE_INDET = 0->1,start the DCD_DELAY, then DCD_TIMER. When VBUS is not present before and AUTO_INDET_EN = 1, once an input source is plugged and qualification passed (VBUS_GOOD_STAT bit changes from 0 to1), start the DCD_DELAY, then DCD_TIMER. DCD timer setting: 00 = Disable DCD 01 = 600ms (default) 10 = 900ms 11 = Forever Note: the DCD_TIMER[1:0] value can be adjust in the DCD detection; when DCD_TIMER[1:0] = 11, host can write other value to exit the DCD detection.	REG_RST WDT_RST
D[4]	SET_DPDM_DRIVE_EN	0	R/W	DPDM Output Driver Voltage Enable Bit 0 = Disabled DP_DRIVE, DM_DRVIE output (default) 1 = Enabled DP_DRIVE, DM_DRVIE output	REG_RST WDT_RST
D[3]	DPDM_STAT_EN	0	R/W	DPDM Voltage Status Comparators Enable Bit 0 = Disabled DP/DM STAT comparators. (default) 1 = Enabled DP/DM STAT comparators.	REG_RST WDT_RST
D[2]	BC1.2_VDAT_REF_SET	0	R/W	0.325V Comparison Threshold Setting Bit for BC1.2 Detection 0 = 0.325V (default) 1 = 0.275V	REG_RST WDT_RST
D[1]	BC1.2_DP_SINK	0	R/W	DP Sink Current Capability Setting Bit 0 = 100μA Sink (default) 1 = 50μA Sink	REG_RST WDT_RST
D[0]	BC1.2_DM_SINK	0	R/W	DM Sink Current Capability Setting Bit 0 = 100μA Sink (default) 1 = 50μA Sink	REG_RST WDT_RST

REGISTER MAPS (continued)

PD PHY

Slave device with address 0x52

REG0x00: VENDOR_ID Register [Reset = 0x7E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID_LBYTE[7:0]	0111 1110	R	A Unique 16-Bit Unsigned Integer. Assigned by the USB-IF to the Vendor. Low byte.	N/A

REG0x01: VENDOR_ID Register [Reset = 0x37]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID_HBYTE[7:0]	0011 0111	R	A Unique 16-Bit Unsigned Integer. Assigned by the USB-IF to the Vendor. High byte.	N/A

REG0x02: PRODUCT_ID Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID_LBYTE[7:0]	0000 0000	R	A Unique 16-Bit Unsigned Integer. Assigned by the Vendor to identify the version of the TCPC. Low byte.	N/A

REG0x03: PRODUCT_ID Register [Reset = 0x66]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID_HBYTE[7:0]	0110 0110	R	A Unique 16-Bit Unsigned Integer. Assigned by the Vendor to identify the version of the TCPC. High byte.	N/A

REG0x04: DEVICE_ID Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID_LBYTE[7:0]	0000 0001	R	A Unique 16-Bit Unsigned Integer. Assigned by the Vendor to identify the version of the TCPC. Low byte.	N/A

REG0x05: DEVICE_ID Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID_HBYTE[7:0]	0000 0000	R	A Unique 16-Bit Unsigned Integer. Assigned by the Vendor to identify the version of the TCPC. High byte.	N/A

REG0x06: USBTYPEC_REV Register [Reset = 0x13]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBTYPEC_REV[7:0]	0001 0011	R	Byte 0 of a 16-Bit USB Type-C Revision. Revision 1.3	N/A

REG0x08: USBPD_REV_VER Register [Reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_REV_VER[7:0]	0001 0010	R	Byte 0 of a 16-Bit USB PD version. Version 1.2	N/A

REG0x09: USBPD_REV_REV Register [Reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_REV_REV[7:0]	0011 0000	R	Byte 1 of a 16-Bit USB PD Revision. Revision 3.0	N/A

REGISTER MAPS (continued)

REG0x0A: PDIF_VER Register [Reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_VER[7:0]	0001 0010	R	Byte 0 of a 16-Bit PD Interface (TCPC) Version. Version 1.2	N/A

REG0x0B: PD_INTERFACE_REV Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_REV[7:0]	0010 0000	R	Byte 1 of a 16-Bit PD Interface (TCPC). Revision. Revision 2.0	N/A

REG0x10: ALERT_L Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TX_SUCCESS	0	R/WC	0 = Cleared (default) 1 = Reset or the SOP* message transmission successful.	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5]	TX_DISCARD	0	R/WC	0 = Cleared (default) 1 = Reset or the SOP* message transmission not sent due to incoming receive message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4]	TX_FAIL	0	R/WC	0 = Cleared (default) 1 = The SOP* message is successfully transmitted, no GoodCRC response received on SOP* message transmission.	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	RX_HARD_RESET	0	R/WC	0 = Cleared (default) 1 = Received Hard Reset message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[2]	RX_SOP_MSG_STATUS	0	R/WC	0 = Cleared (default) 1 = Rx buffer registers changed	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	POWER_STATUS	1	R/WC	0 = Cleared 1 = Port status changed (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	CC_STATUS	0	R/WC	0 = Cleared (default) 1 = CC status changed	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x11: ALERT_H Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2]	RXBUF_OVFLOW	0	R/WC	0 = SGM41620 Rx buffer is functioning properly. (default) 1 = SGM41620 Rx buffer has overflowed	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	FAULT	0	R/WC	0 = No Fault (default) 1 = A Fault has occurred. Read the FAULT_STATUS register	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	Reserved	0	R/W	Reserved	N/A

REGISTER MAPS (continued)

REG0x12: ALERT_L_MASK Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	M_TX_SUCCESS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5]	M_TX_DISCARD	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4]	M_TX_FAIL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	M_RX_HARD_RESET	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[2]	M_RX_SOP_MSG_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	M_POWER_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	M_CC_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x13: ALERT_H_MASK Register [Reset = 0x06]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2]	M_RXBUF_OVFLOW	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	M_FAULT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	Reserved	0	R	Reserved	N/A

REG0x14: POWER_STATUS_MASK Register [Reset = 0x46]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	M_TCPC_INITIAL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5:3]	Reserved	000	R	Reserved	N/A
D[2]	M_VAC_PRESENT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	M_VCONN_PRESENT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	Reserved	0	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x15: FAULT_STATUS_MASK Register [Reset = 0x83]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_VCON_OV	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[6:2]	Reserved	0 0000	R	Reserved	N/A
D[1]	M_VCON_OC	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	M_I2C_ERROR	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked (default)	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x19: TCPC_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	WDT_MON_EN	0	R/W	0 = Watchdog Monitoring is disabled (default) 1 = Watchdog Monitoring is enabled The watchdog timer shall start when any of the interrupts that are not masked in the interrupt register are set or when the INT_N pin is asserted.	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4:2]	Reserved	000	R	Reserved	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	BIST_TEST_MODE	0	R/W	0 = Normal Operation. RECEIVE_DETECT-enabled messages passed to TCPM via Alert. 1 = BIST Test Mode. RECEIVE_DETECT-triggered messages generate GoodCRC response but not reach TCPM via Alert.	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	PLUG_ORIENT	0	R/W	0 = When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD message delivery is enabled. 1 = When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD message delivery is enabled.	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x1A: ROLE_CTRL Register [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	EN_DRP	0	R/W	0 = No DRP. CC1/2[1:0] bits determine Rp/Rd/Ra or open settings for CC1 or CC2 pin. (default) 1 = DRP	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5:4]	RP_VALUE[1:0]	00	R/W	00 = Rp default (default) 01 = Rp 1.5A 10 = Rp 3.0A 11 = Reserved	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3:2]	CC2[1:0]	10	R/W	00 = Ra 01 = Rp (Use Rp definition in RP_VALUE[1:0] bits) 10 = Rd (default) 11 = Open (Disconnect or don't care)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1:0]	CC1[1:0]	10	R/W	00 = Ra 01 = Rp (Use Rp definition in RP_VALUE[1:0] bits) 10 = Rd (default) 11 = Open (Disconnect or don't care)	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x1B: FAULT_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DIS_VCON_OV	0	R/W	0 = VCONN over-voltage detect enabled (default) 1 = VCONN over-voltage detect disabled	SOFT_RESET PD_REG_RST PD_WDT_RST
D[6:1]	Reserved	000 000	R	Reserved	N/A
D[0]	DIS_VCON_OC	0	R/W	0 = VCONN over-current detect enabled (default) 1 = VCONN over-current detect disabled	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x1C: VCONN_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000 000	R	Reserved	N/A
D[0]	EN_VCONN	0	R/W	0 = Disable VCONN Source (default) 1 = Enable VCONN Source to CC Required	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x1D: CC_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	DRP_STATUS	0	R	0 = CC has stopped toggling or EN_DRP bit in ROLE_CTRL register is 0b0 (default) 1 = CC is toggling	N/A
D[4]	DRP_RESULT	0	R	0 = SGM41620 is presenting Rp (default) 1 = SGM41620 is presenting Rd	N/A

D[3:2]	CC2_STATUS[1:0]	00	R	If (ROLE_CONTROL.CC2 = Rp) or (DRP_RESULT = 0)
				00 = SRC.Open (open, Rp) (default)
				01 = SRC.Ra (below maximum vRa)
				10 = SRC.Rd (within the vRd range)
				11 = Reserved
				If (ROLE_CONTROL.CC2 = Rd) or (DRP_RESULT = 1)
				00 = SNK.Open (below maximum vRa)
				01 = SNK.Default (above minimum vRd-Connect)
				10 = SNK.Power1.5 (above minimum vRd-Connect), detects Rp 1.5A
				11 = SNK.Power3.0 (above minimum vRd-Connect), detects Rp 3.0A
				If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC2 = Open, this field is set to 00b
				This field always returns 00b if (DRP_STATUS = 1) or (VCONN_CTRL.EN_VCONN = 1 and TCPC_CTRL.PLUG_ORIENT = 0).
				Otherwise, the returned value depends upon ROLE_CONTROL.CC2.
					N/A

D[1:0]	CC1_STATUS[1:0]	00	R	If (ROLE_CONTROL.CC1 = Rp) or (DRP_RESULT = 0)
				00 = SRC.Open (Open, Rp) (default)
				01 = SRC.Ra (below maximum vRa)
				10 = SRC.Rd (within the vRd range)
				11 = Reserved
				If (ROLE_CONTROL.CC1 = Rd) or DRP_RESULT = 1)
				00 = SNK.Open (Below maximum vRa) (default)
				01 = SNK.Default (Above minimum vRd-Connect)
				10 = SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
				11 = SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
				If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC1 = Open, this field is set to 00b
				This field always returns 00b if (DRP_STATUS = 1) or (VCONN_CTRL.EN_VCONN = 1 and TCPC_CTRL.PLUG_ORIENT = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1
					N/A

REGISTER MAPS (continued)

REG0x1E: POWER_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	TCPC_INITIAL	0	R	0 = The TCPC has completed initialization and all registers are valid 1 = The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h...0Fh	N/A
D[5:3]	Reserved	000	R	Reserved	N/A
D[2]	VAC_PRESENT	0	R	0 = VAC Disconnected (default) 1 = VAC Connected	N/A
D[1]	VCONN_PRESENT	0	R	0 = VCONN is not present (default) 1 = This bit is asserted when VCONN present CC1 or CC2. The rising threshold is 2.6V, falling threshold is 2.4V.	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x1F: FAULT_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VCONN_OV	0	R/WC	0 = Not in a VCONN over-voltage protection state (default) 1 = VCONN Over-voltage fault latched	N/A
D[6:2]	Reserved	0 0000	R	Reserved	N/A
D[1]	VCONN_OC	0	R/WC	0 = No fault detected (default) 1 = Over-current VCONN fault latched	N/A
D[0]	I2C_ERROR	0	R/WC	0 = No Error (default) 1 = I²C error has occurred	N/A

REG0x23: COMMAND Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	COMMAND[7:0]	0000 0000	R/W	00100010 = Disable vSafe0V detection 00110011 = Enable vSafe0V detection 10011001 = Start DRP. Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2 = 01b, start with Rp, if ROLE_CONTROL.CC1/CC2 = 10b, start with Rd. Others: Reserved	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x24: DEVICE_CAPABILITIES_1L Register [Reset = 0xD8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	ROLES_SUPPORT[2:0]	110	R	000 = Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001 = Source only 010 = Sink only 011 = Sink with accessory support (optional) 100 = DRP only 101 = Source, Sink, DRP, Adapter/Cable all supported 110 = Source, Sink, DRP (default) 111 = Not valid	N/A
D[4]	ALL_SOP_SUPPORT	1	R	0 = All SOP* except SOP'_DBG/SOP''_DBG 1 = All SOP* messages are supported (default)	N/A
D[3]	SOURCE_VCONN	1	R	0 = SGM41620 is not capable of switching VCONN 1 = SGM41620 is capable of switching VCONN (default)	N/A
D[2]	CPB_SINK_VBUS	0	R	0 = SGM41620 is not capable of controlling the sink path to the system load (default) 1 = SGM41620 is capable of controlling the sink path to the system load	N/A
D[1]	SOURCE_HV_VBUS	0	R	0 = SGM41620 is not capable of controlling the source high voltage path to VBUS (default) 1 = SGM41620 is capable of controlling the source high voltage path to VBUS	N/A
D[0]	SOURCE_VBUS	0	R	0 = SGM41620 is not capable of controlling the source path to VBUS (default) 1 = SGM41620 is capable of controlling the source path to VBUS	N/A

REG0x25: DEVICE_CAPABILITIES_1H Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	CPB_VBUS_OC	0	R	0 = VBUS OCP is not reported by the SGM41620 (default) 1 = VBUS OCP is reported by the SGM41620	N/A
D[5]	CPB_VAC_OV	0	R	0 = VBUS OVP is not reported by the SGM41620 (default) 1 = VBUS OVP is reported by the SGM41620	N/A
D[4:2]	Reserved	000	R	Reserved	N/A
D[1:0]	SOURCE_RPSUPPORT[1:0]	10	R	00 = Rp default only 01 = Rp 1.5A and default 10 = Rp 3.0A, 1.5A and default (default) 11 = Reserved Rp values which may be configured by the TCPM via the ROLE_CTRL register	N/A

REGISTER MAPS (continued)

REG0x26: DEVICE_CAPABILITIES_2L Register [Reset = 0x31]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SINK_DISCONNECT_DET	0	R	0 = VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER STATUS) (default) 1 = VBUS_SINK_DISCONNECT THRESHOLD implemented	N/A
D[6]	STOP_DISC_THD	0	R	0 = VBUS_STOP_DISCHARGE_ THRESHOLD not implemented (default) 1 = VBUS_STOP_DISCHARGE_ THRESHOLD implemented	N/A
D[5:4]	VBUS_VOL_ALARM_LSB[1:0]	11	R	00 = TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01 = TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10 = TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11 = Not support this function. (default)	N/A
D[3:1]	VCONN_POWER[2:0]	000	R	000 = 1.0W (default) 001 = 1.5W 010 = 2.0W 011 = 3W 100 = 4W 101 = 5W 110 = 6W 111 = External	N/A
D[0]	VCONN_OCF	1	R	0 = TCPC is not capable of detecting a VCONN fault 1 = TCPC is capable of detecting a VCONN fault (default)	N/A

REGISTER MAPS (continued)

REG0x27: DEVICE_CAPABILITIES_2H Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DEVICE_CAPABILITIES_3 _SUPPORT	0	R	0 = TCPC does not support the DEVICE_CAPABILITIES_3 register (default) 1 = TCPC supports the DEVICE_CAPABILITIES_3 register	N/A
D[6]	MSG DISABLE DISCONNECT	0	R	0 = Sink TCPC disables PD message delivery when ALERT_H.VBUS_SINK_DISCNT has been asserted (default) 1 = Sink TCPC disables PD message delivery using the condition as defined in RECEIVE_DETECT.MSG_DISABLE_DISCNCT	N/A
D[5]	GENERIC_TIMER	0	R	0 = GENERIC_TIMER register is not supported (default) 1 = GENERIC_TIMER register is supported	N/A
D[4]	LONG_MSG	0	R	0 = TCPC only supports 30 bytes content of the SOP* message. The value in RX_BYTE_COUNT shall be less than or equal to 31. The value in TX_BYTE_COUNT shall be less than or equal to 30 (default) 1 = TCPC is capable of supporting 264 bytes content of the SOP* message. The TX_BUF holds up to 264 bytes content of the SOP* message. The TCPM can write up to 132 bytes to the Tx buffer in one burst. The value supported in TX_BYTE_COUNT shall be up to 132. RX_BUF holds up to 264 bytes content SOP* message plus a 30 bytes content SOP* message	N/A
D[3]	SMBUS_PEC	0	R	0 = TCPC_CTRL.EN_SMBUS_PEC is not implemented (default) 1 = TCPC_CTRL.EN_SMBUS_PEC implemented	N/A
D[2]	SOURCE_FR_SWAP	0	R	0 = Not capable of sending fast role swap signal as source when receiving SendFRSwapSignal command or receiving standard input source fast role swap low (default) 1 = Capable of sending fast role swap signal as source TCPC when receiving SendFRSwapSignal command. If STANDARD_INPUT_CAPABITILIES.SOURCE_FR_SWAP = 0b10, capable of sending fast role swap signal as source when standard input source fast role swap is set low	N/A
D[1]	SINK_FR_SWAP	0	R	0 = VCONN_CTRL.FR_SWAP_EN enable not supported as Sink (default) 1 = VCONN_CTRL.FR_SWAP_EN enable supported as Sink	N/A
D[0]	WDT_TMR	1	R	0 = TCPC_CTRL.WDT_MON_EN not implemented 1 = TCPC_CTRL.WDT_MON_EN implemented (default)	N/A

REG0x28: STANDARD_INPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4:3]	SOURCE_FR_SWAP[1:0]	00	R	00 = Not present in TCPC (default) 01 = Present in TCPC as an input only pin 10 = Present in TCPC as a bidirectional pin, sharing with the standard output signal VBUS sink disconnect detect indicator. The “VBUS sink disconnect detect indicator” bit in STANDARD_OUTPUT_CAPABILITIES register shall also be set to 1. 11 = Reserved	N/A
D[2]	VBUS_EXT_OVF	0	R	VBUS External Over-Voltage Fault 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[1]	VBUS_EXT_OCF	0	R	VBUS External Over-Current Fault 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[0]	FORCE_OFF_VBUS_IN	0	R	Force Off VBUS (Source or Sink) 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A

REGISTER MAPS (continued)

REG0x29: STANDARD_OUTPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_SINK_DISCONNECT_DET_IND	0	R	Sink Disconnect Detection Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC Shall present in TCPC if “Source Fast Role Swap” in STANDARD_INPUT_CAPABILITIES is set to 10b (present as a bidirectional pin).	N/A
D[6]	CPB_DBG_ACC_IND	0	R	Debug Accessory Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[5]	CPB_VBUS_PRESENT_MNT	0	R	VBUS Present Monitor 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[4]	CPB_AUDIO_ADT_ACC_IND	0	R	Audio Adapter Accessory Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[3]	CPB_ACTIVE_CABLE_IND	0	R	Active Cable Indicator 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[2]	CPB_MUX_CFG_CTRL	0	R	MUX Configuration Control 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A
D[1]	CPB_CONNECT_PRESENT	0	R	Connection Present 0 = No Connection (default) 1 = Connection Controlled by the TCPM.	N/A
D[0]	CPB_CONNECT_ORIENT	0	R	Connector Orientation 0 = Not present in TCPC (default) 1 = Present in TCPC	N/A

REG0x2E: MESSAGE_HEADER_INFO Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	CABLE_PLUG	0	R/W	0 = Message originated from Source, Sink and DRP (default) 1 = Message originated from a cable	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	DATA_ROLE	0	R/W	0 = UFP (default) 1 = DFP	SOFT_RESET PD_REG_RST PD_WDT_RST
D[2:1]	USBPD_SPECREV[1:0]	01	R/W	00 = Revision 1.0 01 = Revision 2.0 (default) 10 = Revision 3.0 11 = Reserved	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	POWER_ROLE	0	R/W	0 = Sink (default) 1 = Source	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x2F: RECEIVE_DETECT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	EN_CABLE_RST	0	R/W	0 = SGM41620 does not detect Cable Reset signaling (default) 1 = SGM41620 detects Cable Reset signaling	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5]	EN_HARD_RST	0	R/W	0 = SGM41620 does not detect Hard Reset signaling (default) 1 = SGM41620 detects Hard Reset signaling	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4]	EN_SOP2DB	0	R/W	0 = SGM41620 does not detect SOP_DBG'' message (default) 1 = SGM41620 detects SOP_DBG'' message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	EN_SOP1DB	0	R/W	0 = SGM41620 does not detect SOP_DBG' message (default) 1 = SGM41620 detects SOP_DBG' message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[2]	EN_SOP2	0	R/W	0 = SGM41620 does not detect SOP'' message (default) 1 = SGM41620 detects SOP'' message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	EN_SOP1	0	R/W	0 = SGM41620 does not detect SOP' message (default) 1 = SGM41620 detects SOP' message	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	EN_SOP	0	R/W	0 = SGM41620 does not detect SOP message (default) 1 = SGM41620 detects SOP message	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x30: RX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_BYTE_COUNT[7:0]	0000 0000	R/W	Indicates number of bytes in this register that are not stale. The TCPM should read the first RX_BYTE_COUNT byte in this register. This is the number that counts from RX_BUF_FRAME_TYPE to the RX_BUF register which is stored the last data byte.	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x31: RX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2:0]	RX_BUF_FRAME_TYPE[2:0]	000	R/W	Type of Received Frame 000 = Received SOP (default) 001 = Received SOP' 010 = Received SOP'' 011 = Received SOP_DBG' 100 = Received SOP_DBG'' 110 = Received Cable Reset All others are Reserved.	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x32: RX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_0[7:0]	0000 0000	R	Byte0 Bits [7:0] of Message Header	N/A

REG0x33: RX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_1[7:0]	0000 0000	R	Byte1 Bits [15:8] of Message Header	N/A

REG0x34+[x(1~7)-1]×4 RX_BUF_OBJx_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_0[7:0]	0000 0000	R	Byte0 of Data Object x(1~7) of Receive Buffer	N/A

REG0x35+[x(1~7)-1]×4 RX_BUF_OBJx_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_1[7:0]	0000 0000	R	Byte1 of Data Object x(1~7) of Receive Buffer	N/A

REG0x36+[x(1~7)-1]×4 RX_BUF_OBJx_BYTE_2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_2[7:0]	0000 0000	R	Byte2 of Data Object x(1~7) of Receive Buffer	N/A

REG0x37+[x(1~7)-1]×4 RX_BUF_OBJx_BYTE_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_3[7:0]	0000 0000	R	Byte3 of Data Object x(1~7) of Receive Buffer	N/A

REG0x50: TX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	TX_RETRY_CNT[1:0]	00	R/W	00 = No message retry is required (default) 01 = Automatically retry message transmission once 10 = Automatically retry message transmission twice 11 = Automatically retry message transmission three times	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	TX_BUF_FRAME_TYPE[2:0]	000	R/W	Type of Received Frame 000 = Transmit SOP (default) 001 = Transmit SOP' 010 = Transmit SOP" 011 = Transmit SOP_DBG' 100 = Transmit SOP_DBG'' 101 = Transmit Hard Reset 110 = Transmit Cable Reset 111 = Transmit BIST Carrier Mode 2 (SGM41620 shall exit the BIST mode no later than $t_{BISTContMode}$ max)	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x51: TX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_BYTE_COUNT[7:0]	0000 0000	R/W	The Number of Bytes that the TCPM will Write	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x52: TX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_0[7:0]	0000 0000	R/W	Byte0 Bits [7:0] of Message Header	N/A

REG0x53: TX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_1[7:0]	0000 0000	R/W	Byte1 Bits [15:8] of Message Header	N/A

REG0x54+[x(1~7)-1]×4: TX_BUF_OBJx_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_0[7:0]	0000 0000	R/W	Byte0 of Data Object x(1~7) of Transmit Buffer	N/A

REG0x55+[x(1~7)-1]×4: TX_BUF_OBJx_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_1[7:0]	0000 0000	R/W	Byte1 of Data Object x(1~7) of Transmit Buffer	N/A

REG0x56+[x(1~7)-1]×4: TX_BUF_OBJx_BYTE_2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_2[7:0]	0000 0000	R/W	Byte2 of Data Object x(1~7) of Transmit Buffer	N/A

REG0x57+[x(1~7)-1]×4: TX_BUF_OBJx_BYTE_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_3[7:0]	0000 0000	R/W	Byte3 of Data Object x(1~7) of Transmit Buffer	N/A

REG0x90: ANA_CTRL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VCONN_DISCHARGE_EN	0	R/W	Turn on discharge path when CC OVP and VCONN switch on or VCONN OVP occurs 0 = No discharge (default) 1 = Discharge	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x93: VCONN_OCP_CTRL Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VCONN_OCP[2:0]	100	R/W	VCONN Over-Current Control Selection 000 = Current level = 200mA 001 = Current level = 300mA 010 = Current level = 400mA 011 = Current level = 500mA 100 = Current level = 600mA (default) 101 - 111 = Reserved If VCONN OCP is triggered, the switch turns off timing under 20μs.	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4:0]	Reserved	0 0000	R	Reserved	NA

REG0x97: ANA_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1]	VSAFE0V_STATUS	0	R	0 = VAC is above vSafe0V. (default) 1 = VAC is below vSafe0V.	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x98: ANA_INT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	INT_RESET	0	R/WC	0 = Cleared (default) 1 = Hard reset from Enterprise	SOFT_RESET PD_REG_RST PD_WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	INT_RA_DETACH	0	R/WC	0 = Cleared (default) 1 = Ra detach	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	INT_CC_OVP	0	R/WC	0 = Cleared (default) 1 = CC over-voltage triggered	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	INT_VSAFE0V_STATUS	0	R/WC	0 = Cleared (default) 1 = VAC vSafe0V event occurs	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	INT_WAKEUP	0	R/WC	0 = Cleared (default) 1 = Low power mode exited	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0x99: ANA_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_RESET	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	N/A
D[6]	Reserved	0	R	Reserved	N/A
D[5]	M_RA_DETACH	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4:3]	Reserved	00	R	Reserved	N/A
D[2]	M_CC_OVP	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET PD_REG_RST PD_WDT_RST
D[1]	M_VSAFE0V	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET PD_REG_RST PD_WDT_RST
D[0]	M_WAKEUP	0	R/W	0 = Interrupt masked (default) 1 = Interrupt unmasked	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0x9B: ANA_CTRL2 Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CK_300K_SEL	1	R/W	0 = TX Clock_300K from Internal Clock_300K 1 = TX Clock_300K divided from Internal Clock_12M (default)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	SHUTDOWN_OFF	0	R/W	0 = Shutdown mode (default) 1 = Non-Shutdown mode	SOFT_RESET PD_REG_RST PD_WDT_RST
D[4]	ENEXTMSG	0	R/W	0 = Disable PD3.1 extended message (default) 1 = Enable PD3.1 extended message affect GoodCRC receive detect between PD2.0 and PD3.1	SOFT_RESET PD_REG_RST PD_WDT_RST
D[3]	AUTOIDLE_EN	0	R/W	1 = Auto enter idle mode enable (default) 0 = Auto enter idle mode disable	SOFT_RESET PD_REG_RST PD_WDT_RST
D[2:0]	AUTOIDLE_TIMEOUT[2:0]	000	R/W	Enter idle mode timeout time = (AUTOIDLE_TIMEOUT[2:0] × 2 + 1) × 6.4ms	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0xA0: SOFT_RST_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000 000	R	Reserved	N/A
D[0]	SOFT_RESET	0	R/WC	Write to trigger soft-reset	N/A

REG0xA2: DRP_CTRL Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	TDRP[3:0]	0011	R/W	The Period of DRP Advertisement (Period = TDRP[3:0] × 6.4 + 51.2ms) 0000 = 51.2ms 0001 = 57.6ms 0010 = 64ms 0011 = 70.4ms (default) … 1110 = 140.8ms 1111 = 147.2ms	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

REG0xA3: DRP_DUTY_CTRL0 Register [Reset = 0x47]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DRP_DUTY[7:0]	0100 0111	R/W	The Duty of Time when DRP Advertises Source (DUTY = (DRP_DUTY[9:0] + 1) / 1024) 000000000 = 1/1024 000000001 = 2/1024 … 0101000111 = 328/1024 (default) … 1111111110 = 1023/1024 1111111111 = 1024/1024 Note: Setting with 0xA4[9:8]	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0xA4: DRP_DUTY_CTRL1 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	Reserved	0000 00	R	Reserved	N/A
D[1:0]	DRP_DUTY[9:8]	01	R/W	The Duty of Time when DRP Advertises Source (DUTY = (DRP_DUTY[9:0] + 1) / 1024) 0000000000 = 1/1024 000000001 = 2/1024 … 0101000111 = 328/1024 (default) … 1111111110 = 1023/1024 1111111111 = 1024/1024 Note: Setting with 0xA3[7:0]	SOFT_RESET PD_REG_RST PD_WDT_RST

REG0xA5: PD_PHY_RST Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PD_WDT_TIMER_RST	0	R/WC	I²C PD PHY Watchdog Timer Reset 0 = Normal (default) 1 = Reset PD PHY watchdog timer (Back to 0 after timer reset)	SOFT_RESET PD_REG_RST PD_WDT_RST
D[6]	PD_REG_RST	0	R/WC	PD PHY Register Reset 0 = Keep current register setting (default) 1 = Reset to default register value	SOFT_RESET PD_REG_RST PD_WDT_RST
D[5:3]	Reserved	000	R	Reserved	N/A
D[2:0]	PD_WDT_TIMER[2:0]	000	R/W	I²C PD PHY Watchdog Timer Setting for generating the PD_WDT_RST signal. 000 = Disable watchdog timer (default) 001 = 625ms 010 = 1.25s 011 = 2.5s 100 = 5s 101 = 10s 110 = 20s 111 = 40s	SOFT_RESET PD_REG_RST PD_WDT_RST

REGISTER MAPS (continued)

UFCS PHY

Slave device with address 0x53

REG0x00: UFCS_CTRL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_EN	0	R/W	UFCS Block Enable Bit 0 = Disable UFCS block (default) 1 = Enable UFCS block This bit will be reset to default value on a VBUS_PRESENT falling edge	REG_RST WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	UFCS_HANDSHAKE_EN	0	R/WC	UFCS Protocol Handshake Enable Bit 0 = Disable UFCS handshake (default) 1 = Enable UFCS handshake	REG_RST WDT_RST
D[4:3]	BAUD_RATE[1:0]	00	R/W	UFCS Communication Baud Rate Setting Bits 00 = 115200 bps (default) 01 = 57600 bps 10 = 38400 bps 11 = 115200 bps	REG_RST WDT_RST
D[2]	SND_CMD	0	R/WC	Master Transmission Start Bit 0 = Not transaction (default) 1 = Start transaction When transmission is completed, this bit is automatically reset to 0.	REG_RST
D[1]	CABLE_HARDRESET	0	R/WC	Send Reset Command to Cable 0 = Do not send hard-reset command to cable (default) 1 = Send hard-reset command to cable	REG_RST
D[0]	SOURCE_HARDRESET	0	R/WC	Send Reset Command to Source 0 = Do not send hard-reset command to source (default) 1 = Send hard-reset command to source	REG_RST

REG0x01: UFCS_CTRL2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_DP_PULLUP_EN	0	R/W	DP Pull-Up Enable Bit 0 = No pullup (default) 1 = 50kΩ pullup to 3.3V	REG_RST WDT_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	TX_BUFFER_CLR	0	R/WC	TX_BUFFER Clear Bit 0 = Not clear TX_BUFFER data (default) 1 = Clear TX_BUFFER data when it's not locked	REG_RST
D[4]	RX_BUFFER_CLR	0	R/WC	RX_BUFFER Clear Bit 0 = Not clear RX_BUFFER data (default) 1 = Clear RX_BUFFER data when it's not locked	REG_RST
D[3:2]	DETECTED_BAUD_RATE[1:0]	00	R	UFCS Baud Rate Detection Result 00 = 115200 bps (default) 01 = 57600 bps 10 = 38400 bps 11 = Not used	REG_RST WDT_RST
D[1]	ACK_CABLE	0	R/W	UFCS Reply Setting Bit 0 = UFCS reply ACK or NCK to source (default) 1 = UFCS reply ACK or NCK to cable	REG_RST WDT_RST
D[0]	EN_DM_HIZ	0	R/W	DM Pin HIZ-Mode Enable Bit 0 = UFCS drive DM when enable UFCS block (default) 1 = UFCS doesn't drive DM when enable UFCS block	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x03: UFCS_INT_FLAG1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_HANDSHAKE_FAIL_FLAG	0	RC	Error Flag of UFCS Failed Handshake 0 = UFCS handshake success or not complete (default) 1 = UFCS handshake fail. The device auto resets UFCS_HANDSHAKE_EN bit to 0, and then generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	UFCS_HANDSHAKE_SUCC_FLAG	0	RC	Event Flag of UFCS Successful Handshake 0 = UFCS handshake fail or not complete (default) 1 = UFCS handshake success. After a successful initial handshake, this bit is set. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. Then the AP can set the SND_CMD bit to start ping transmission.	N/A
D[5]	SENT_PACKET_COMPLETE_FLAG	0	RC	Event Flag of UFCS Data Packet Transmission Complete 0 = Sent packet not complete or fail (default) 1 = Sent packet complete. After master completes data packet transmission and pulls the DM line high, this flag bit is set. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	DATA_READY_FLAG	0	RC	Received Slave Data is Ready for I²C Read by Master 0 = Received data is not ready (default) 1 = Received data is ready. After slave completes data packet transmission and pulls the DP line high, if no CRC error occurs, this bit is set. Read this bit to reset it to 0.	N/A
D[3]	RX_OVERFLOW_FLAG	0	RC	Error Flag of UFCS Receive Buffer Overflow 0 = RX data don't exceed RX buffer length (default) 1 = RX data exceed RX buffer length. It discards the received data, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	RX_BUFFER_BUSY_FLAG	0	RC	Event Flag of RX Buffer Busy when Receiving Message 0 = The last RX buffer data has been read while a new DATA_READY_FLAG received 1 = The last RX buffer data has not been read while a new DATA_READY_FLAG received. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	MSG_TRANS_FAIL_FLAG	0	RC	Error Flag of UFCS Failed Data Transmission 0 = No message sent fail 1 = Message sent fail after retry three times. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	ACK_RECEIVE_TIMEOUT_FLAG	0	RC	Error Flag of Receiving ACK Signal Timeout 0 = No ACK receive timeout event (default) 1 = ACK receive timeout event has occured. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x04: UFCS_INT_FLAG2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAUD_RATE_ERROR_FLAG	0	RC	Error Flag of UFCS Baud Rate 0 = BAUD_RATE_CHECK OK (default) 1 = BAUD_RATE error. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	TRAINING_BYTES_ERROR_FLAG	0	RC	Error Flag of UFCS Receiving Training Byte 0 = Training byte is right (default) 1 = Training byte is error. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	DATA_BYTE_TMOUT_FLAG	0	RC	Error Flag of Data Byte Duration 0 = Data byte duration is within 600μs (default) 1 = Data byte duration is beyond 600μs. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	LENGTH_ERROR_FLAG	0	RC	Error Flag of Received Data Length 0 = Received data length is right (default) 1 = Received data length is error. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	START_FAIL_FLAG	0	RC	Error Flag of Received Data Start Byte 0 = Received data start byte is right (default) 1 = Received data start byte detects fail. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	STOP_ERROR_FLAG	0	RC	Error Flag of Received Data Stop Byte 0 = Received data stop byte is right (default) 1 = Received data stop byte is error. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	CRC_ERROR_FLAG	0	RC	Error Flag of CRC Check 0 = CRC_check OK (default) 1 = CRC error. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	HARD_RESET_FLAG	0	RC	Event Flag of UFCS Receiving Hard Reset Signal 0 = Do not receive hard reset (default) 1 = Receive hard reset. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REG0x05: UFCS_INT_FLAG3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_CONFLICT_FLAG	0	RC	Event Flag of Bus Conflict 0 = DP and DM bus don't work conflict 1 = DP and DM bus work conflict. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	BAUDRATE_CHG_FLAG	0	RC	Event Flag of UFCS Baud Rate Change 0 = Baud-rate not changed 1 = Baud-rate is changed after RX ping message with different baud-rate. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	DATA_BIT_ERR_FLAG	0	RC	Error Flag of Data Bit 0 = Data bit doesn't changes in the range 1/4~3/4 of bit count 1 = Data bit changes in the range 1/4~3/4 of bit count. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4:2]	Reserved	000	R	Reserved	N/A
D[1]	TX_BUSY	0	R	TX Transmit Status Bit 0 = UFCS PHY TX is not in transmit process 1 = UFCS PHY TX is during transmit process	N/A
D[0]	RX_BUSY	0	R	RX Transmit Status Bit 0 = UFCS PHY RX is not in transmit process 1 = UFCS PHY RX is during transmit process	N/A

REGISTER MAPS (continued)

REG0x06: UFCS_INT_MASK1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_HANDSHAKE_FAIL_MASK	0	R/W	Mask UFCS Failed Handshake Interrupt 0 = UFCS failed handshake interrupt can work. (default) 1 = Mask UFCS failed handshake interrupt. UFCS_HANDSHAKE_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[6]	UFCS_HANDSHAKE_SUCC_MASK	0	R/W	Mask UFCS Successful Handshake Interrupt 0 = UFCS successful handshake interrupt can work. (default) 1 = Mask UFCS successful handshake interrupt. UFCS_HANDSHAKE_SUCC_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[5]	SENT_PACKET_COMPLETE_MASK	0	R/W	Mask UFCS Data Packet Transmission Complete Interrupt 0 = Data packet transmission complete interrupt can work. (default) 1 = Mask data packet transmission complete interrupt. SENT_PACKET_COMPLETE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[4]	DATA_READY_MASK	0	R/W	Mask Received Slave Data Ready Interrupt 0 = Received slave data ready interrupt can work. (default) 1 = Mask received slave data ready interrupt. DATA_READY_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[3]	RX_OVERFLOW_MASK	0	R/W	Mask UFCS Receive Buffer Overflow Interrupt 0 = UFCS receive buffer overflow interrupt can work. (default) 1 = Mask UFCS receive buffer overflow interrupt. RX_OVERFLOW_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[2]	RX_BUFFER_BUSY_MASK	0	R/W	Mask UFCS Receive Buffer Busy Interrupt 0 = UFCS receive buffer busy interrupt can work. (default) 1 = Mask UFCS receive buffer busy interrupt. RX_BUFFER_BUSY_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[1]	MSG_TRANS_FAIL_MASK	0	R/W	Mask UFCS Failed Data Transmission Interrupt 0 = UFCS failed data transmission interrupt can work. (default) 1 = Mask UFCS failed data transmission interrupt. MSG_TRANS_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[0]	ACK_RECEIVE_TIMEOUT_MASK	0	R/W	Mask Receiving ACK Signal Timeout Error Interrupt 0 = Receiving ACK signal timeout error interrupt can work. (default) 1 = Mask receiving ACK signal timeout error interrupt. ACK_RECEIVE_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x07: UFCS_INT_MASK2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAUD_RATE_ERROR_MASK	0	R/W	Mask UFCS Baud Rate Error Interrupt 0 = Baud rate error interrupt can work. (default) 1 = Mask baud rate error interrupt. BAUD_RATE_ERROR_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[6]	TRAINING_BYTES_ERROR_MASK	0	R/W	Mask UFCS Receiving Training Byte Error Interrupt 0 = Receiving training byte error interrupt can work. (default) 1 = Mask receiving training byte error interrupt. TRAINING_BYTES_ERROR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[5]	DATA_BYTE_TMOUT_MASK	0	R/W	Mask Data Byte Duration Timeout Interrupt 0 = Data byte duration timeout interrupt can work. (default) 1 = Mask data byte duration timeout interrupt. DATA_BYTE_TMOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[4]	LENGTH_ERROR_MASK	0	R/W	Mask Received Data Length Error Interrupt 0 = Received data length error interrupt can work. (default) 1 = Mask received data length error interrupt. LENGTH_ERROR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[3]	START_FAIL_MASK	0	R/W	Mask Received Data Start Byte Detected Fail Interrupt 0 = Received data start byte detected fail interrupt can work. (default) 1 = Mask received data start byte detected fail interrupt. START_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[2]	STOP_ERROR_MASK	0	R/W	Mask Received Data Stop Byte Error Interrupt 0 = Received data stop byte error interrupt can work. (default) 1 = Mask received data stop byte error interrupt. STOP_ERROR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[1]	CRC_ERROR_MASK	0	R/W	Mask UFCS Cyclic Redundancy Check (CRC) Error Interrupt 0 = CRC error interrupt can work. (default) 1 = Mask CRC error interrupt. CRC_ERRO_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[0]	HARD_RESET_MASK	0	R/W	Mask UFCS Receiving Hard Reset Signal Interrupt 0 = Receiving hard reset signal interrupt can work. (default) 1 = Mask receiving hard reset signal interrupt. HARD_RESET_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST

REGISTER MAPS (continued)

REG0x08: UFCS_INT_MASK3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_CONFLICT_MASK	0	R/W	Mask BUS Conflict Interrupt 0 = BUS conflict interrupt can work. (default) 1 = Mask BUS conflict interrupt. BUS_CONFLICT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[6]	BAUDRATE_CHG_MASK	0	R/W	Mask UFCS Baud Rate Change Interrupt 0 = Baud rate change interrupt can work. (default) 1 = Mask baud rate change interrupt. BAUDRATE_CHG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[5]	DATA_BIT_ERR_MASK	0	R/W	Mask Data Bit Error Interrupt 0 = Data bit error interrupt can work. (default) 1 = Mask data bit error interrupt. DATA_BIT_ERR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST WDT_RST
D[4:0]	Reserved	0 0000	R	Reserved	N/A

REG0x09: TX_LENGTH Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_LENGTH[7:0]	0000 0000	R/W	UFCS Transmitter Length Configuration Register The length is the number of bytes in the transmitted data packet, excluding training byte and CRC byte. It is automatically reset to 0000 0000 when transmission is completed.	REG_RST WDT_RST

REG0x0A ~ REG0x2D: TX_BUFFERx (x: 0 ~ 35) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_BUFFERx[7:0]	0000 0000	R/W	TX_BUFFER is a 36-byte transmitted buffer. It includes all bytes in the transmitted data packet except the training byte and CRC byte. All of the 36-byte data are automatically reset to 0000 0000 when transmission is completed.	REG_RST WDT_RST

REG0x2E: RX_LENGTH Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_LENGTH[7:0]	0000 0000	R	UFCS Receiver Data Length Register The length is the number of bytes in the received data packet, excluding training byte and CRC byte.	N/A

REG0x2F ~ REG0x6E: RX_BUFFERx (x: 0 ~ 63) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_BUFFERx[7:0]	0000 0000	R	RX_BUFFER is a 64-byte received buffer. It includes all bytes in the received data packet except the training byte.	N/A

REGISTER MAPS (continued)

Dual-Channel LED Control

Slave device with address 0x54

REG0x80: LED_CTRL1 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FLED1_EN	0	R/W	LED1 Flash Mode Enable 0 = LED1 flash mode is disabled (default) 1 = LED1 flash mode is enabled This bit is automatically reset to 0 when flash timeout duration expires.	REG_RST
D[6]	FLED2_EN	0	R/W	LED2 Flash Mode Enable 0 = LED2 flash mode is disabled (default) 1 = LED2 flash mode is enabled This bit is automatically reset to 0 when flash timeout duration expires.	REG_RST
D[5]	TLED1_EN	0	R/W	LED1 Torch Mode Enable 0 = LED1 torch mode is disabled (default) 1 = LED1 torch mode is enabled	REG_RST
D[4]	TLED2_EN	0	R/W	LED2 Torch Mode Enable 0 = LED2 torch mode is disabled (default) 1 = LED2 torch mode is enabled	REG_RST
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	TRPT[2:0]	001	R/W	Torch Current On/Off Ramp Time 000 = 0ms 001 = 1ms (default) 010 = 32ms 011 = 64ms 100 = 128ms 101 = 256ms 110 = 512ms 111 = 1024ms	REG_RST

REG0x81: FLED1_BR_CTR Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:0]	FLED1_BR[6:0]	000 0000	R/W	LED1 Flash Brightness Setting Offset: 25mA (0000000) Step:12.5mA Range: 25mA (0000000) ~ 1.5A (1110110 ~ 1111111) Default: 25mA (0000000)	REG_RST

REG0x82: FLED2_BR_CTR Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:0]	FLED2_BR[6:0]	000 0000	R/W	LED2 Flash Brightness Setting Offset: 25mA (0000000) Step:12.5mA Range: 25mA (0000000) ~ 1.5A (1110110 ~ 1111111) Default: 25mA (0000000)	REG_RST

REGISTER MAPS (continued)

REG0x83: FLED_TIMER Register [Reset = 0x8A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FTIMEOUT_EN	1	R/W	Flash Timeout Protection Enable. 0 = Disable flash Timeout 1 = Enable flash Timeout (default)	REG_RST WDT_RST
D[6:4]	FRPT[2:0]	000	R/W	Flash Current On/Off Ramp Time 000 = 512μs (default) 001 = 1ms 010 = 2ms 011 = 4ms 100 = 8ms 101 = 16ms 110 = 32ms 111 = 64ms	REG_RST
D[3:0]	FTIMEOUT[3:0]	1010	R/W	Flash Timeout Duration 0000 = 50ms 0001 = 100ms 0010 = 150ms 0011 = 200ms 0100 = 250ms 0101 = 300ms 0110 = 350ms 0111 = 400ms 1000 = 450ms 1001 = 500ms 1010 = 600ms (default) 1011 = 700ms 1100 = 800ms 1101 = 900ms 1110 = 1000ms 1111 = 1200ms	REG_RST

REG0x84: TLED1_BR_CTR Register [Reset = 0x8E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TLED1[7:0]	1000 1110	R/W	LED1 Torch Brightness (TLED1[6:0]) Setting when TORCH_STEP_CTRL = 0 Offset: 25mA (0000000) Step:12.5mA Range: 25mA (0000000) ~ 500mA (0100110 ~ 1111111) Default: 200mA (0001110) LED1 Torch Brightness (TLED1[7:0]) Setting when TORCH_STEP_CTRL = 1 Offset: 6.25mA (00000000) Step:1.5625mA Range: 6.25mA (00000000) ~ 404.6875mA (11111111) Default: 228.125mA (10001110)	REG_RST

REGISTER MAPS (continued)

REG0x85: TLED2_BR_CTR Register [Reset = 0x8E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TLED2[7:0]	1000 1110	R/W	LED2 Torch Brightness (TLED2[6:0]) Setting when TORCH_STEP_CTRL = 0 Offset: 25mA (0000000) Step:12.5mA Range: 25mA (0000000) ~ 500mA (0100110 ~ 1111111) Default: 200mA (0001110) LED2 Torch Brightness (TLED2[7:0]) Setting when TORCH_STEP_CTRL = 1 Offset: 6.25mA (00000000) Step:1.5625mA Range: 6.25mA (00000000) ~ 404.6875mA (11111111) Default: 228.125mA (10001110)	REG_RST

REG0x86: LED_PRO Register [Reset = 0x11]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:5]	VBAT_MIN_FLED_DEG[1:0]	00	R/W	VBAT_MIN_FLED Deglitch Time 00 = 10μs (default) 01 = 50μs 10 = 100μs 11 = 500μs	REG_RST
D[4:2]	VBAT_MIN_FLED[2:0]	100	R/W	Falling Threshold of VBAT Voltage to Reset LED Flash Function Enable Bits Offset: 2.8V Range: 2.8V (000) ~ 3.5V (111) Default: 3.2V (100)	REG_RST
D[1:0]	FLASH_FLED_OVP_DEG[1:0]	01	R/W	FLASH_VDD OVP Deglitch Time 00 = 10μs 01 = 50μs (default) 10 = 200μs 11 = 1ms	REG_RST

REG0x87: LED_STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	FLED1_STAT	0	R	The Status of LED1 Flash Function 0 = LED1 is not working in flash mode. 1 = LED1 is working in flash mode.	N/A
D[2]	FLED2_STAT	0	R	The Status of LED2 Flash Function 0 = LED2 is not working in flash mode. 1 = LED2 is working in flash mode.	N/A
D[1]	TLED1_STAT	0	R	The Status of LED1 Torch Function 0 = LED1 is not working in torch mode. 1 = LED1 is working in torch mode.	N/A
D[0]	TLED2_STAT	0	R	The Status of LED2 Torch Function 0 = LED2 is not working in torch mode. 1 = LED2 is working in torch mode.	N/A

REGISTER MAPS (continued)

REG0x88: LED_STAT2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FTIMEOUT1_STAT	0	R	LED1 Flash Timeout Fault Status Bit 0 = LED1 flash duration is below timeout counter. 1 = LED1 flash timeout is occurring.	N/A
D[6]	FTIMEOUT2_STAT	0	R	LED2 Flash Timeout Fault Status Bit 0 = LED2 flash duration is below timeout counter. 1 = LED2 flash timeout is occurring.	N/A
D[5]	FLASH_FLED_OVP_STAT	0	R	FLASH_VDD Over-Voltage Fault Status Bit 0 = FLASH voltage is below OVP threshold. 1 = FLASH voltage is over OVP threshold.	N/A
D[4]	LED1_SHORT_STAT	0	R	LED1 Short Circuit Fault Status Bit 0 = LED1 is not shorting to ground. 1 = LED1 is shorting to ground.	N/A
D[3]	LED2_SHORT_STAT	0	R	LED2 Short Circuit Fault Status Bit 0 = LED2 is not shorting to ground. 1 = LED2 is shorting to ground.	N/A
D[2]	TORCH_VDD_UVP_STAT	0	R	TORCH_VDD Under-Voltage Fault Status Bit 0 = TORCH_VDD voltage is equal or over 2V. 1 = TORCH_VDD voltage is below 2V.	N/A
D[1]	TORCH_VDD_OVP_STAT	0	R	TORCH_VDD Over-Voltage Fault Status Bit 0 = TORCH_VDD voltage is below TORCH_VDD_OVP threshold. 1 = TORCH_VDD voltage is over TORCH_VDD_OVP threshold.	N/A
D[0]	VBAT_LED_LOW_STAT	0	R	Status Bit for VBAT Falling to Reset LED Flash Function Enable Bits 0 = VBAT voltage is over VBAT_MIN_FLED. 1 = VBAT voltage is below VBAT_MIN_FLED.	N/A

REGISTER MAPS (continued)

REG0x89: LED_FLAG Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FTIMEOUT1_FLAG	0	RC	LED1 Flash Timeout Fault Flag Bit 0 = No LED1 flash timeout fault 1 = LED1 flash timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[6]	FTIMEOUT2_FLAG	0	RC	LED2 Flash Timeout Fault Flag Bit 0 = No LED2 flash timeout fault 1 = LED2 flash timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[5]	FLASH_FLED_OVP_FLAG	0	RC	Flash Over-Voltage Fault Flag Bit 0 = No flash over-voltage fault 1 = Flash over-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	LED1_SHORT_FLAG	0	RC	LED1 Short Circuit Fault Flag Bit 0 = No LED1 short circuit fault 1 = LED1 short circuit fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3]	LED2_SHORT_FLAG	0	RC	LED2 Short Circuit Fault Flag Bit 0 = No LED2 short circuit fault 1 = LED2 short circuit fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[2]	TORCH_VDD_UVP_FLAG	0	RC	TORCH_VDD Under-Voltage Fault Flag Bit 0 = No TORCH_VDD under-voltage fault 1 = TORCH_VDD under-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[1]	TORCH_VDD_OVP_FLAG	0	RC	TORCH_VDD Over-Voltage Fault Flag Bit 0 = No TORCH_VDD over-voltage fault 1 = TORCH_VDD over-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	VBAT_LED_LOW_FLAG	0	RC	Flag Bit for VBAT Falling to Reset Flash Function Enable Bits 0 = No VBAT falling to reset flash function fault 1 = VBAT falling to reset flash function fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x8A: LED_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FTIMEOUT1_MASK	0	R/W	Mask LED1 Flash Timeout Fault Interrupt 0 = LED1 flash timeout fault interrupt can work. (default) 1 = Mask LED1 flash timeout fault interrupt. FTIMEOUT1_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	FTIMEOUT2_MASK	0	R/W	Mask LED2 Flash Timeout Fault Interrupt 0 = LED2 flash timeout fault interrupt can work. (default) 1 = Mask LED2 flash timeout fault interrupt. FTIMEOUT2_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	FLASH_FLED_OVP_MASK	0	R/W	Mask Flash Over-Voltage Fault Interrupt 0 = Flash over-voltage fault interrupt can work. (default) 1 = Mask flash over-voltage fault interrupt. FLASH_FLED_ OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	LED1_SHORT_MASK	0	R/W	Mask LED1 Short Circuit Fault Interrupt 0 = LED1 short circuit fault interrupt can work (default) 1 = Mask LED1 short circuit fault interrupt. LED1_SHORT_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	LED2_SHORT_MASK	0	R/W	Mask LED2 Short Circuit Fault Interrupt 0 = LED2 short circuit fault interrupt can work. (default) 1 = Mask LED2 short circuit fault interrupt. LED2_SHORT_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	TORCH_VDD_UVP_MASK	0	R/W	Mask TORCH_VDD Under-Voltage Fault Interrupt 0 = TORCH_VDD under-voltage fault interrupt can work. (default) 1 = Mask TORCH_VDD under-voltage fault interrupt. TORCH_ VDD_UVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	TORCH_VDD_OVP_MASK	0	R/W	Mask TORCH_VDD Over-Voltage Fault Interrupt 0 = TORCH_VDD over-voltage fault interrupt can work. (default) 1 = Mask TORCH_VDD over-voltage fault interrupt. TORCH_ VDD_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	VBAT_LED_LOW_MASK	0	R/W	Mask VBAT Falling to Reset Flash Function Fault Interrupt 0 = VBAT falling to reset flash function fault interrupt can work. (default) 1 = Mask VBAT falling to reset flash function fault interrupt. VBAT_LED_LOW_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x8B: RESERVED Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x8C: LED_EXT_CTRL Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TORCH_STEP_CTRL	0	R/W	Change the Torch step for TLED1_BR_CTR and TLED2_BR_CTR register. 0 = 12.5mA (default) 1 = 1.5625mA	REG_RST
D[6]	LED_EN	0	R/W	LED Block Enable Bit 0 = LED block is shutdown (default) 1 = Enable the LED block, and STAT and FLAG are active.	REG_RST WDT_RST
D[5:4]	Reserved	00	R	Reserved	N/A
D[3]	FLASH_OVER_TORCH_STAT	0	R	Status Bit for FLASH_VDD Greater than TORCH_VDD 0 = FLASH_VDD voltage is not greater than TORCH_VDD 1 = FLASH_VDD voltage is greater than TORCH_VDD	N/A
D[2]	FLASH_VDD_UVP_STAT	0	R	FLASH_VDD Under-Voltage Status Bit 0 = FLASH_VDD voltage is equal or over 2.5V 1 = FLASH_VDD voltage is below 2.5V	N/A
D[1]	FLASH_VDD_UVP_FLAG	0	RC	FLASH_VDD Under-Voltage Fault Flag Bit 0 = No FLASH_VDD under-voltage fault 1 = FLASH_VDD under-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[0]	FLASH_VDD_UVP_MASK	1	R/W	Mask FLASH_VDD Under-Voltage Fault Interrupt 0 = FLASH_VDD under-voltage fault interrupt can work (default) 1 = Mask FLASH_VDD under-voltage fault interrupt. FLASH_VDD_UVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

APPLICATION INFORMATION

Design Requirements

This design requires the smart wall adapter to provide the SGM41620 with the appropriate input voltage and input current based on the USB_PD programmable power supply (PD PPS) voltage steps and current steps. The SGM41620 is capable of charging up to 8A in voltage divider mode, but this may not be practical for some applications due to the total power loss at this operating point. Thermal constraints, space constraints and operating conditions should be carefully considered to ensure acceptable performance.

Inductor Design

Small energy storage elements (inductor and capacitor) can be used since the high frequency (1.5MHz) switching converter is used in the SGM41620. Inductor should tolerate current which is higher than the maximum charge current (I_{CHG}) when enable Buck charger plus half the inductor peak to peak ripple current (ΔI) without saturation:

$$I_{SAT} > I_{CHG} + \frac{\Delta I}{2} \quad (12)$$

The inductor ripple current is determined by the input voltage (V_{VBUS}), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (f_{SW_BUCK} = 1.5MHz) and the inductance (L). In CCM:

$$\Delta I = \frac{V_{VBUS} \times D \times (1-D)}{f_{SW\_BUCK} \times L} \quad (13)$$

Inductor ripple current is maximum when D ≈ 0.5. In the practical designs, inductor peak to peak current ripple is selected in a range from 20% to 40% of the maximum DC current ΔI = (0.2 ~ 0.4) × I_{CHG} for a good trade-off between inductor size and efficiency. Selecting the higher ripple allows choosing of smaller inductance.

For each application, V_{VBUS} and I_{CHG} are known, so L can be calculated from Equation 13 and current rating of the inductor can be selected from Equation 12. Choose an inductor that has small DCR and core losses at 1.5MHz to have high efficiency and cool operation at full load.

Input Capacitors (C_{VAC}, C_{VBUS}, C_{PMID_CP} and C_{PMID_BUCK})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For $C_{VAC,}$ use at least a 1μF/25V low ESR bypass ceramic capacitor placed close to the VAC and PGND pins. The C_{VBUS} and C_{PMID} are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, 10μF/25V or larger X5R ceramic capacitors are sufficient for C_{PMID_BUCK} or C_{PMID_CP}, 1μF/25V or larger X5R ceramic capacitors are sufficient for C_{VBUS}. Considering the DC bias derating of the ceramic capacitors, the X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFET (Q_{OVP})

The maximum recommended V_{VBUS} input range is 13.5V. If the supplied VAC voltage is above 13.5V, or if regulation functions are needed during load or wall adapter transients, an external OVPFET is recommended between the USB connector and the SGM41620. Choose a low R_{DSON} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors (C_{FLY})

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to half of the input voltage. To trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of the V_{BAT} as a good starting point. The C_{FLY} for each channel can be calculated by Equation 14:

$$C_{FLY} = \frac{I_{BAT}}{4 f_{SW} V_{CFLY\_RPP}} = \frac{I_{BAT}}{8\% f_{SW} V_{OUT}} \quad (14)$$

where I_{BAT} is the charging current when enable switched capacitor charger and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

The default switching frequency is f_{SW} = 700kHz. It can be adjusted by FSW_SET[2:0] bits in REG0x64. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}).

APPLICATION INFORMATION (continued)

When choosing the C_{FLY} capacitor, it is important to consider the current rating of the caps, their ESR, and the capacitance rating. Be sure to consider the bias voltage derating for the caps, as the CFLY caps are biased to half of the input voltage, and this will affect their effective capacitance. An optimal system will have three 22μF/10V caps per channel, for a total of 6 caps per device. It is possible to use fewer caps, with a minimum recommendation of 2. Using fewer caps will result in higher voltage and current ripple on the output, as well as lower efficiency.

Output Capacitor for Switched Capacitor Charger (C_{BAT})

C_{BAT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{BAT} value results in less output voltage ripple, but due to the dual-channel operation, the C_{BAT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{BAT} as given in Equation 15:

$$C_{BAT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{BAT\_RPP}} \quad (15)$$

where t_{DEAD} is the dead time between the two channels and V_{BAT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{BAT}.

C_{BAT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically two 10μF/10V, X5R or better grade ceramic capacitors placed close to the BAT and PGND pins provide stable performance.

Output Capacitor for Buck Charger (C_{SYS})

The output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{SYS} (C_{SYS} RMS current) can be calculated by:

$$I_{SYS} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (16)$$

And the system voltage ripple can be calculated by:

$$\Delta V_{SYS} = \frac{V_{SYS}}{8LC_{SYS}f_{SW\_BUCK}^{2}} \left(1 - \frac{V_{SYS}}{V_{VBUS}}\right) \quad (17)$$

Increasing L or C_{SYS} (the LC filter) can reduce the ripple.

The internal loop compensation of the device is optimized for > 20μF ceramic output capacitor. 10V, X7R (or X5R) ceramic capacitors are recommended for the output.

External Bootstrap Capacitor

The bootstrap capacitors provide the gate driver supply voltage for the internal high-side switches (Q_{CH1} and Q_{CH2}). Place two 100nF/10V low ESR ceramic capacitors between BST1/2 and CFH1/2 pins separately.

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41620. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VAC, VBUS, PMID_BUCK, PMID_CP, and BAT pins to PGND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. Connect or reference all quiet signals to the AGND pin.
7. Connect and reference all power signals to the PGND pins (preferably the nearest ones).
8. Try not to split the power planes by signal traces.

The reference layout is shown in Figure 18.

APPLICATION INFORMATION (continued)

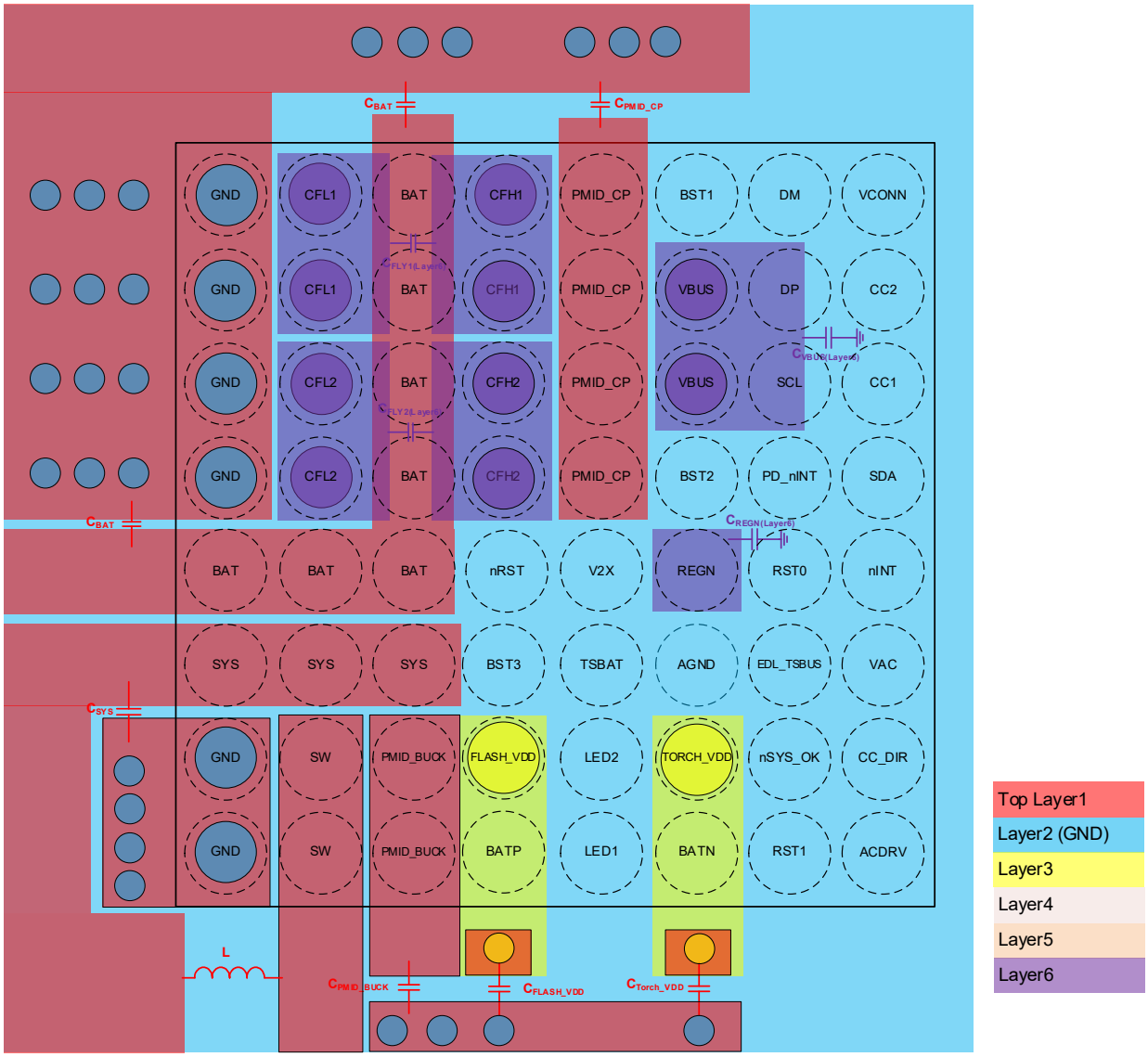


Figure 18. Reference Layout

REVISION HISTORY

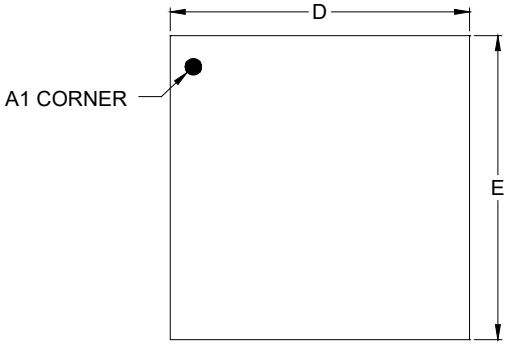
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MARCH 2026 – REV.A to REV.A.1	Page
Changed Pin Description section	7
Changed Detailed Description section	44
Changed Register Maps section	52, 65

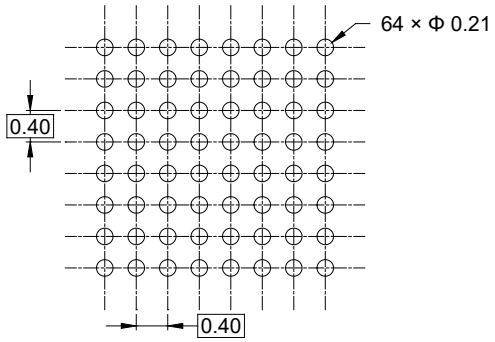
Changes from Original to REV.A (OCTOBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

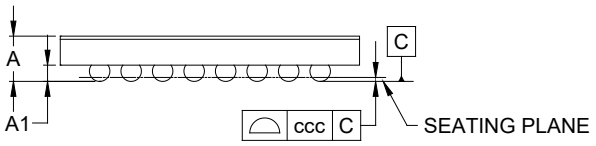
WLCSP-3.8×3.86-64B



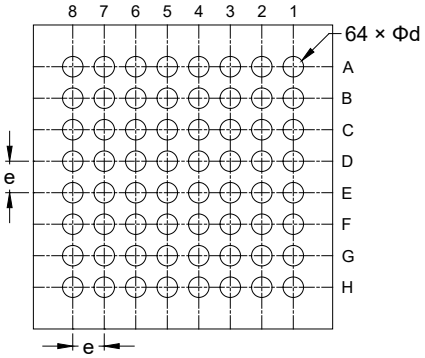
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



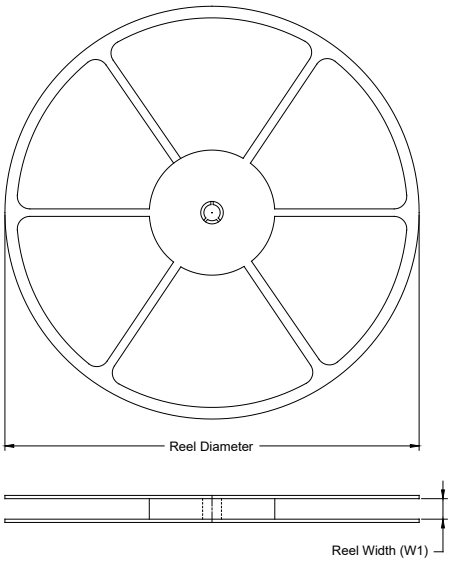
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.613
A1	0.186	-	0.226
D	3.770	-	3.830
E	3.830	-	3.890
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

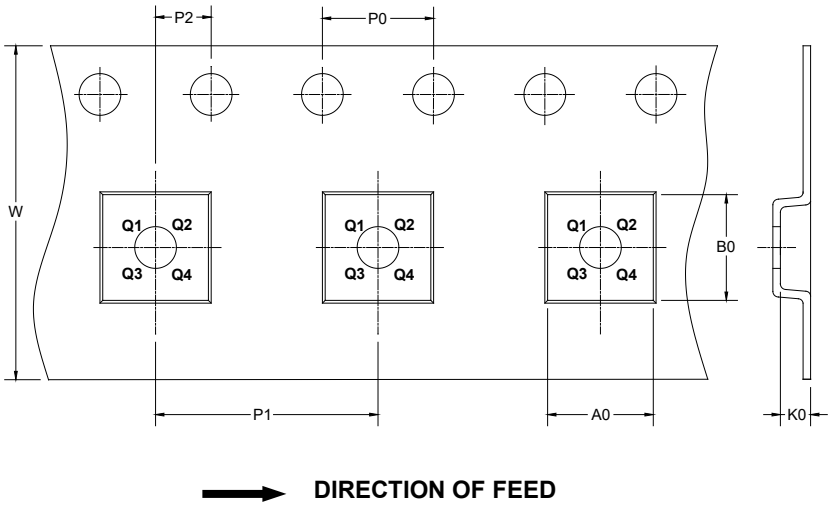
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



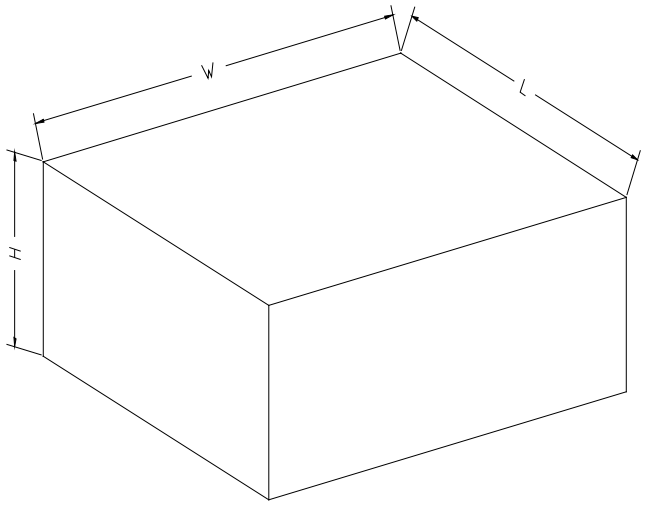
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.8×3.86-64B	7"	12.4	4.20	4.20	0.80	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002