SGM42404Q
Automotive Quad Channel Low-side Driver with Serial Interface Option

GENERAL DESCRIPTION

The SGM42404Q consists of four identical low-side drivers with over-current protection. It has inductive clamp circuit to discharge the inductive load energy when the output is turned off such as unipolar stepper motors, DC motors, relays, solenoids or other loads.

The SGM42404Q provides a serial interface, which can read/write the data register/control register (configuring the energizing time & PWM duty cycle) through the serial interface, and also can diagnose the open-load or over-current fault condition. Multiple devices can be daisy-chain connected together to save the microcontroller resource.

The device has multiple protection functions, including open-load detection, over-temperature shutdown, over-current and short-circuit protections. Fault conditions are indicated on the SDO/nFAULT pin.

The SGM42404Q is available in a Green TSSOP-16 (Exposed Pad) package.

APPLICATIONS

Digital Outputs
Relay and Solenoid Drivers
PLC and DCS Systems
Motor Control

FEATURES

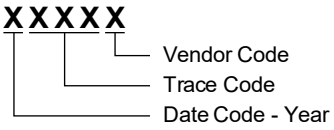
- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Supply Voltage Range: 5V to 50V**
- **Continuous Output Current:**
  - **2A (1-Channel On)**
  - **1A/Channel (4-Channel On)**
- **Integrated LDO Output**
- **Load Voltage Range: 5V to 48V**
- **Support SPI Mode or DIR Mode**
- **Reduces Power and Heat Dissipation**
  - **On-Resistance: 300mΩ/Channel (TYP)**
  - **Supply Current: 1.4mA (TYP)**
- **Robust Design Features**
  - **Each Channel with Independent Over-Current Protection and Open-Load Detection and Thermal Shutdown Protection**
  - **Data Output Can be Read Back for Reliable Verification**
  - **Short-Circuit Protection**
  - **Lighting Surge Protection**
  - **Electro-Static Discharge Protection**
- **nFAULT Indication:**
  - **Thermal Overload**
  - **Over-Current**
  - **Open-Load**
- **200kHz Switching Rates**
- **Support PWM Generation and Duty Cycle Settable**
- **±500V/42Ω, 8μs/20μs Surge Protection**
- **±8kV Contact and ±15kV Airgap ESD Protection**
- **16-Bit SPI for Diagnostics and Control**
- **Protection and Features Independent by Each Channel**
  - **Open-Load Detection Circuit in Output-Off State**
  - **3.2A Over-Current Protection (OCP) with 2A Current Foldback after TSD Event**
  - **Active Clamp Energy**
  - **Thermal Shutdown (TSD)**
- **SGM42404Q Available in a Green TSSOP-16 (Exposed Pad) Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42404Q	TSSOP-16 (Exposed Pad)	-40℃ to +125℃	SGM42404QPTS16G/TR	2LQPTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} ..... -0.3V to 55V
Input Voltage, V_{nDIR}, V_{EN}, V_{RESET} ..... -0.3V to 6V
Digital Input Voltage, IN1/nCS, IN2/SDI, IN3/RST_B, IN4/SCK ..... -0.3V to 6V
nFAULT/SDO (1) ..... -0.3V to 5.5V
OUT1, OUT2, OUT3, OUT4 to PGND ..... -0.3V to V_{CLAMP}
OUTx Load Current (Continues DC) 1A
Package Thermal Resistance
TSSOP-16 (Exposed Pad), θ_{JA} ..... 33.7℃/W
TSSOP-16 (Exposed Pad), θ_{JB} ..... 13.3℃/W
TSSOP-16 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 30.5℃/W
TSSOP-16 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 2.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±5000V
CDM ..... ±1000V

NOTES:
1. Recommended for use with 5V MCUs.
2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

V_{DD} ..... 5V to 50V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

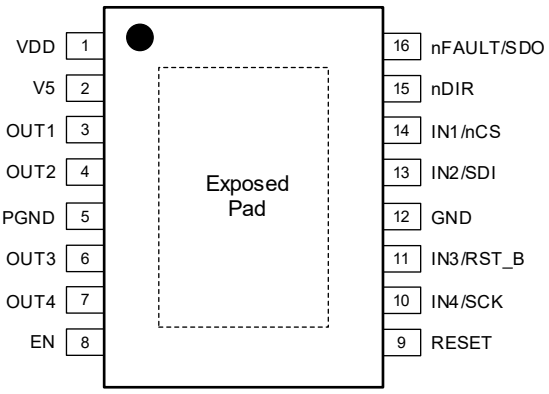
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM42404Q (TOP VIEW)



TSSOP-16 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
Power Supply		
1	VDD	Power Supply. Connect a 0.1μF bypass capacitor and a 10μF ceramic capacitor between VDD and GND pins.
5	PGND	Power Ground. Connect to exposed pad (EP).
12	GND	Analog Ground. Connect to exposed pad (EP).
Switch Control		
14	IN1/nCS	Switch 1 Control Logic Input/SPI Enable Input (nDIR = H). Internal pull-up when in SPI mode.
13	IN2/SDI	Switch 2 Control Logic Input/Serial Data Input (nDIR = H). Internal pull-down.
11	IN3/RST_B	Switch 3 Control Logic Input/Reset Terminal (nDIR = H). Internal pull-down.
10	IN4/SCK	Switch 4 Control Logic Input/Serial Clock (nDIR = H). Internal pull-down.
Switch Output		
3	OUT1	Low-side Switch 1 Output.
4	OUT2	Low-side Switch 2 Output.
6	OUT3	Low-side Switch 3 Output.
7	OUT4	Low-side Switch 4 Output.
Configuration		
15	nDIR	nDIR = L, DIR mode. nDIR = H, SPI mode.
8	EN	Enable Input Pin. A high DC signal on this pin will enable the device, internal pull-down.
9	RESET	Reset Input Pin. Logic high resets internal logic and over-current protection, internal pull-down.
Diagnostics Signaling		
16	nFAULT/SDO	Global Overload Open-Drain Output/Serial Data Output Terminal (nDIR = H). It is a fault flag pin when DIR = mode. This pin is pulled low when over-temperature, over-current or open-load occurs. Connect a pull-up resistor to logic voltage. (nDIR = L).
2	V5	5V LDO Output. Connect a 0.1μF bypass capacitor to GND.
Exposed Pad	-	Exposed Pad. Connect with Ground.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 5V to 50V, typical values are at T_A = +25℃ and V_{DD} = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Linear Regulator (VDD)						
V_{DD} Supply Voltage Range	V_{DD}		5		50	V
V_{DD} Supply Current	I_{DD}	V_5 = no load		1.4	3	mA
Sleep Current	I_{SLEEP}	EN = low			1	μA
V_5 Regulator Output Voltage	V_5	0mA to 20mA external load current	4.55	5	5.45	V
V_5 Regulator Current Limit		7V ≤ V_{DD} ≤ 50V	20	31	42	mA
V_5 Line Regulation		7V ≤ V_{DD} ≤ 50V, I_{V5} = 20mA, C_{LOAD} = 100nF		2	40	mV
V_5 Load Regulation		V_{DD} = 24V, 0mA ≤ I_{V5} ≤ 20mA, C_{LOAD} = 100nF		45	80	mV
Switch Outputs (OUTx)						
On-Resistance	R_{DSON}	I_{OUTx} = 600mA		300	600	mΩ
Inductive Clamp Voltage (1)	V_{CLAMP}	OUTx is off, I_{OUTx} = 500mA	46	51	56	V
Off-State Leakage Current at OUTx	I_{LEAK}	INx = low, V_{OUTx} = 0V to 45V	-15		15	μA
Switch Turn-Off Propagation Delay	t_{OFF}	INx to OUTx, low to high		280	400	ns
Switch Turn-On Propagation Delay	t_{ON}	INx to OUTx, high to low		80	130	ns
Output Fall Time	t_F	V_{DD} = 24V, 48Ω resistive load		200		ns
Current Limit	I_{LIM}		2.3	3.2	4.2	A
Logic Inputs (INx)						
Input Voltage High	V_{IH}		2			V
Input Voltage Low	V_{IL}				0.8	V
Input Threshold Hysteresis	V_{I_TH}			0.3		V
Input Pull-Down Resistor	$R_{PULL-DOWN}$	All logic input pins		210		kΩ
RESET Pulse Width	t_{RESET}			38		μs
Input Pin						
Low-Level Input Current 1 (RST_B, nDIR, IN1 to IN4, SCK, SDI)	I_{INL1}	V_{RST_B}, V_{nDIR}, V_{IN1} to V_{IN4}, V_{SCK}, V_{SDI} = 0V	-1		1	μA
Low-Level Input Current 2 (nCS)	I_{INL2}	V_{nCS} = 0V, V_{nDIR} = 5V	-40	-16	-5	μA
Low-Level Input Current 3 (nCS)	I_{INL3}	V_{nCS} = 0V, V_{nDIR} = 0V	-1		1	μA
High-Level Input Current 1 (RST_B, nDIR, IN1 to IN4, SCK, SDI)	I_{INH1}	V_{RST_B}, V_{nDIR}, V_{IN1} to V_{IN4}, V_{SCK}, V_{SDI} = 5V	10	25	50	μA
High-Level Input Current 2 (nCS)	I_{INH2}	V_{nCS} = 5V, V_{nDIR} = 5V	-10		10	μA
High-Level Input Current 3 (nCS)	I_{INH3}	V_{nCS} = 5V, V_{nDIR} = 0V	10	25	50	μA
Serial Output						
Low-Level Output Voltage	V_{SDOL}	I_{SDO} = 1mA		0.2	0.5	V
High-Level Output Voltage	V_{SDOH}	I_{SDO} = -1mA	4.3	4.8		V
Serial Output Leakage Current	I_{SDO_OFF}		-6		6	μA
Logic Output (nFAULT)						
Output Logic Low	V_{OL}	I_{LOAD} = 5mA		0.2	0.5	V
Three-State Leakage	I_{LKG}	Open-drain output off, V_{PULLUP} = 5V (2)	-6		6	μA

NOTES:
1. Not production tested. By characterization only.
2. Current into the device is positive and current out of the device is negative.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, V_{DD} = 5V to 50V, typical values are at T_A = +25℃ and V_{DD} = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Open-Load Detection						
Open-Load Release Voltage	V_{OL_R}		1.1	1.5	1.9	V
Open-Load Detection Voltage	V_{OL_D}	V_{INx} = 0V, V_{nDIR} = 0V	0.9	1.2	1.5	V
Thermal Protection						
Thermal Shutdown	T_{SD}	Temperature rising		160		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

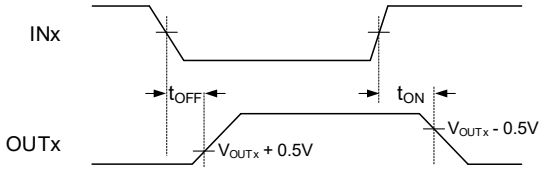


Figure 1. INx to OUTx Propagation Times

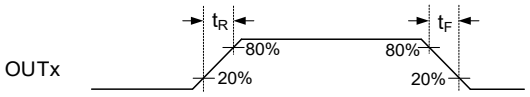


Figure 2. Output Channel Rise and Fall Times

POWER SOURCE ON/OFF SEQUENCE

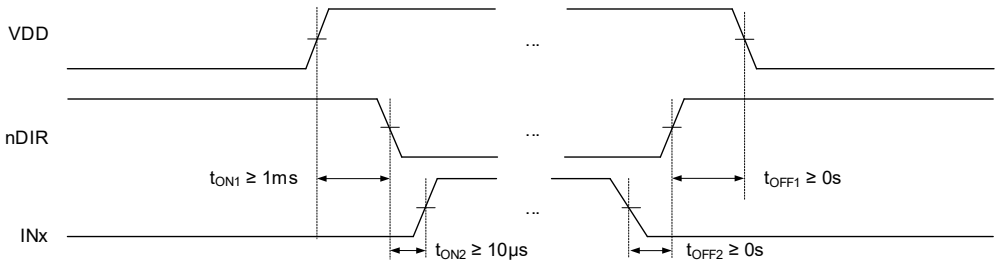


Figure 3. Power Source On/Off Sequence (DIR Mode)

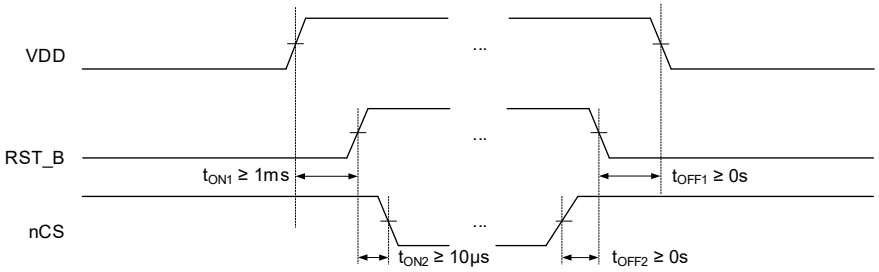
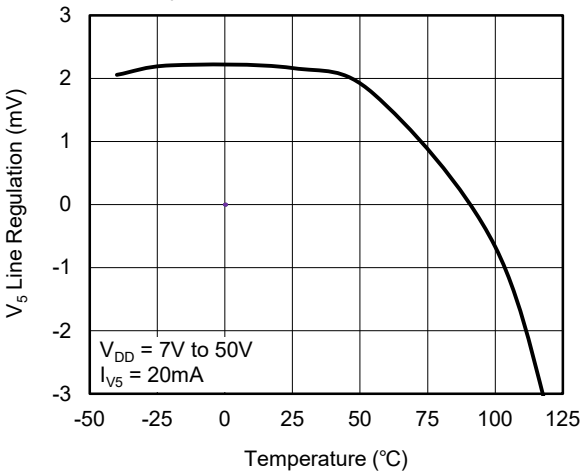


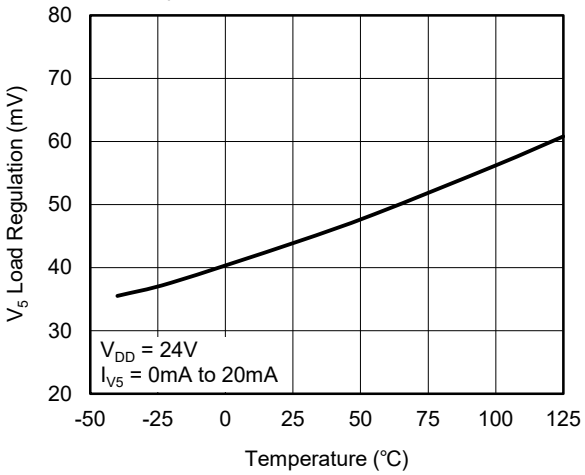
Figure 4. Power Source On/Off Sequence (SPI Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

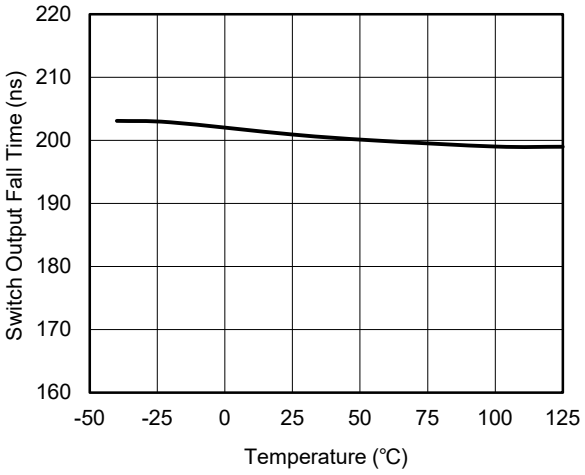
V_5 Line Regulation vs. Temperature



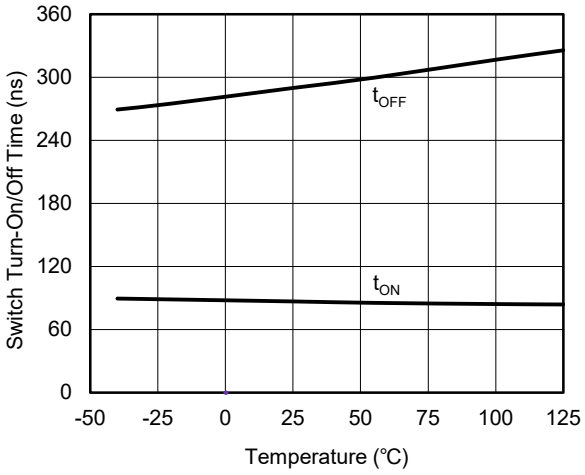
V_5 Load Regulation vs. Temperature



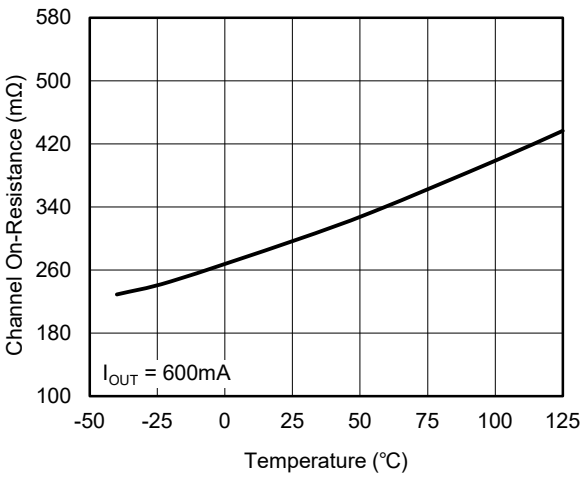
Switch Output Fall Time vs. Temperature



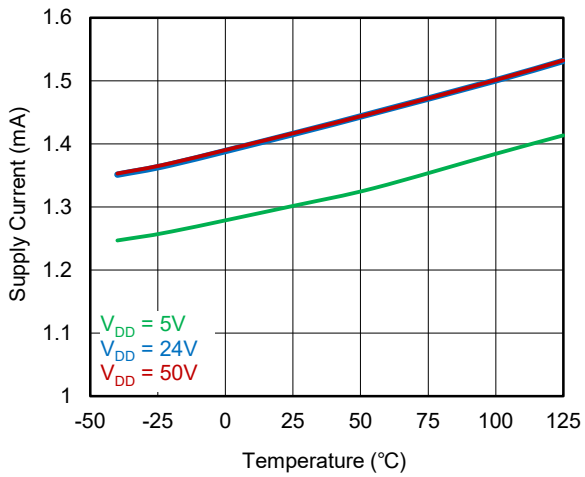
Switch Turn-On/Off Time vs. Temperature



Channel On-Resistance vs. Temperature



Supply Current vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

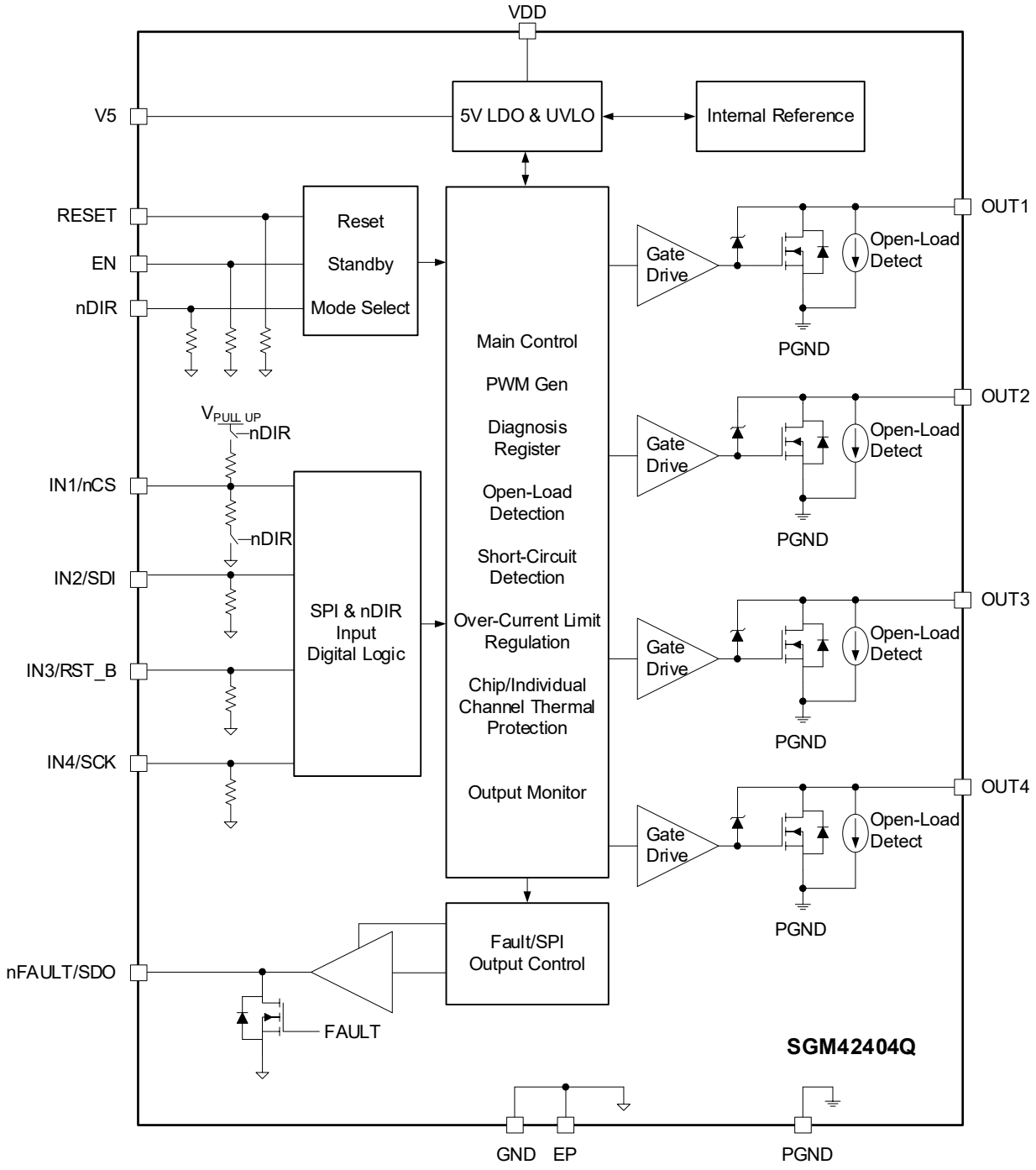


Figure 5. SGM42404Q Block Diagram

TYPICAL APPLICATION

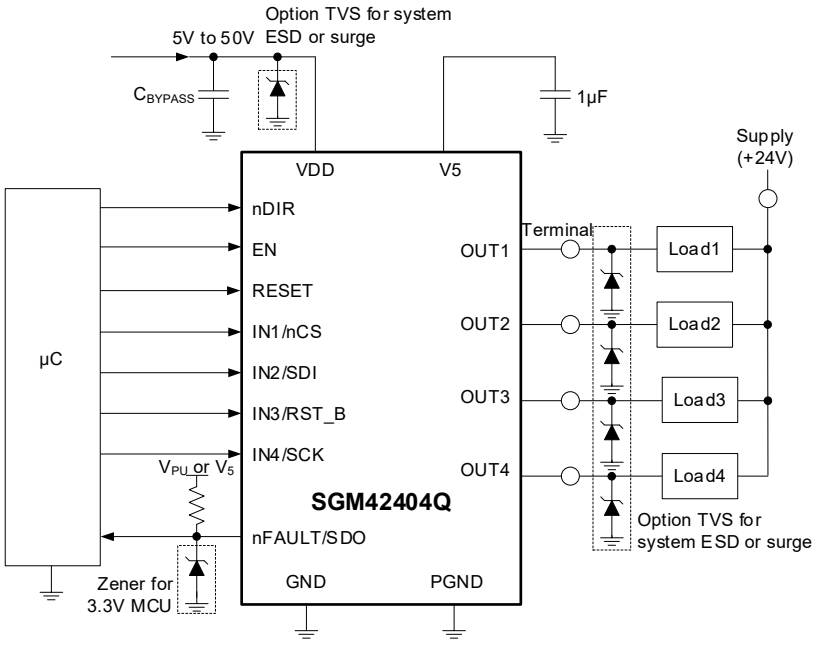


Figure 6. Typical Application Circuits

EN and RESET Operation

The EN pin is active-high and is pulled down internally.

The RESET pin is active-high. If RESET pin is pulled to high, the internal logic is reset, outputs are turned off, and input control signal on INx pin is ignored. RESET pin is pulled down internally.

DIR MODE

DIR (Direct) Mode

Transition to direct mode is brought about by switching nDIR terminal to low.
Output controlled for each input is shown below.
Further, SPI input and RST_B input are not accepted during direct mode.

INPUT PIN	CONTROLLED OUTPUT
IN1/nCS	OUT1
IN2/SDI	OUT2
IN3/RST_B	OUT3
IN4/SCK	OUT4

DIR (Direct) Mode Timing Chart (1)

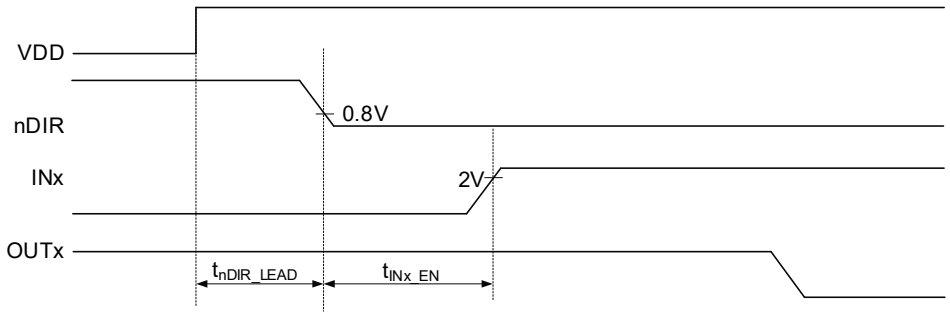
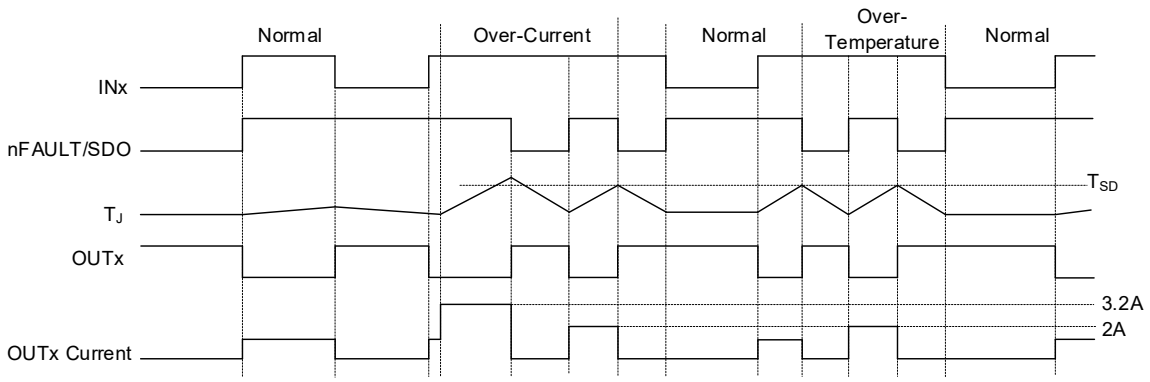


Figure 7. DIR Mode Timing (a)

ITEM	SYMBOL	MIN	TYP	MAX	UNITS
nDIR Lead Time (1)	t_{nDIR_LEAD}	1			ms
INx Enable Time (1)	t_{INx_EN}	10			μs

NOTE: 1. Not 100% tested.



NOTE: Current limit = 3.2A, REP_OC = low

Figure 8. DIR Mode Timing (b)

SPI MODE

An SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the SGM42404Q device. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16-bit word, with an 8-bit command and 8-bit of data. The SPI output data (SDO) word consists of the fault status indication bits and then the register data being accessed for read commands or the existing data for write commands.

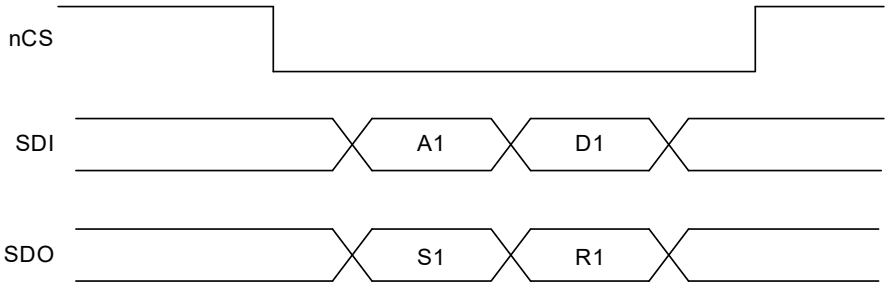


Figure 9. SPI Mode

A valid frame must meet the following conditions:

- The SCK pin should be low when the nCS pin transitions from high to low and from low to high.
- The nCS pin should be pulled high between words.
- When the nCS pin is pulled high, any signals at the SCK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCK and data is propagated on the rising edge of SCK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error (SCLK_FLT) occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin follow the 8 bits command data.
- When performing a read action, D1 is ignored.

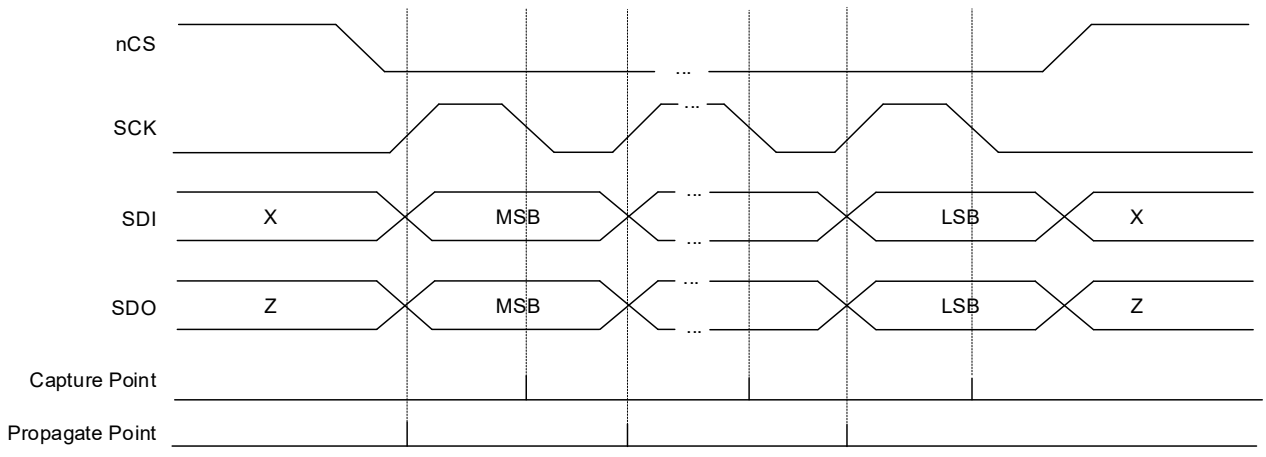


Figure 10. SPI Mode Chart

SPI MODE (continued)

SPI Format

Two SPI data frame formats are accepted. One is for single device communication and another is for multiple devices communication. The format is determined by the MSB bit C[0] received via SDI.

Single Device Communication

The input data SDI is 16 bits long and the format is as follow:

- bit[15]: Chained communication bit, C[0]
- bit[14]: Read/Write bit, R/W[0]
- bit[13:8]: Register address, A[5:0]
- bit[7:0]: Data, D[7:0]

The SDI input half-word start with C[0] = 0 that indicates single device communication. The following R/W bit, R/W[0], indicates read or write action. R/W[0] = 0 is a write command and R/W[0] = 1 is a read command. The register address A[5:0] and data D[7:0] follow after.

The SDO output data half-word is 16 bits long. Starting from MSB, bit[15:14] = 11, followed by 6 bits IC status and 8 bits response data. For a write command (R[0] = 0), the response data is the existing data in the register being written to. For a read command (R[0] = 1), the response data is the content currently in the register being read.

SPI Write

SDI

Field	C	R/W	Address						Data In							
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Data	0	0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

SDO

Field			Global Status						Data Out							
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Data	1	1	FAULT	SCLK_FLT	OL	UV	OC	OT	D7	D6	D5	D4	D3	D2	D1	D0

SPI Read

SDI

Field	C	R/W	Address						Data In							
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Data	0	1	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

SDO

Field			Global Status						Data Out							
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Data	1	1	FAULT	SCLK_FLT	OL	UV	OC	OT	D7	D6	D5	D4	D3	D2	D1	D0

- FAULT: it indicates any one of the OUT switches is current overload, thermal overload, open-load, or the chip is in thermal shutdown. If FAULT_LAT = 0, it observes real time error (IC_STAT1). If FAULT_LAT = 1, it observes latched error (IC_STAT2). Note that direct mode fault pin output logic is the same as this FAULT bit.
- SCLK_FLT: it indicates frame error including invalid address, parity bit error and wrong clock count (i.e. Single device is not 16 and multiple-device (n) is not 16 × (n+1)) in SPI mode only.
- OL: it indicates any one of the OUT switches is in open-load condition. It is the ORed logic of OLx bits in both IC_STAT1 and IC_STAT2.
- UV: V5 voltage is in under-voltage condition.
- OC: it indicates any one of the OUT switches is in over-current condition. It is the ORed logic of OCx bits in both IC_STAT1 and IC_STAT2.
- OT: it indicates any one of the OUT switches or chip is in over-temperature condition (thermal overload). It is the ORed logic of TSDx bits in IC_STAT1 and IC_STAT2 and chip internal OT bit.

SPI MODE (continued)

SPI Interface for Multiple Slaves

Multiple devices can be connected to the master controller with and without the daisy chain. In order to connect 'n' devices to the main controller without using daisy chains, 'n' I/O sources from the main controller must be utilized for the nCS pins. Whereas, if the daisy chain configuration is used, then a single nCS line can be used for connecting multiple devices.

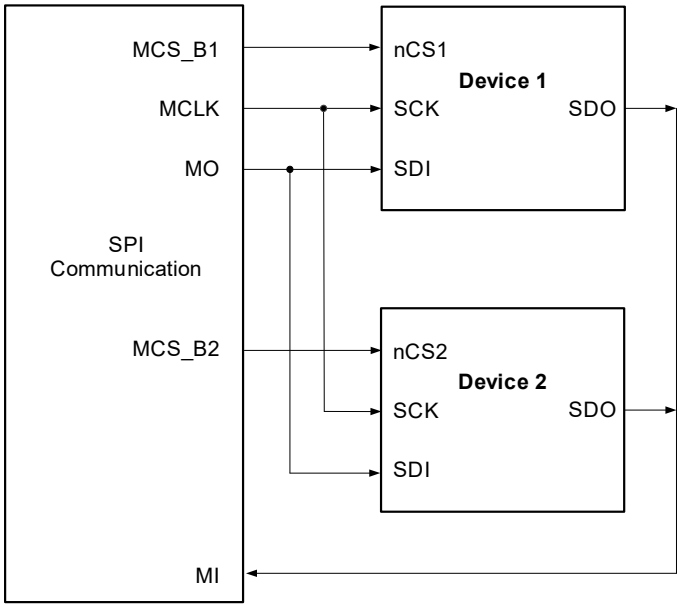


Figure 11. Operation without Daisy Chain

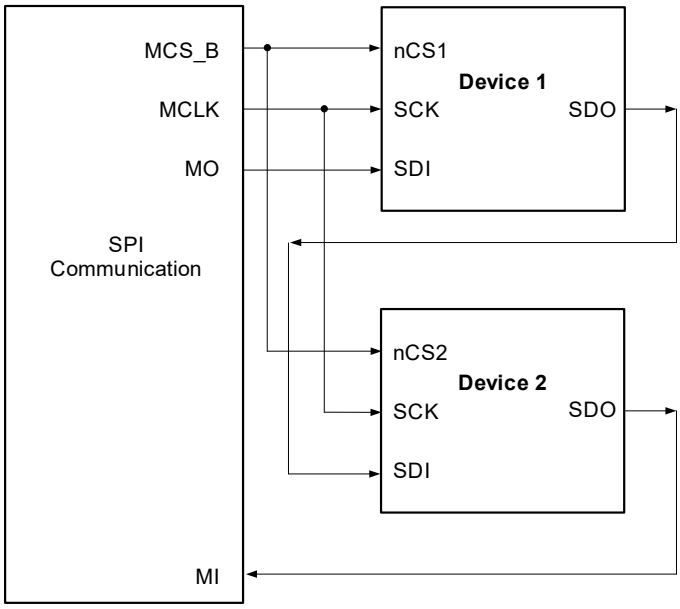


Figure 12. SPI Operation with Daisy Chain

SPI MODE (continued)

SPI Interface for Multiple Slaves in Daisy Chain

The device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU.

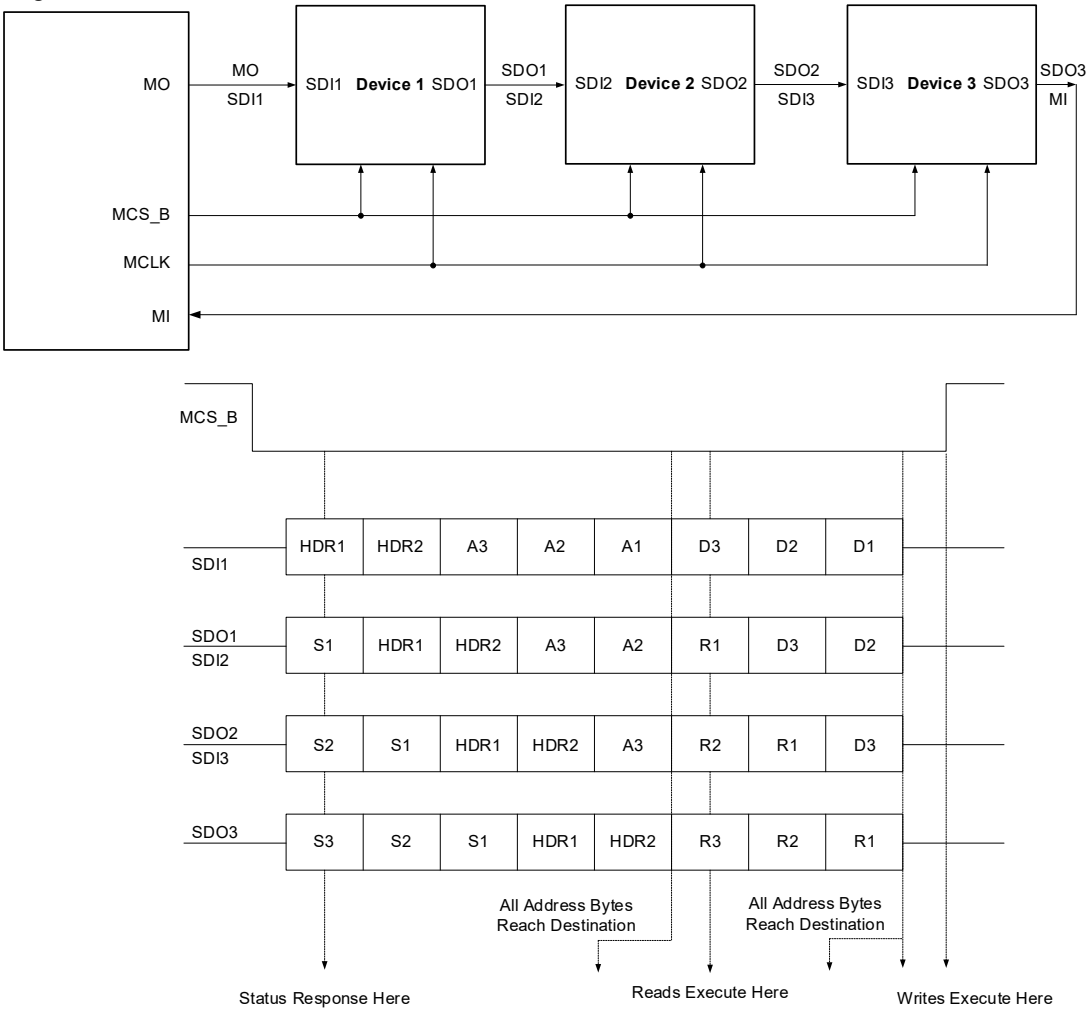


Figure 13. Multiple Slaves in Daisy Chain

The first device in the chain shown above receives data from the master controller in the following format.

- 2 bytes of header
- 3 bytes of address
- 3 bytes of data

After the data has been transmitted through the chain, the master controller receives it in the following format.

- 3 bytes of status
- 2 bytes of header (should be identical to the information controller sent)
- 3 bytes of report

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nCS) signal. N5 through N0 are 6 bits dedicated to show the number of device in the chain. Up to 63 devices can be connected in series per daisy chain connection.

SPI MODE (continued)

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

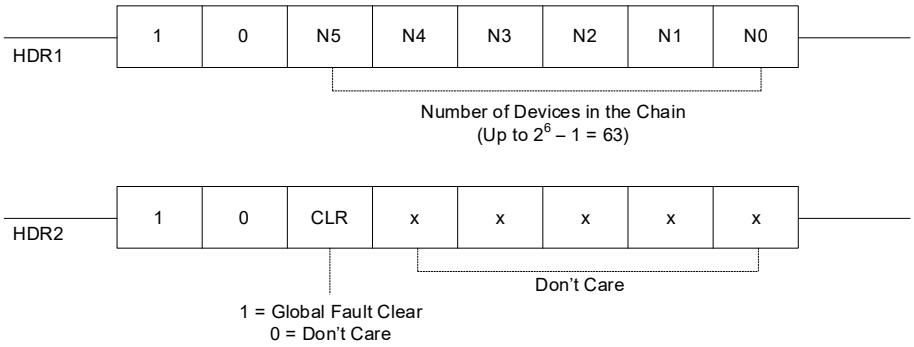


Figure 14. Daisy Chain Head Format

The status byte provides information about the fault status register for each device in the daisy chain. That way the master controller does not have to initiate a read command to read the fault status from any particular device. This saves the controller additional read commands and makes the system more efficient to determine fault conditions flagged in a device.

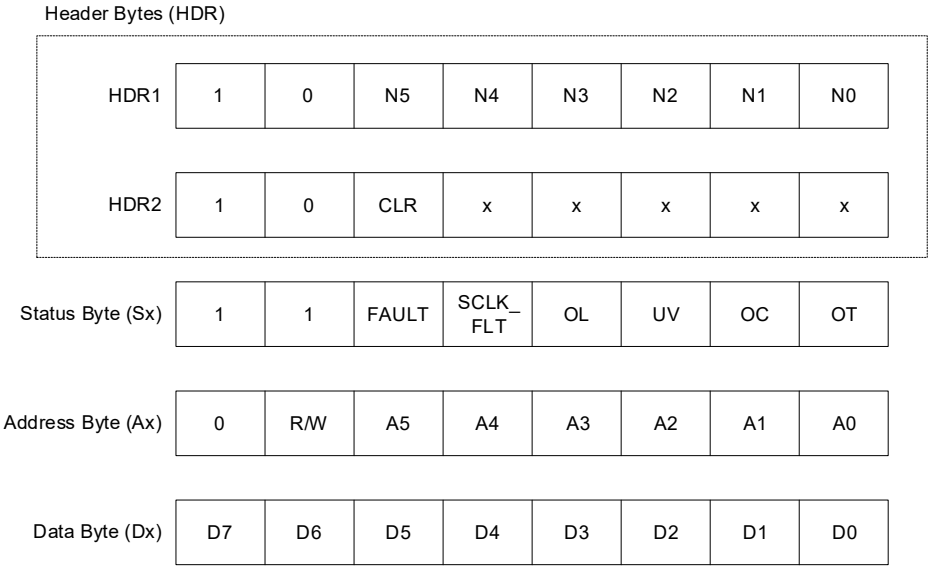


Figure 15. Daisy Chain Data Format

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives following by the first header byte. For example, in this 3 device configuration, device 2 in the chain will receive two status bytes before receiving HDR1 byte, followed by HDR2 byte. From the two Status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a single device connection. The report bytes (R1 through R3), as shown in the figure above, is the content of the register being accessed.

SPI MODE (continued)

SPI RST_B Releasing Sequence

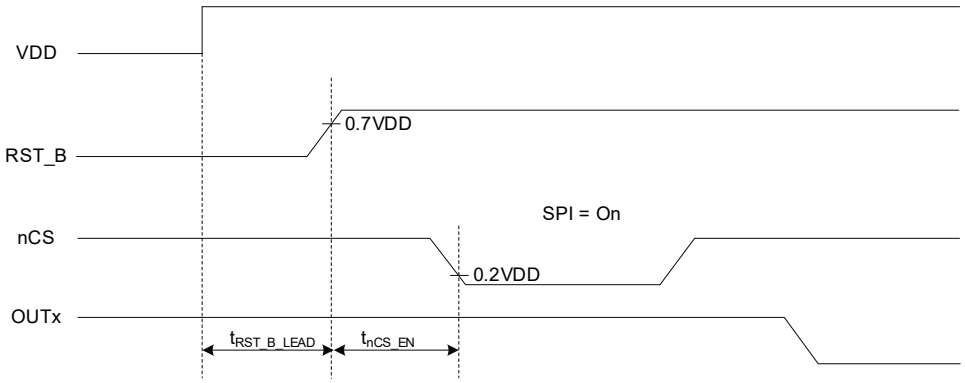


Figure 16. RST_B Releasing Sequence

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RST_B Lead Time (1) (2)	$t_{RST_B_LEAD}$	1			ms
nCS Enable Time (1)	t_{nCS_EN}	10			μs

NOTES:

1. Not 100% tested.
2. RST_B L time and H time must be over 10μs.

SPI Timing Chart

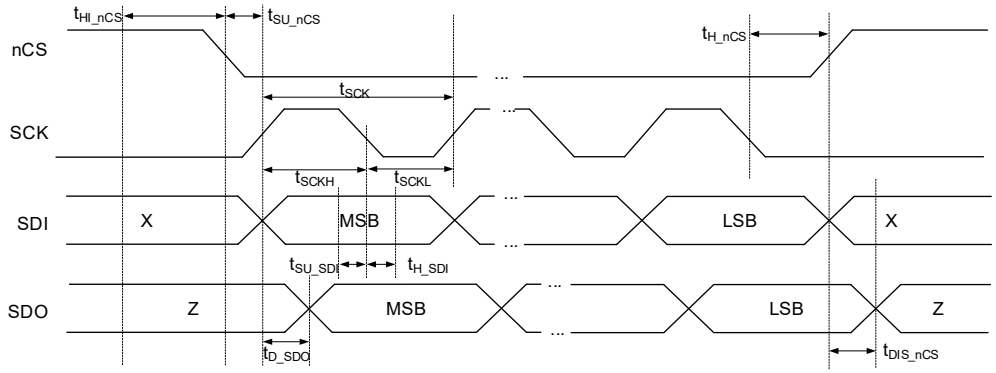


Figure 17. SPI Timing Chart

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCK Minimum Period	t_{SCK}	200			ns
SCK High Time	t_{SCKH}	100			ns
SCK Low Time	t_{SCKL}	100			ns
SDI Input Data Setup Time	t_{SU_SDI}	50			ns
SDI Input Data Hold Time	t_{H_SDI}	50			ns
SDO Output Data Delay Time, C_L = 20pF	t_{D_SDO}			65	ns
nCS Input Setup Time	t_{SU_nCS}	50			ns
nCS Input Hold Time	t_{H_nCS}	50			ns
nCS Minimum High Time	t_{HI_nCS}	900			ns
Enable Delay Time, nCS Low to SDO Active	t_{EN_nCS}			100	ns
Disable Delay Time, nCS high to SDO Hi-Z	t_{DIS_nCS}			100	ns

REGISTER MAPS

The registers provide variety of feedback information and configuration options.

These include specific fault diagnostics, general device configurations, driver configurations, fault and diagnostic configurations, and amplifier configurations. Additionally, the advanced register maps provide advanced driver functions to assist in certain system conditions, but not required for standard operation of the device.

To assist with software development and reuse, the register maps share an overlapping register structure with differences for specific device properties. The primary differences between the two device register maps are outlined below.

Table 1. Memory Map

ADDRESS	NAME	TYPE	BITS							
			BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]
00h	IC_STAT1	R	OL4	OC/TSD4	OL3	OC/TSD3	OL2	OC/TSD2	OL1	OC/TSD1
01h	IC_STAT2	R	IC_STAT_LAT							
09h	REPO_DRV	R/W	REP_OC	FAULT_LAT	RESERVED					
0Ah	CH_CTRL1	R/W	CTRL_CH4		CTRL_CH3		CTRL_CH2		CTRL_CH1	
12h	CH_ENG1	R/W	ENER_CH1			ENER_TIME_CH1				PARITY_ENG1
13h	CH_ENG2	R/W	ENER_CH2			ENER_TIME_CH2				PARITY_ENG2
14h	CH_ENG3	R/W	ENER_CH3			ENER_TIME_CH3				PARITY_ENG3
15h	CH_ENG4	R/W	ENER_CH4			ENER_TIME_CH4				PARITY_ENG4
1Ah	CH_FRDT1	R/W	FREQ_CH1			DUTY_CH1				PARITY_FRDT1
1Bh	CH_FRDT2	R/W	FREQ_CH2			DUTY_CH2				PARITY_FRDT2
1Ch	CH_FRDT3	R/W	FREQ_CH3			DUTY_CH3				PARITY_FRDT3
1Dh	CH_FRDT4	R/W	FREQ_CH4			DUTY_CH4				PARITY_FRDT4

NOTE: Odd parity check calculation includes register address and bit[7:1].

REGISTER MAPS (continued)

FIELD	BITS	DATA	STATE
OLx	D[7], D[5], D[3], D[1]	0	Normal operation
		1	Load open
OC/TSDx	D[6], D[4], D[2], D[0]	0	Normal operation
		1	OCP or TSD

REG0x00: IC_STAT1 Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	OL4	0	R	Indicate Channel 4 Open-Load Condition. 0 = Normal operation (default) 1 = Open-load condition detected
D[6]	OC/TSD4	0	R	Indicate Channel 4 OCP or TSD Condition. 0 = Normal operation (default) 1 = OCP or TSD detected
D[5]	OL3	0	R	Indicate Channel 3 Open-Load Condition. 0 = Normal operation (default) 1 = Open-load condition detected
D[4]	OC/TSD3	0	R	Indicate Channel 3 OCP or TSD Condition. 0 = Normal operation (default) 1 = OCP or TSD detected
D[3]	OL2	0	R	Indicate Channel 2 Open-Load Condition. 0 = Normal operation (default) 1 = Open-load condition detected
D[2]	OC/TSD2	0	R	Indicate Channel 2 OCP or TSD Condition. 0 = Normal operation (default) 1 = OCP or TSD detected
D[1]	OL1	0	R	Indicate Channel 1 Open-Load Condition. 0 = Normal operation (default) 1 = Open-load condition detected
D[0]	OC/TSD1	0	R	Indicate Channel 1 OCP or TSD Condition. 0 = Normal operation (default) 1 = OCP or TSD detected

REG0x01: IC_STAT2 Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IC_STAT_LAT	0000 0000	R	Channel latched OC, OL, OT errors. It indicates the channel was in OC, OL or OT status before. Cleared by read once or daisy chain CLR.

This register indicated the channel was in open-load, OCP or TSD. It is also designed for reading the fault information occurred in previous DIR mode operation status.

REG0x09: REPO_DRV Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	REP_OC	0	R/W	Configure Real-Time (FAULT_LAT = 0) Over-Current Reporting. 0 = OC reporting disabled (default) 1 = OC reporting enabled
D[6]	FAULT_LAT	0	R/W	Configure FAULT Logic in Status Byte (SPI mode) or FAULT Pin Logic (DIR Mode). 0 = Observe real-time error (IC_STAT1) (default) 1 = Observe latched error (IC_STAT2)
D[5:0]	RESERVED	00 0000	R/W	Reserved. Only write 6'h00 to this field. May cause unexpected behavior otherwise.

This register cannot be cleared during operation. It resets during power up or enabling the chip.

REGISTER MAPS (continued)

Bits	CHx	Output and Protection Circuit Status			
		Output	OCP	TSD	OLD
D[7:6], D[5:4], D[3:2], D[1:0]	00	Off	Disable	Disable	Disable
	01	NA	NA	NA	NA
	10	On	Enable	Enable	Disable
	11	Off	Disable	Disable	Enable

REG0x0A: CH_CTRL1 Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	CTRL_CH4	00	R/W	Configure Channel 4 Output and Protection Status. 00 = Output disabled. OCP, TSD and OLD disabled (default) 01 = Reserved 10 = Output enabled. (OCP, TSD) enabled and OLD disabled 11 = Output disabled. (OCP, TSD) disabled and OLD enabled
D[5:4]	CTRL_CH3	00	R/W	Configure Channel 3 Output and Protection Status. 00 = Output disabled. OCP, TSD and OLD disabled (default) 01 = Reserved 10 = Output enabled. (OCP, TSD) enabled and OLD disabled 11 = Output disabled. (OCP, TSD) disabled and OLD enabled
D[3:2]	CTRL_CH2	00	R/W	Configure Channel 2 Output and Protection Status. 00 = Output disabled. OCP, TSD and OLD disabled (default) 01 = Reserved 10 = Output enabled. (OCP, TSD) enabled and OLD disabled 11 = Output disabled. (OCP, TSD) disabled and OLD enabled
D[1:0]	CTRL_CH1	00	R/W	Configure Channel 1 Output and Protection Status. 00 = Output disabled. OCP, TSD and OLD disabled (default) 01 = Reserved 10 = Output enabled. (OCP, TSD) enabled and OLD disabled 11 = Output disabled. (OCP, TSD) disabled and OLD enabled

Internally let 2'b01 behave as 2'b00.

REGISTER MAPS (continued)

ENERGIZING TIME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	DESCRIPTION
N/A	0	X	X	X	X	X	X	P	Outputs always in energizing mode.
0ms	1	X	X	0	0	0	0	P	No energizing, starts in PWM chopping.
12ms	1	X	X	0	0	0	1	P	Set the energizing time (100% duty cycle) before switching to PWM phase.
20ms	1	X	X	0	0	1	0	P	
40ms	1	X	X	0	0	1	1	P	
60ms	1	X	X	0	1	0	0	P	
80ms	1	X	X	0	1	0	1	P	
120ms	1	X	X	0	1	1	0	P	
200ms	1	X	X	0	1	1	1	P	
320ms	1	X	X	1	0	0	0	P	
440ms	1	X	X	1	0	0	1	P	
560ms	1	X	X	1	0	1	0	P	
680ms	1	X	X	1	0	1	1	P	
800ms	1	X	X	1	1	0	0	P	
920ms	1	X	X	1	1	0	1	P	
1040ms	1	X	X	1	1	1	0	P	
1200ms	1	X	X	1	1	1	1	P	

REG0x12 to REG0x15: CH_ENGx Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	ENER_CHx	000	R/W	Configure Channel x Energizing Mode. 0xx = Output always in energizing mode 100 = Output enter energizing mode before PWM chopping
D[4:1]	ENER_TIME_CHx	0000	R/W	Configure Channel x Energizing Time. 0000 = 0ms (output start in PWM chopping) (default) 0001 = 12ms 0010 = 20ms 0011 = 40ms 0100 = 60ms 0101 = 80ms 0110 = 120ms 0111 = 200ms 1000 = 320ms 1001 = 440ms 1010 = 560ms 1011 = 680ms 1100 = 800ms 1101 = 920ms 1110 = 1040ms 1111 = 1200ms
D[0]	PARITY_ENERx	0	R/W	Odd parity bit for data validity check, include register address. Incorrect parity bit results in frame error (SCLK_FLT) and register will not be updated.

REGISTER MAPS (continued)

FREQUENCY	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	DESCRIPTION
100Hz	0	0	0	X	X	X	X	P	Set the Frequency.
200Hz	0	0	1	X	X	X	X	P	
500Hz	0	1	0	X	X	X	X	P	
1kHz	0	1	1	X	X	X	X	P	
2kHz	1	0	0	X	X	X	X	P	
5kHz	1	0	1	X	X	X	X	P	
10kHz	1	1	0	X	X	X	X	P	
20kHz	1	1	1	X	X	X	X	P	

DUTY	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	DESCRIPTION
0.0%	X	X	X	0	0	0	0	P	Output is Off after Energizing Phase.
6.25%	X	X	X	0	0	0	1	P	Set PWM Chopping Duty Cycle.
12.5%	X	X	X	0	0	1	0	P	
18.75%	X	X	X	0	0	1	1	P	
25.0%	X	X	X	0	1	0	0	P	
31.25%	X	X	X	0	1	0	1	P	
37.5%	X	X	X	0	1	1	0	P	
43.75%	X	X	X	0	1	1	1	P	
50.0%	X	X	X	1	0	0	0	P	
56.25%	X	X	X	1	0	0	1	P	
62.5%	X	X	X	1	0	1	0	P	
68.75%	X	X	X	1	0	1	1	P	
75.0%	X	X	X	1	1	0	0	P	
81.25%	X	X	X	1	1	0	1	P	
87.5%	X	X	X	1	1	1	0	P	
93.75%	X	X	X	1	1	1	1	P	

REG0x1A to REG0x1D: CH_FRDTx Register [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	FREQ_CHx	000	R/W	Configure Channel x PWM Chopping Frequency. 000 = 100Hz (default) 001 = 200Hz 010 = 500Hz 011 = 1kHz 100 = 2kHz 101 = 5kHz 110 = 10kHz 111 = 20kHz
D[4:1]	DUTY_CHx	0000	R/W	Configure Channel x PWM Chopping Duty Ratio. 0000 = 0% (output off after energizing) (default) 1000 = 50% 0001 = 6.25% 1001 = 56.25% 0010 = 12.5% 1010 = 62.5% 0011 = 18.75% 1011 = 68.75% 0100 = 25% 1100 = 75% 0101 = 31.25% 1101 = 81.25% 0110 = 37.5% 1110 = 87.5% 0111 = 43.75% 1111 = 93.75%
D[0]	PARITY_FRDTx	0	R/W	Odd parity bit for data validity check, include register address. Incorrect parity bit results in frame error (SCLK_FLT) and register will not be updated.

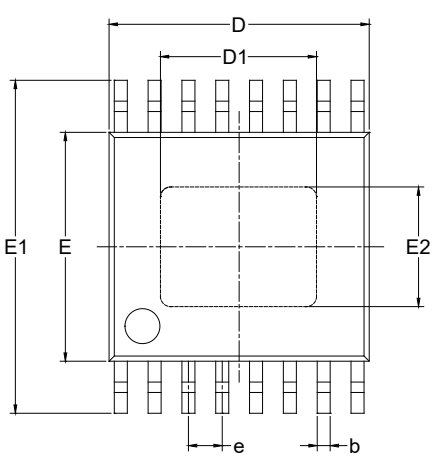
REVISION HISTORY

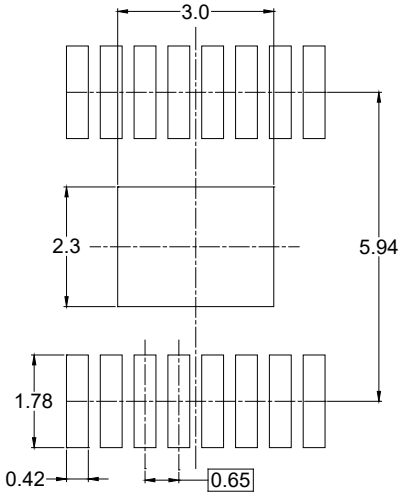
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

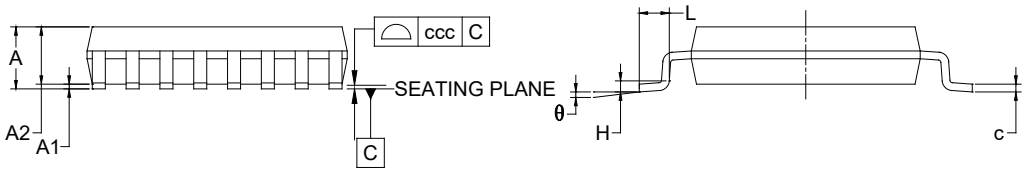
PACKAGE OUTLINE DIMENSIONS

TSSOP-16 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

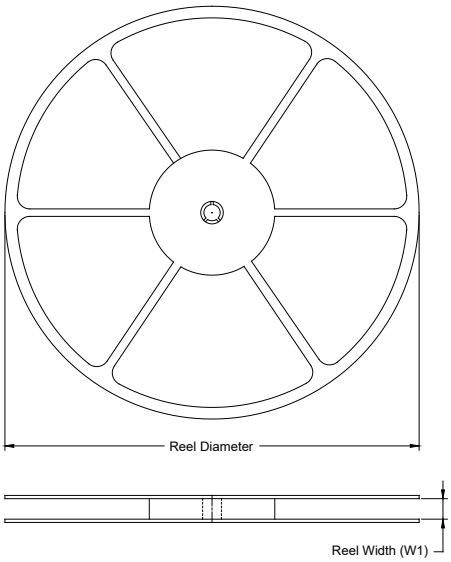


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
D1	2.900	-	3.400
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.200	-	2.980
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

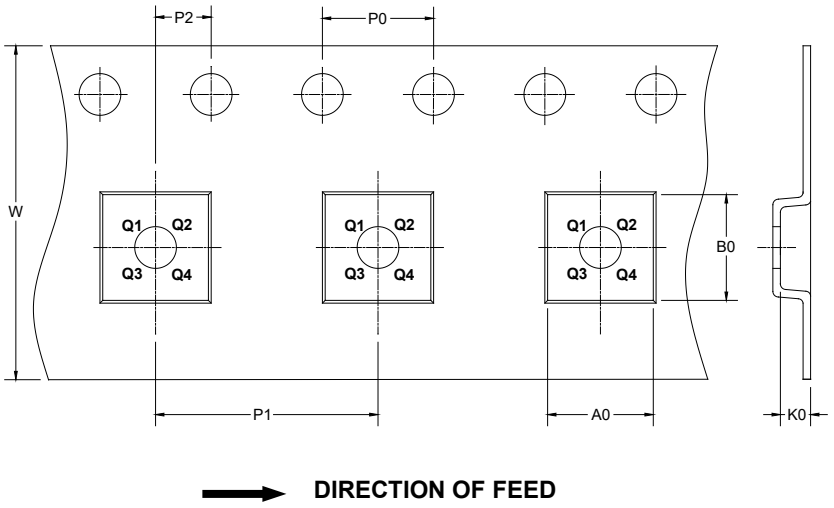
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions, or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



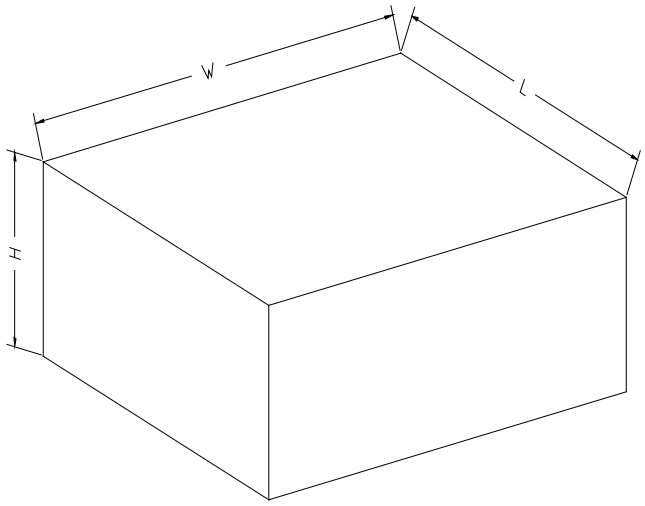
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16 (Exposed Pad)	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002