

# Automotive Linear Regulator with Watchdog, Wake-Up, Reset and Enable Function

### GENERAL DESCRIPTION

The SGM70411Q is a low dropout linear regulator with 5V fixed output and low quiescent current. This device adopts user-programmable reset delay, watchdog timer, automatic wake-up function and enable function. It also has over-temperature protection and over-current protection. Additionally, it can suppress transient voltages with maximum magnitude within 45V.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM70411Q is available in a Green SOIC-8 (Exposed Pad) package. It operates over the ambient temperature range of -40°C to +125°C.

### **FEATURES**

AEC-Q100 Qualified for Automotive Applications
 Device Temperature Grade 1

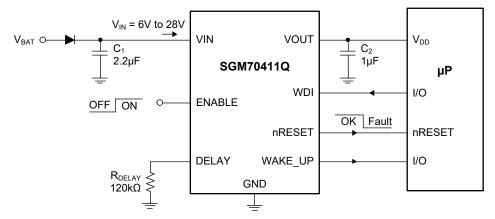
SGM70411Q

- $T_A = -40^{\circ}C$  to +125°C
- Output Voltage of 5.0V
- High Accuracy Output Voltage Tolerance
- Up to 250mA Output Current
- Suitable for Micropower Control Applications: Enable, Watchdog, nRESET and Wake-Up
- Low Dropout Voltage
- Low Quiescent Current: 85µA (TYP)
- Low Sleep Mode Current: Typically Less than 1µA
- Thermal Shutdown and Short-Circuit Protection
- Available in a Green SOIC-8 (Exposed Pad) Package

### **APPLICATIONS**

Automotive Applications
Tire Pressure Monitor
Battery-Powered Consumer Electronics
Applications Requiring Site and Change Control

### TYPICAL APPLICATION



NOTE: C<sub>1</sub> is recommended if the regulator is located away from the power filter. If extremely fast input voltage transients are required to be suppressed, an input filter with several capacitors in parallel can be used.

Figure 1. Typical Application Circuit



### PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ERATURE ORDERING		PACKING OPTION
SGM70411Q	SOIC-8 (Exposed Pad)	-40°C to +125°C	SGM70411QPS8G/TR	1BBPS8 XXXXX	Tape and Reel, 4000

### MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXX	
	- Vendor Code
	Trace Code
	Date Code - Yea

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

### ABSOLUTE MAXIMUM RATINGS

ABOOLOTE MAXIMOM NATINGO
Input Voltage, V <sub>IN</sub> 0.3V to 45V
ENABLE Voltage, V <sub>EN</sub> 0.3V to 45V
Output Voltage, V <sub>OUT</sub> 0.3V to 7V
nRESET Voltage, V <sub>nRESET</sub> 0V to V <sub>OUT</sub>
nRESET Current (1), I <sub>nRESET</sub> Internally Limited
Reset, WDI, Wake-Up, Delay Inputs/Outputs0.3V to 7V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ <sub>JA</sub>
SOIC-8 (Exposed Pad), θ <sub>JB</sub> 19.7°C/W
SOIC-8 (Exposed Pad), θ <sub>JC (TOP)</sub>
SOIC-8 (Exposed Pad), θ <sub>JC (BOT)</sub> 8.5°C/W
Junction Temperature+150°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10s)+260°C
ESD Susceptibility (2)(3)
HBM±4000V
CDM±1000V

#### NOTES:

- 1. nRESET may be incidentally shorted either to VOUT or to GND without damage.
- 2. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
- 3. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

### RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V <sub>IN</sub>	6V to 28V
Operating Ambient Temperature Range40°C	to +125℃
Operating Junction Temperature Range40°C	to +150°C

### **OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

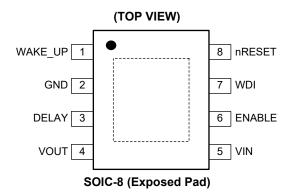
### **ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

### DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

# **PIN CONFIGURATION**



# **PIN DESCRIPTION**

PIN	NAME	FUNCTION
1	WAKE_UP	Frequently wake up the microprocessor from the sleeping mode.
2	GND	Ground.
3	DELAY	Precise Voltage Reference Pin. It is used to provide reference current for the timing circuit with R <sub>DELAY</sub> resistor.
4	VOUT	Regulated Output Voltage.
5	VIN	Power Supply Voltage.
6	ENABLE	Positive Logic Enable Control of the IC.
7	WDI	Watchdog Input Pin. Falling edge effective.
8	nRESET	Reset Output Pin. If $V_{\text{OUT}}$ drops by more than 7% from nominal, or the WDI pin fails to accept an effective falling edge within a wake-up period, the nRESET will become low.
Exposed Pad	_	Exposed Pad.

## **ELECTRICAL CHARACTERISTICS**

 $(V_{IN}$  = 6.0V to 28V,  $I_{OUT}$  = 100μA to 150mA,  $C_2$  = 1.0μF,  $R_{DELAY}$  = 120k $\Omega$ ,  $T_A$  = -40°C to +125°C, typical values are measured at  $T_A$  = +25°C, unless otherwise noted.)

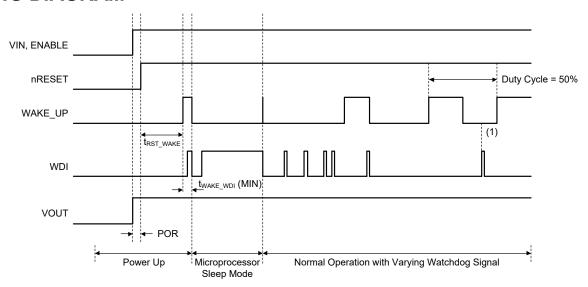
Output Voltage   Vour   Vou	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Output Voltage   Vour   Vou	Output		•				•	
Dropout Voltage (1) (V <sub>N</sub> - V <sub>Ox7</sub> )	0 ( ) () ()			4.93	5	5.07	V	
Load Regulation   REG.   No.   13.5V,	Output Voltage	V <sub>OUT</sub>		-1.4		1.4	%	
Line Regulation   REG <sub>LINE</sub>   Court = 5.0mA, V <sub>IN</sub> = 6.0V to 28V   -10   mV   mV   mV   mA   mA   mA   mA   mA	Dropout Voltage (1) (V <sub>IN</sub> - V <sub>OUT</sub> )	$V_{DO}$	I <sub>OUT</sub> = 150mA		260	450	mV	
Current Limit	Load Regulation	REG <sub>LOAD</sub>	V <sub>IN</sub> = 13.5V, I <sub>OUT</sub> = 100μA to 150mA	-10		10	mV	
Thermal Shutdown (C)	Line Regulation	REG <sub>LINE</sub>	I <sub>OUT</sub> = 5.0mA, V <sub>IN</sub> = 6.0V to 28V	-10		10	mV	
Quiescent Current   I_Q   V <sub>IN</sub> = 13.5V, I <sub>OUT</sub> = 100µA, ENABLE = 2.0V   85   130   µA	Current Limit	I <sub>LIM</sub>		270	480		mA	
Shutdown Current   I_{SD}	Thermal Shutdown (2)	$T_{J\_MAX}$		160	173	186	°C	
Threshold Voltage   Resert = 10kΩ to Vour, Vour = 1.0V   Vour - 0.2   Vour Volty Low   Resert = 10kΩ to Vour, Vour = 1.0V   Vour - 0.2   Vour - 0.01   Vour + 1.0V   Vour - 0.2   Vour - 0.01   Vour + 1.0V   Vour - 0.2   Vour - 0.01   V	Quiescent Current	ΙQ	$V_{IN} = 13.5V$ , $I_{OUT} = 100\mu A$ , ENABLE = 2.0V		85	130	μΑ	
Threshold Voltage	Shutdown Current	I <sub>SD</sub>	ENABLE = 0V, T <sub>A</sub> = +125°C			1.5	μΑ	
Output Low   Resest = 10kΩ to Vour, VouT = 1.0V   0.015   0.2   V	nRESET	I	1					
Output High   Robert   First   Firs	Threshold Voltage			4.58	4.65	4.72	V	
Power-On Reset Delay Time   V <sub>IN</sub> = 13.5V, R <sub>DELAY</sub> = 60 kΩ, I <sub>OUT</sub> = 5.0mA   3.22   V <sub>IN</sub> = 13.5V, R <sub>DELAY</sub> = 120 kΩ, I <sub>OUT</sub> = 5.0mA   5.25   6.25   7.25   ms	Output Low		$R_{nRESET} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1.0V$		0.015	0.2	V	
Power-On Reset Delay Time         to $V_{IN} = 13.5V, R_{DELAY} = 120kΩ, I_{OUT} = 5.0mA$ 5.25         6.25         7.25         ms           Reset Reaction Time $t_{RR}$ $t_{RR}$ 6 $\mu$ s           Watchdog Input (WDI)         Threshold         WDI <sub>HIGH</sub> 30         50         70 $V_{OUT}$ %           Hysteresis         WDI <sub>HIGH</sub> 30         50         70 $V_{OUT}$ %           Hysteresis         WDI <sub>HIGH</sub> 25         100         mV           Input Current         WDI = 6.0V         1.2         2 $\mu$ S           Edge Delay         WDI = 6.0V         1.2         2 $\mu$ S           EMABLE         WAKE_UP Rising Edge to WDI Falling Edge to WDI Falling Falling Edge Delay $\mu$ S $\mu$ S $\mu$ S           EMABLE         ENABLE         2 $\mu$ S $\mu$ S $\mu$ S $\mu$ S           EMABLE         Logic Low Input Threshold $V_{TH_LENH}$ 2 $V$	Output High		$R_{nRESET} = 10k\Omega$ to GND	V <sub>OUT</sub> - 0.2	V <sub>OUT</sub> - 0.01		V	
VIN = 13.5V, R <sub>DELAY</sub> = 500kΩ, I <sub>OUT</sub> = 5.0mA   25.4			$V_{IN}$ = 13.5V, $R_{DELAY}$ = 60k $\Omega$ , $I_{OUT}$ = 5.0mA		3.22			
Reset Reaction Time   trian   trian   watchdog Input (WDI)	Power-On Reset Delay Time	$t_D$	$V_{IN} = 13.5V$ , $R_{DELAY} = 120k\Omega$ , $I_{OUT} = 5.0mA$	5.25	6.25	7.25	ms	
Watchdog Input (WDI)           Threshold         WDI <sub>HIGH</sub> 30         50         70         Voutr%           Hysteresis         WDI <sub>HYS</sub> 25         100         mV           Input Current         WDI = 6.0V         1.2         2         µA           Wake-Up Rising Edge to WDI Falling Edge to WDI Falling Edge Delay         twake_Up Rising Edge to WDI Falling Edge to WDI Falling Edge Delay         5         µs         µs           ENABLE         Use of the property			$V_{IN} = 13.5V$ , $R_{DELAY} = 500k\Omega$ , $I_{OUT} = 5.0mA$		25.4		1	
Threshold   WDI <sub>HIGH</sub>   30   50   70   V <sub>OUT</sub> %	Reset Reaction Time	t <sub>RR</sub>			6		μs	
Hysteresis   WDI <sub>HYS</sub>   25   100   mV     Input Current   WDI = 6.0V   1.2   2   μA     Wake-Up Rising Edge to WDI Falling Edge Delay   twake_Up Rising Edge to WDI Falling Edge Delay   twake_WDI     ENABLE   Logic Low Input Threshold   V <sub>TH_ENL</sub>   0.8   V     Logic High Input Threshold   V <sub>TH_ENL</sub>   2   V     Input Current   ENABLE = 2.0V   3   10   μA     WAKE_UP Output (V <sub>IN</sub> = 13.5V, I <sub>OUT</sub> = 5.0mA)	Watchdog Input (WDI)							
Input Current   WDI = 6.0V   1.2   2	Threshold	WDI <sub>HIGH</sub>		30	50	70	V <sub>OUT</sub> %	
Wake-Up Rising Edge to WDI Falling Edge Delay   ENABLE	Hysteresis	WDI <sub>HYS</sub>		25	100		mV	
Edge Delay   I_WAKE_WDI   S   PS	Input Current		WDI = 6.0V		1.2	2	μΑ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Wake-Up Rising Edge to WDI Falling Edge Delay	t <sub>wake_wdi</sub>		5			μs	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ENABLE							
Input Current ENABLE = 2.0V 3 10 μA WAKE_UP Output ( $V_{IN}$ = 13.5V, $I_{OUT}$ = 5.0mA)  Wake-Up Period $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Logic Low Input Threshold	$V_{TH\_ENL}$				8.0	V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Logic High Input Threshold	$V_{TH\_ENH}$		2			V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Current		ENABLE = 2.0V		3	10	μΑ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	WAKE_UP Output ( $V_{IN} = 13.5V$ , $I_{OUT} =$	5.0mA)						
$R_{DELAY} = 500k\Omega \hspace{1cm} 203 \hspace{1cm} \\ R_{DELAY} = 500k\Omega \hspace{1cm} 203 \hspace{1cm} \\ R_{DELAY} = 500k\Omega \hspace{1cm} 203 \hspace{1cm} \\ R_{DELAY} = 60k\Omega \hspace{1cm} 12.9 \hspace{1cm} \\ R_{DELAY} = 60k\Omega \hspace{1cm} 12.9 \hspace{1cm} \\ R_{DELAY} = 120k\Omega \hspace{1cm} 21 \hspace{1cm} 25 \hspace{1cm} 29 \hspace{1cm} \\ R_{DELAY} = 120k\Omega \hspace{1cm} 21 \hspace{1cm} 25 \hspace{1cm} 29 \hspace{1cm} \\ R_{DELAY} = 500k\Omega \hspace{1cm} \\ R_{DELAY} = 100k\Omega \hspace{1cm} \\ R_{DELAY} = 10k\Omega $			$R_{DELAY} = 60k\Omega$		26			
Wake-Up Duty Cycle Nominal50%nRESET High to Wake-Up Rising Delay Time (50% nRESET rising edge to 50% wake-up edge) $t_{RST\_WAKE}$ $R_{DELAY} = 60k\Omega$ 12.9RDELAY = 120kΩ212529msRDELAY = 500kΩ102Wake-Up Response to Watchdog Input (50% WDI falling edge to 50% wake-up falling edge)0.25 $\mu$ sOutput Low $R_{WAKE-UP} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1V$ 0.010.2 $V$ Output High $R_{WAKE-UP} = 10k\Omega$ to GND $V_{OUT} - 0.2$ $V_{OUT} - 0.015$ $V$	Wake-Up Period		$R_{DELAY} = 120k\Omega$		50		ms	
RESET High to Wake-Up Rising Delay Time (50% nRESET rising edge to 50% wake-up edge)			$R_{DELAY} = 500k\Omega$		203			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Wake-Up Duty Cycle Nominal				50		%	
edge to 50% wake-up edge) $R_{DELAY} = 500k\Omega$ 102       Wake-Up Response to Watchdog Input (50% WDI falling edge to 50% wake-up falling edge)     0.2     5     μs       Output Low $R_{WAKE-UP} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1V$ 0.01     0.2 $V$ Output High $R_{WAKE-UP} = 10k\Omega$ to GND $V_{OUT} - 0.2$ $V_{OUT} - 0.015$ $V$	nRESET High to Wake-Up Rising		$R_{DELAY} = 60k\Omega$		12.9			
Wake-Up Response to Watchdog       Roelay = 500kΩ       102         Input (50% WDI falling edge to 50% wake-up falling edge)       0.2       5 $\mu$ s         Output Low $R_{WAKE-UP} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1V$ 0.01       0.2 $V$ Output High $R_{WAKE-UP} = 10k\Omega$ to GND $V_{OUT} - 0.2$ $V_{OUT} - 0.015$ $V$	Delay Time (50% nRESET rising	t <sub>RST_WAKE</sub>	$R_{DELAY} = 120k\Omega$	21	25	29	ms	
Input (50% WDI falling edge to 50% wake-up falling edge)  Output Low $R_{WAKE-UP} = 10k\Omega$ to $V_{OUT}$ , $V_{OUT} = 1V$ Output High $R_{WAKE-UP} = 10k\Omega$ to GND $R_{WAKE-UP} = 10k\Omega$ to GND $R_{WAKE-UP} = 10k\Omega$ to GND	,		$R_{DELAY} = 500k\Omega$		102			
Output Low $R_{WAKE-UP} = 10kΩ$ to $V_{OUT}$ , $V_{OUT} = 1V$ 0.01         0.2         V           Output High $R_{WAKE-UP} = 10kΩ$ to GND $V_{OUT} - 0.2$ $V_{OUT} - 0.015$ V           DELAY	Wake-Up Response to Watchdog Input (50% WDI falling edge to 50% wake-up falling edge)	_		_	0.2	5	μs	
DELAY	Output Low		$R_{\text{WAKE-UP}} = 10 \text{k}\Omega$ to $V_{\text{OUT}}$ , $V_{\text{OUT}} = 1 \text{V}$		0.01	0.2	V	
	Output High		$R_{WAKE-UP} = 10k\Omega$ to GND	V <sub>OUT</sub> - 0.2	V <sub>OUT</sub> - 0.015		V	
Output Voltage $R_{DELAY} = 60 k\Omega$ , $120 k\Omega$ , $500 k\Omega$ 0.48 V	DELAY							
	Output Voltage		$R_{DELAY}$ = 60kΩ, 120kΩ, 500kΩ		0.48		V	

#### NOTES:

- 1. These values are taken when the output voltage decreases by 2% from its nominal value.
- 2. Guaranteed by design.
- 3. Input or enable slew rates in excess of 3V/µs may cause nRESET to change state.



## **TIMING DIAGRAM**



NOTE: 1. If the WDI pulse occurs with the WAKE\_UP signal low, the wake-up duty cycle will be 50%.

VIN, ENABLE

nRESET

WAKE\_UP

WDI

VOUT

POR

Wake Up Period

Figure 2. Power-Up, Sleep Mode and Normal Operation



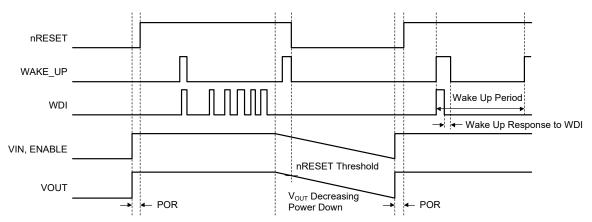
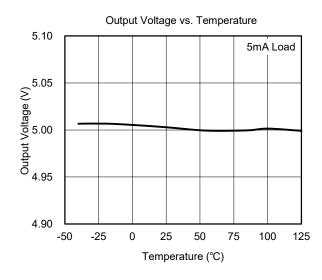
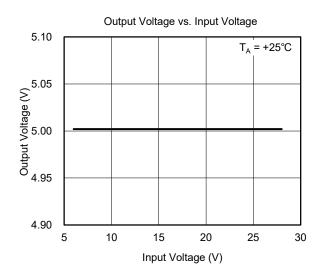
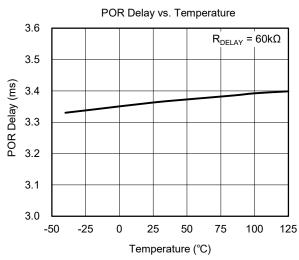


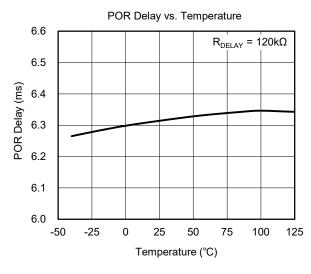
Figure 4. Power-Down, Restart Sequence, and Wake-Up Response to WDI

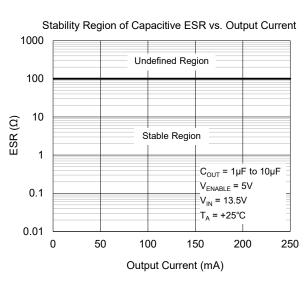
# TYPICAL PERFORMANCE CHARACTERISTICS

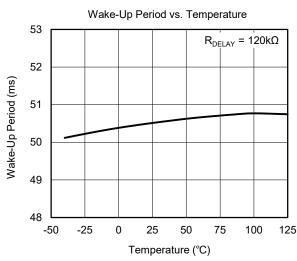




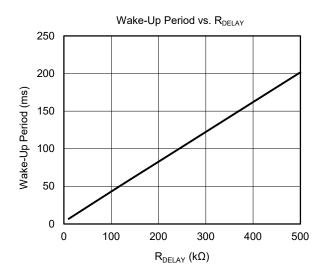


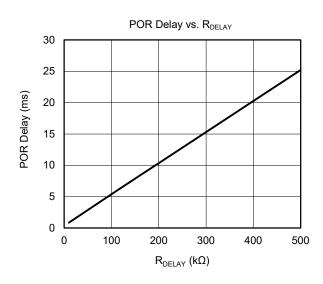


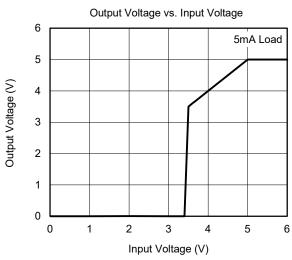


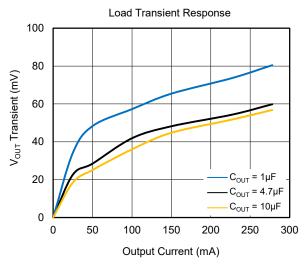


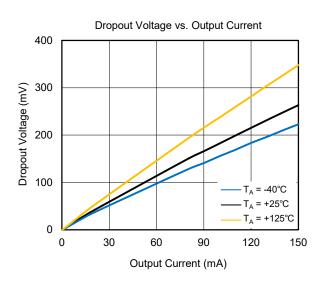
# **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

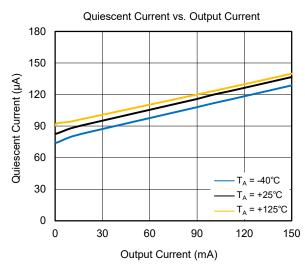












# **FUNCTIONAL BLOCK DIAGRAM**

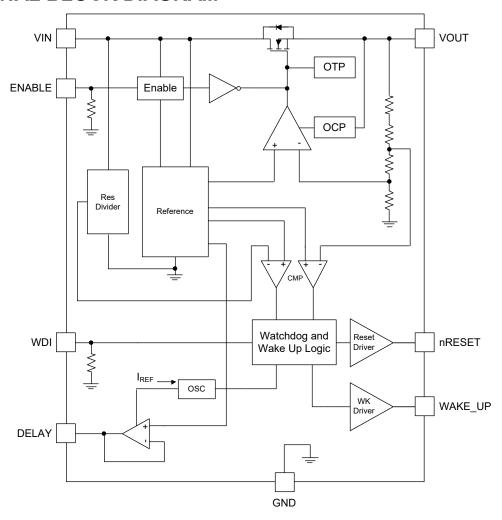


Figure 5. Block Diagram

### **DEATILED DESCRIPTION**

### General

The SGM70411Q is a high precision linear low dropout regulator with enable, watchdog, wake-up and reset functions. It has low supply current of  $85\mu A$  (TYP) at  $100\mu A$  load and low dropout voltage of 260mV (TYP) at 150mA load. With the two advantages mentioned above, this device is very suitable for battery powered consumer electronics and automotive applications.

The SGM70411Q has built-in short-circuit protection and thermal shutdown function without any external elements. It can still work properly under extremely high transient voltage up to 45V, making it ideal for automotive applications.

### Wake Up and Watchdog

To reduce the power loss of the battery when no code is executing, the micro-processor usually goes into the sleeping mode in order to consume very low supply current. The SGM70411Q periodically provides wake-up signal that tries to break the sleeping mode. At the rising edge of the wake up signal, a WDI signal is sent out by the micro-processor and checked to determine whether the SGM70411Q stays in the sleeping mode or wakes up to the normal mode. Typically, the wake-up signal is a 5V square wave with a duty cycle of 50% generated by  $V_{\rm OUT}$ . The frequency of the wake-up signal is decided by the external resistor placed between the DELAY pin and GND.

The falling edge of the WDI signal is effective for the SGM70411Q. When an effective WDI pulse is recognized, the WAKE UP pin is pulled low and other pulses from WDI are aborted in this wake-up period. Note that the watchdog module continues to receive and monitor the WDI signal. Once no WDI falling edge is detected during a wake-up period, the nRESET pin will be pulled low at the end of the wake-up cycle (see Figure 3).

### **nRESET**

When  $V_{\text{OUT}}$  drops and the nRESET pin goes low, the nRESET keeps low until  $V_{\text{OUT}}$  < 1V. The nRESET goes low for any of four conditions:

- 1. The nRESET pin maintains low until  $V_{\text{OUT}}$  is higher than the nRESET positive-going threshold in the power-on process.
- 2. When  $V_{\text{OUT}}$  is in regulation, the nRESET goes low as  $V_{\text{OUT}}$  falls under the nRESET negative-going threshold. The nRESET will not turn high unless the following two conditions are simultaneously met:
- 1).  $V_{\text{OUT}}$  is higher than the nRESET positive-going threshold.
- 2). The new reset delay POR is finished.
- 3. No effective WDI falling edge is detected in a wake-up period.
- 4. The VIN voltage is too low, and the internal circuits cannot work properly. This voltage value of VIN is related to temperature. For example, it is about 4.5V at +25°C.

The WAKE\_UP pin goes low when nRESET is asserted. After the nRESET returns high, the wake-up timer starts to count again (see Figure 3).

The wake-up period, nRESET delay time and nRESET high to wake-up delay time are determined by  $R_{\text{DELAY}}$ , described as below:

Wake-up period(s) = 
$$(4.18 \times 10^{-7}) \times R_{DFLAY}(\Omega)$$
 (1)

nRESET delay time (s) = 
$$(5.21 \times 10^{-8}) \times R_{DELAY}(\Omega)$$
 (2)

nRESET high to wake-up delay time(s)

$$= (2.08 \times 10^{-7}) \times R_{DELAY}(\Omega) \tag{3}$$

The DELAY pin voltage is generated from the bandgap and is intended to be used as a voltage reference.

### **Enable**

The ENABLE pin is used to turn on or turn off the SGM70411Q and can be applied with TTL or CMOS logic level. Logic high means the device is enabled and turned on while logic low means the device is disabled and turned off. When in disabled status, the overall supply current decreases to no more than 1.5µA.

### **REVISION HISTORY**

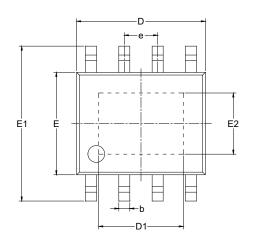
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

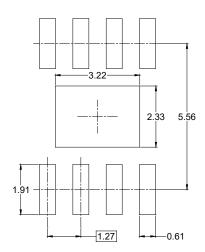
Changes from Original to REV.A (JUNE 2025)

Page



# **PACKAGE OUTLINE DIMENSIONS SOIC-8 (Exposed Pad)**





### RECOMMENDED LAND PATTERN (Unit: mm)



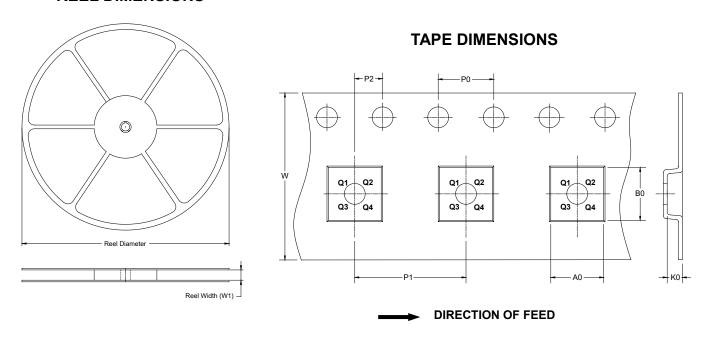
Symbol	Dimensions In Millimeters						
	MIN	NOM	MAX				
Α			1.700				
A1	0.000	-	0.150				
A2	1.250	-	1.650				
b	0.330	-	0.510				
С	0.170	-	0.250				
D	4.700 -		5.100				
D1	3.020	-	3.420				
Е	3.800	-	4.000				
E1	5.800	-	6.200				
E2	2.130	-	2.530				
е	1.27 BSC						
L	0.400	1.270					
θ	0°	8°					
ccc	0.100						

### NOTES:

- This drawing is subject to change without notice.
   The dimensions do not include mold flashes, protrusions or gate burrs.
- 3. Reference JEDEC MS-012.

# TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**

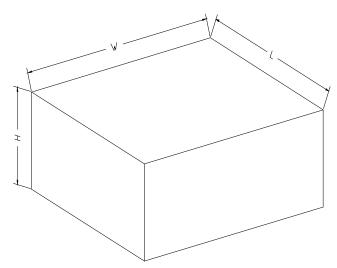


NOTE: The picture is only for reference. Please make the object as the standard.

### **KEY PARAMETER LIST OF TAPE AND REEL**

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

# **CARTON BOX DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

# **KEY PARAMETER LIST OF CARTON BOX**

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
13″	386	280	370	5	DD0002