SGM52461S4/SGM52461S8
4- and 8-Channel, 24-Bit, Simultaneously-Sampling, Sigma-Delta ADCs

GENERAL DESCRIPTION

The SGM52461S4 and SGM52461S8 are highly advanced analog-to-digital converters (ADCs) that are specifically designed for industrial power monitoring and protection, as well as test and measurement applications. They feature simultaneous sampling, 24-bit sigma-delta (Σ-Δ) conversion, a programmable gain amplifier (PGA), internal reference, and an on-chip oscillator. The SGM52461S4 and SGM52461S8 have a wide dynamic range and scalable data rates, making them ideal for a wide range of industrial applications.

The SGM52461S4 and SGM52461S8 have relatively high-impedance inputs that enable voltage transformer, current transformer, or Rogowski coil for line voltage and current measurement. These devices also have a flexible input multiplexer per channel, which can be independently connected to internally-generated signals for testing, temperature, and fault detection. The integrated comparators with digital-to-analog converter (DAC)-controlled trigger levels enable the fault detection to be implemented internally.

The SGM52461S4 and SGM52461S8 are highly integrated, which means that they offer exceptional performance and internal fault detection monitors. These devices can operate at data rates up to 64kSPS and are packaged in a Green TQFP-10×10-64L package, making them ideal for creating scalable industrial power systems at a reduced size, power, and overall cost.

The SGM52461S4 and SGM52461S8 operate over the industrial temperature range of -40℃ to +125℃, which makes them suitable for a wide range of industrial environments.

FEATURES

- **Features Eight Differential ADC Inputs**
- **Programmable Gains: 1, 2, 4, 8, and 12**
- **Data Rates: 1, 2, 4, 8, 16, 32, and 64kSPS**
- **Outstanding Performance:**
  - **Dynamic Range: 119dB (TYP) at 1kSPS**
  - **Crosstalk: -110dB (TYP)**
  - **THD: -98dB (TYP) at 8kSPS**
- **Analog Supply Range Options:**
  - **3V to 5V (Unipolar)**
  - **±2.5V (Bipolar, Allows DC-Coupling)**
- **Digital Supply Range: 1.8V to 3.6V**
- **Low Power: 2.2mW/Channel (TYP) at Analog Supply = 3V**
- **Device Testing Capability and Fault Detection**
- **SPI-Compatible Interface and Four GPIOs**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green TQFP-10×10-64L Package**

APPLICATIONS

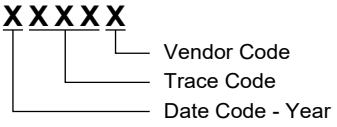
Medical and Healthcare
Battery Test Systems (BTS)
Power Protection: Relay Protection and Circuit Breakers
Energy Metering: Power Quality, Single Phase and Polyphase
Simultaneous Sampling Data Acquisition Systems (DAS)
Testing and Measurement

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52461S4	TQFP-10×10-64L	-40℃ to +125℃	SGM52461S4XTFI64G/TR	SGM52461S4 XTFI64 XXXXX	Tape and Reel, 1000
			SGM52461S4XTFI64SG/TR	SGM52461S4 XTFI64 XXXXX	Tape and Reel, 500
SGM52461S8	TQFP-10×10-64L	-40℃ to +125℃	SGM52461S8XTFI64G/TR	SGM52461S8 XTFI64 XXXXX	Tape and Reel, 1000
			SGM52461S8XTFI64SG/TR	SGM52461S8 XTFI64 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range
AVDD to AVSS ..... -0.3V to 5.5V
AVSS to DGND ..... -3V to 0.2V
DVDD to DGND ..... -0.3V to 5.5V
Analog Input Voltage Range
Analog Input to AVSS ..... AVSS - 0.3V to AVDD + 0.3V
Digital Input Voltage Range
Digital Input to DVDD ..... DGND - 0.3V to DVDD + 0.3V
Input Current
Momentary ..... -100mA to 100mA
Continuous, All Other Pins except Power Supply Pins ..... -10mA to 10mA
Package Thermal Resistance
TQFP-10×10-64L, θ_{JA} ..... 52.1℃/W
TQFP-10×10-64L, θ_{JB} ..... 35.0℃/W
TQFP-10×10-64L, θ_{JC} ..... 11.0℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±6000V
CDM ..... ±1000V

NOTES:
1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Analog Power Supply Voltage Range, AVDD
AVDD to AVSS ..... 2.7V to 5.25V, 5V (TYP)
Digital Power Supply Voltage Range, DVDD
DVDD to DGND ..... 1.7V to 3.6V, 3.3V (TYP)
Analog to Digital Supply Voltage Range
AVDD to DVDD ..... -2.1V to 3.6V
Differential Input Voltage Range, V_{IN} (V_{IN} = V_{INxP} - V_{INxN}) ..... -V_{REF}/Gain to V_{REF}/Gain
Absolute Input Voltage, V_{INxP}, V_{INxN} ..... AVSS - 0.05V to AVDD + 0.05V
Reference Input Voltage Range, V_{REF}, (V_{REF} = V_{VREFP} - V_{VREFN})
AVDD = 3V ..... 2V to AVDD, 2.5V (TYP)
AVDD = 5V ..... 2V to AVDD, 4V (TYP)
Negative Reference Input, VREFN ..... AVSS
Positive Reference Input
VREFP ..... (AVDD - 3V) to AVDD, AVSS + 2.5V (TYP)
Master Clock Rate, f_{CLK} (CLKSEL Pin = 0)
AVDD - AVSS = 3V ..... 1.7MHz to 2.25MHz, 2.048MHz (TYP)
AVDD - AVSS = 5V ..... 1MHz to 2.25MHz, 2.048MHz (TYP)
Input Voltage Range ..... DGND - 0.1V to DVDD + 0.1V
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

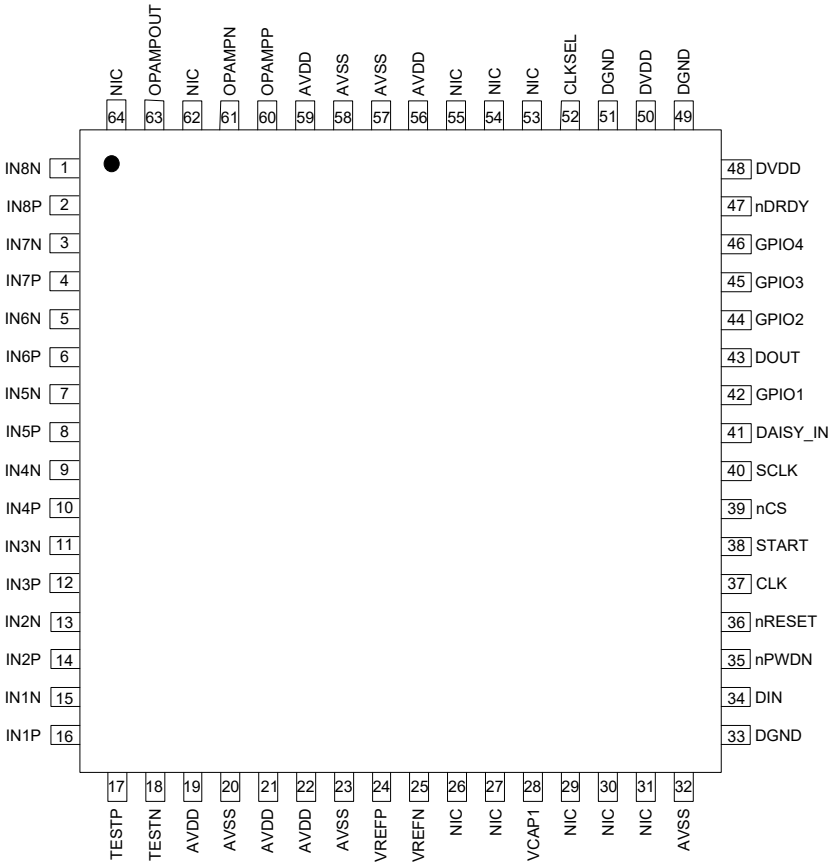
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

SGM52461S4/SGM52461S8 (TOP VIEW)



TQFP-10×10-64L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	IN8N (2)	AI	Negative Analog Input 8 (SGM52461S8 Only).
2	IN8P (2)	AI	Positive Analog Input 8 (SGM52461S8 Only).
3	IN7N (2)	AI	Negative Analog Input 7 (SGM52461S8 Only).
4	IN7P (2)	AI	Positive Analog Input 7 (SGM52461S8 Only).
5	IN6N (2)	AI	Negative Analog Input 6 (SGM52461S8 Only).
6	IN6P (2)	AI	Positive Analog Input 6 (SGM52461S8 Only).
7	IN5N (2)	AI	Negative Analog Input 5 (SGM52461S8 Only).
8	IN5P (2)	AI	Positive Analog Input 5 (SGM52461S8 Only).
9	IN4N (2)	AI	Negative Analog Input 4.
10	IN4P (2)	AI	Positive Analog Input 4.
11	IN3N (2)	AI	Negative Analog Input 3.
12	IN3P (2)	AI	Positive Analog Input 3.
13	IN2N (2)	AI	Negative Analog Input 2.
14	IN2P (2)	AI	Positive Analog Input 2.
15	IN1N (2)	AI	Negative Analog Input 1.
16	IN1P (2)	AI	Positive Analog Input 1.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
17	TESTP	AI	Positive Test Signal Pin.
18	TESTN	AI	Negative Test Signal Pin.
19, 21, 22, 56, 59	AVDD	P	Analog Supply. Each AVDD pin connects a 1μF (or larger) capacitor to AVSS.
20, 23, 32, 57, 58	AVSS	P	Analog Ground.
24	VREFP	AIO	Positive Reference Voltage. Place a minimum 10μF capacitor between this pin and VREFN.
25	VREFN	AI	Negative Reference Voltage. Connect it to AVSS.
26, 27, 29, 30, 31, 53, 54, 55, 62, 64	NIC	—	No Inner Connection. Leave floating. It can be connected to AVDD or AVSS with a 10kΩ or higher resistor.
28	VCAP1	AO	Analog Bypass Capacitor. Place a 22μF capacitor between this pin and AVSS.
33, 49, 51	DGND	P	Digital Ground.
34	DIN	DI	Serial Data Input.
35	nPWDN	DI	Power-Down. Active low.
36	nRESET	DI	System Reset. Active low.
37	CLK	DI	Master Clock Input. If not in use, connect to DGND.
38	START	DI	Start Conversion.
39	nCS	DI	Chip Select. Active low.
40	SCLK	DI	Serial Clock Input.
41	DAISY_IN	DI	Daisy-Chain Input. If not in use, connect to DGND.
42	GPIO1	DIO	General-Purpose Input/Output Pin 1. If not in use, connect to DGND with a 10kΩ resistor.
43	DOUT	DO	Serial Data Output.
44	GPIO2	DIO	General-Purpose Input/Output Pin 2.If not in use, connect to DGND with a 10kΩ resistor.
45	GPIO3	DIO	General-Purpose Input/Output Pin 3. If not in use, connect to DGND with a 10kΩ resistor.
46	GPIO4	DIO	General-Purpose Input/Output Pin 4. If not in use, connect to DGND with a 10kΩ resistor.
47	nDRDY	DO	Data Ready. Active low. If not in use, connect to DGND with a 10kΩ resistor.
48, 50	DVDD	P	Digital Core Power Supply. Each DVDD pin connects a 1μF (or larger) capacitor to DGND.
52	CLKSEL	DI	Master Clock Select.
60	OPAMPP	AI	Operational Amplifier Noninverting Input. If not used, leave it unconnected and power down the operational amplifier.
61	OPAMPN	AI	Operational Amplifier Inverting Input. If not used, leave it unconnected and power down the operational amplifier.
63	OPAMPOUT	AO	Operational Amplifier Output. If not used, leave it unconnected and power down the operational amplifier.

NOTES:

1. AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

2. For any unused or powered-down analog input pins, connect to AVDD.

ELECTRICAL CHARACTERISTICS

(DVDD = 1.8V, AVDD = 3V, AVSS = 0V, V_{REF} = 2.4V, External f_{CLK} = 2.048MHz, Data Rate = 8kSPS, and Gain = 1, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Inputs						
Input Capacitance	C_I			5.8		pF
Input Bias Current	I_{IB}	PGA output in normal range		115		nA
DC Input Impedance				740		kΩ
PGA Performance						
Gain Settings				1, 2, 4, 8, 12		
Bandwidth	BW			See Table 3		
ADC Performance						
Data Rate	DR	f_{CLK} = 2.048MHz	1		64	kSPS
Resolution		DR = 1kSPS, 2kSPS, 4kSPS, 8kSPS, and 16kSPS	24			Bits
		DR = 32kSPS and 64kSPS	16			
Channel Performance (DC Performance)						
Integral Nonlinearity	INL	Full-scale, best fit		10		ppm
Dynamic Range		G = 1	See the Noise Measurements section			
		Gain settings other than 1				
Offset Error	E_O			-100		μV
Offset Error Drift				0.65		μV/℃
Gain Error	E_G	Excluding voltage reference error		0.03		%
Gain Drift		Excluding voltage reference drift		0.5		ppm/℃
Gain Match between Channels				0.02		% of FS
Channel Performance (AC Performance)						
Common Mode Rejection Ratio	CMRR	f_{CM} = 50Hz and 60Hz (1)		-110		dB
Power Supply Rejection Ratio	PSRR	f_{PS} = 50Hz and 60Hz		-80		dB
Crosstalk		f_{IN} = 50Hz and 60Hz		-110		dB
Accuracy		3000:1 dynamic range with a 1-second measurement (V_{RMS}/I_{RMS}), AVDD = 3V, V_{REF} = 2.4V		0.04		%
		3000:1 dynamic range with a 1-second measurement (V_{RMS}/I_{RMS}), AVDD = 5V, V_{REF} = 4V		0.025		
Signal-to-Noise Ratio	SNR	f_{IN} = 50Hz and 60Hz, gain = 1		105		dB
Total Harmonic Distortion	THD	10Hz, -0.5dBFs		-98		dB
Internal Reference						
Output Voltage	V_{REF}	T_A = +25℃, V_{REF} = 2.4V	2.394	2.400	2.406	V
		T_A = +25℃, V_{REF} = 4V		4		V
V_{REF} Accuracy				±0.01		%
Temperature Drift		T_A = -40℃ to +125℃		5	10	ppm/℃
Start-Up Time		Settled to 0.2%		150		ms
External Reference						
Input Impedance				42		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(DVDD = 1.8V, AVDD = 3V, AVSS = 0V, V_{REF} = 2.4V, External f_{CLK} = 2.048MHz, Data Rate = 8kSPS, and Gain = 1, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Oscillator							
Accuracy					±0.15	±2	%
Internal Oscillator Clock Frequency			Nominal frequency		2.048		MHz
Internal Oscillator Start-Up Time					20		μs
Internal Oscillator Power Consumption					135		μW
Fault Detect and Alarm							
Comparator Threshold Accuracy					±30		mV
Operational Amplifier							
Integrated Noise			0.1Hz to 25Hz		8		μVRMS
Noise Density			2kHz		120		$nV\sqrt{Hz}$
Gain Bandwidth Product		GBP	50kΩ || 10pF load		100		kHz
Slew Rate		SR	50kΩ || 10pF load		0.3		V/μs
Load Current					100		μA
Total Harmonic Distortion		THD	f_{IN} = 100Hz		70		dB
Common Mode Input Range				AVSS + 0.3		AVDD - 0.3	V
Quiescent Power Consumption					32		μA
System Monitors							
Supply Reading Error	Analog				2		%
	Digital				0.5		
Device Wake-Up			From pulling nPWDN high to nDRDY low		475		μs
			From exiting standby mode to nDRDY low		475		
			Standby mode		31.25		
Temperature Sensor Reading	Voltage		T_A = +25℃		145		mV
	Coefficient				470		μV/℃
Self-Test Signal							
Signal Frequency			See the General Register Maps section for settings		$f_{CLK}/2^{21}$		Hz
					$f_{CLK}/2^{20}$		
Signal Voltage (2)			See the General Register Maps section for settings		±0.87		mV
					±1.74		
Digital Input and Output (DVDD = 1.8V to 3.6V)							
High-Level Input Voltage		V_{IH}		0.8 × DVDD		DVDD + 0.1	V
Low-Level Input Voltage		V_{IL}		-0.1		0.2 × DVDD	V
High-Level Output Voltage		V_{OH}	I_{OH} = -500μA	0.9 × DVDD			V
Low-Level Output Voltage		V_{OL}	I_{OL} = 500μA			0.1 × DVDD	V
Input Current		I_{IN}	0V < $V_{DigitalInput}$ < DVDD	-1		1	μA

NOTES:

1. The CMRR is measured using a common mode signal of (AVSS + 0.3V) to (AVDD - 0.3V). The value shown is the minimum of the eight channels.

2. The self-test signal voltage is measured with all channel inputs connected to the test signal and all channels enabled simultaneously.

ELECTRICAL CHARACTERISTICS (continued)

(DVDD = 1.8V, AVDD = 3V, AVSS = 0V, V_{REF} = 2.4V, External f_{CLK} = 2.048MHz, Data Rate = 8kSPS, and Gain = 1, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Operational Amplifier Turned Off)							
Normal Mode		I_{AVDD}	AVDD - AVSS = 3V		11.6		mA
			AVDD - AVSS = 5V		13.5		
		I_{DVDD}	DVDD = 3.3V		2		
			DVDD = 1.8V		1.0		
Power Dissipation (Analog Supply = 3V, Internal f_{CLK} = 2.048MHz, SGM52461S4 Register Address: 0x09 - 0x0C, Value: 0x80)							
Quiescent Power Dissipation	SGM52461S4		Normal mode		21.5	28	mW
			Power-down mode		2		μW
			Standby mode		2.2		mW
	SGM52461S8		Normal mode		36.5	46	mW
			Power-down mode		2		μW
			Standby mode		2.2		mW
Power Dissipation (Analog Supply = 3.3V, Internal f_{CLK} = 2.048MHz)							
Quiescent Power Dissipation	SGM52461S8		Normal mode		39		mW
			Standby mode		2.5		
Power Dissipation (Analog Supply = 5V, Internal f_{CLK} = 2.048MHz, SGM52461S4 Register Address: 0x09 - 0x0C, Value: 0x80)							
Quiescent Power Dissipation	SGM52461S4		Normal mode		39		mW
			Power-down mode		3.2		μW
			Standby mode		4		mW
	SGM52461S8		Normal mode		69.5		mW
			Power-down mode		3.2		μW
			Standby mode		4		mW

TIMING REQUIREMENTS

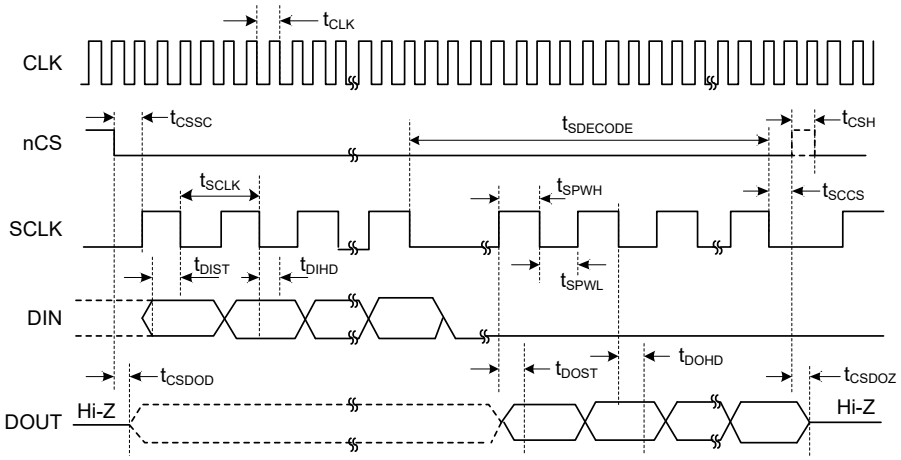
(T_A = -40℃ to +125℃ and DVDD = 1.7V to 3.6V, unless otherwise noted.)

PARAMETER	SYMBOL	2.7V ≤ DVDD ≤ 3.6V		2.0V ≤ DVDD ≤ 2.7V		1.7V ≤ DVDD ≤ 2.0V		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Master Clock Period	t_{CLK}	444	588	444	588	444	588	ns
Delay Time, First SCLK Rising Edge after nCS Falling Edge	t_{CSSC}	6		17		17		ns
SCLK Period	t_{SCLK}	50		66.6		76		ns
Pulse Duration, SCLK High or Low	$t_{SPWH, L}$	17		26		34		ns
Setup Time, DIN Valid before SCLK Falling Edge	t_{DIST}	10		10		10		ns
Hold Time, DIN Valid after SCLK Falling Edge	t_{DIHD}	10		11		11		ns
Pulse Duration, nCS High	t_{CSH}	2		2		2		t_{CLK}
Delay Time, nCS Rising Edge after Final SCLK Falling Edge	t_{SCCS}	4		4		4		t_{CLK}
Command Decode Time	$t_{SDECODE}$	4		4		4		t_{CLK}
Setup Time, DAISY_IN Valid before SCLK Falling Edge	$t_{DISCK2ST}$	10		10		10		ns
Hold Time, DAISY_IN Valid after SCLK Falling Edge	$t_{DISCK2HT}$	10		10		12		ns

SWITCHING CHARACTERISTICS

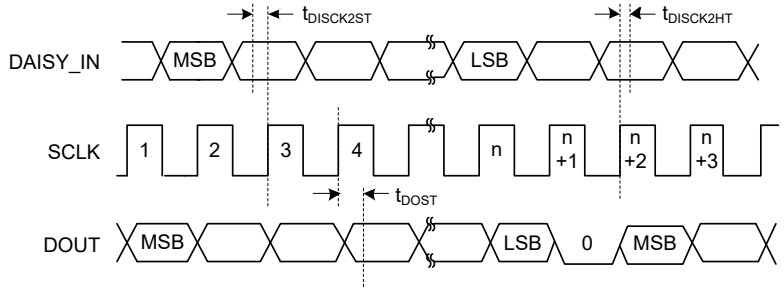
(T_A = -40℃ to +125℃, DVDD = 1.7V to 3.6V, and load on DOUT = 20pF || 100kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	2.7V ≤ DVDD ≤ 3.6V		2.0V ≤ DVDD ≤ 2.7V		1.7V ≤ DVDD ≤ 2.0V		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Propagation Delay Time, nCS Falling Edge to DOUT Driven	t_{CSDOD}	16		24		32		ns
Propagation Delay Time, SCLK Rising Edge to Valid New DOUT	t_{DOST}		17		24		32	ns
Hold Time, SCLK Falling Edge to Invalid DOUT	t_{DOHD}	10		10		10		ns
Propagation Delay Time, nCS Rising Edge to DOUT High Impedance	t_{CSDOZ}		20		24		30	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing Diagram

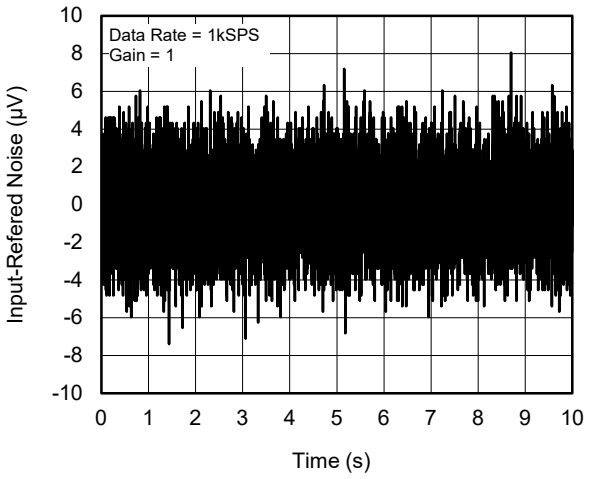


NOTE: n = Number of channels × resolution + 24 bits.
Number of channels is 8, resolution is 24-bit.

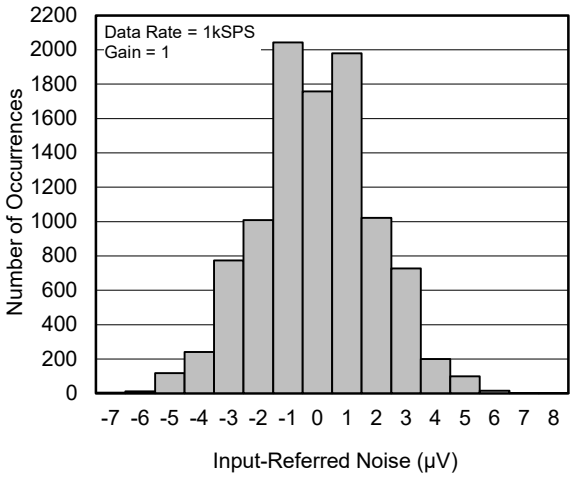
Figure 2. Daisy-Chain Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

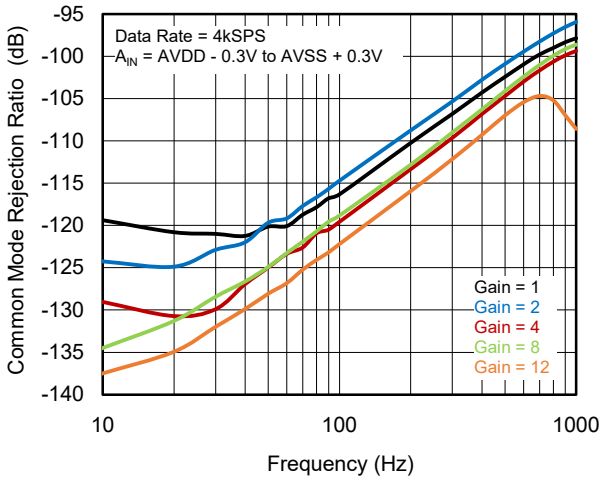
Input-Referred Noise



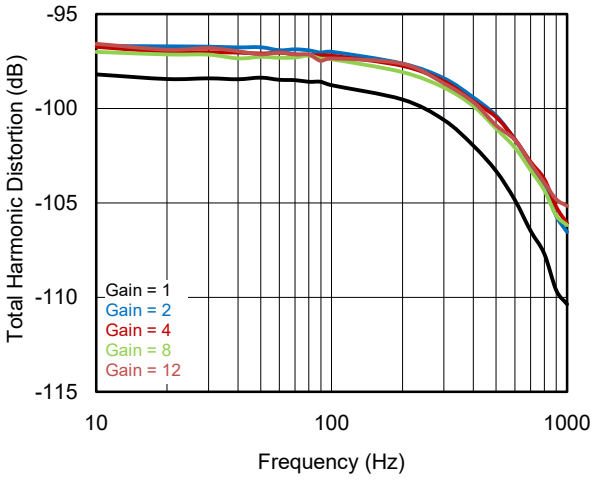
Noise Histogram



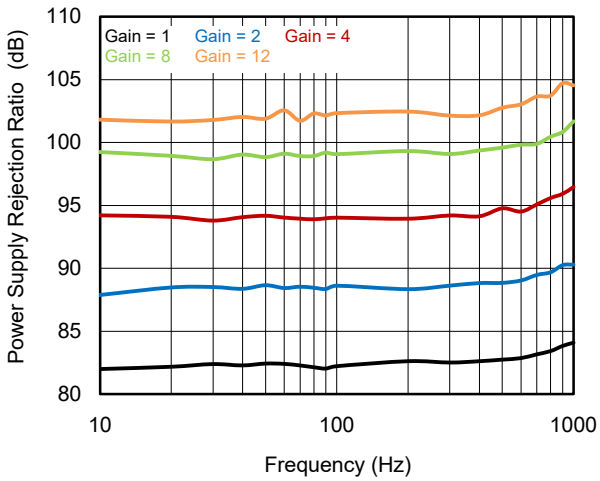
Common Mode Rejection Ratio vs. Frequency



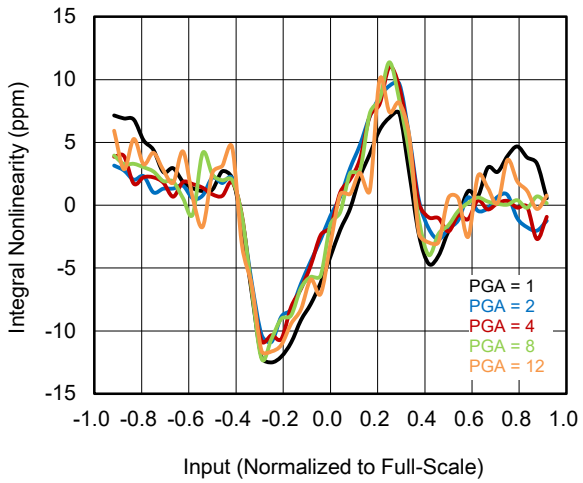
Total Harmonic Distortion vs. Frequency



Power Supply Rejection Ratio vs. Frequency

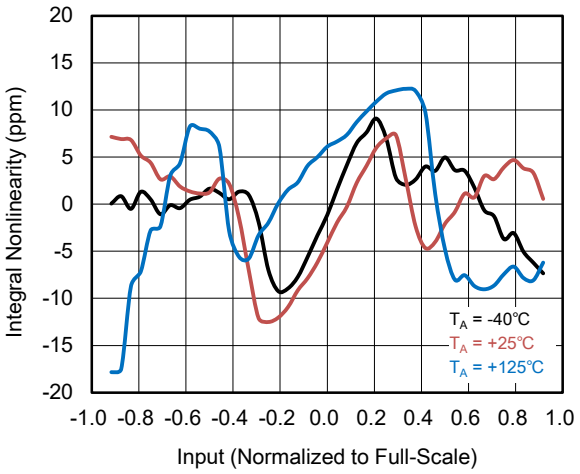


INL vs. PGA Gain

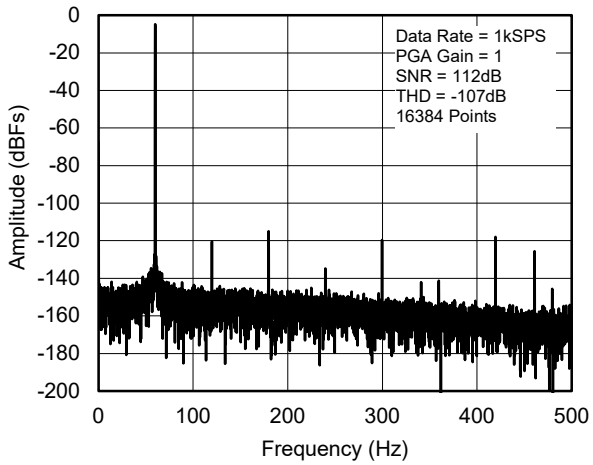


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

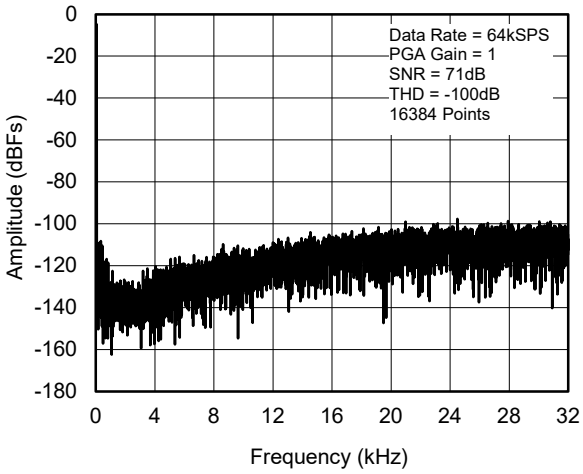
INL vs. Temperature



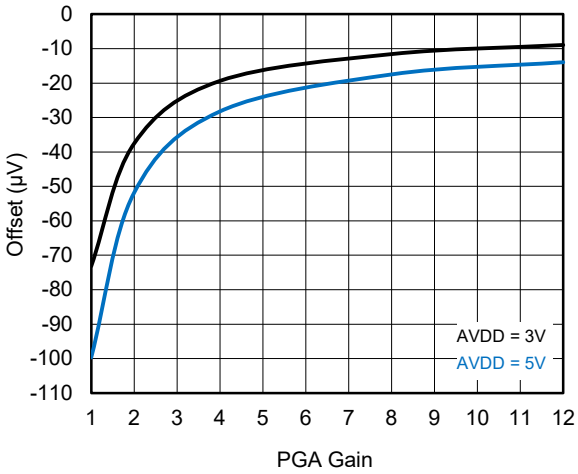
THD FFT Plot



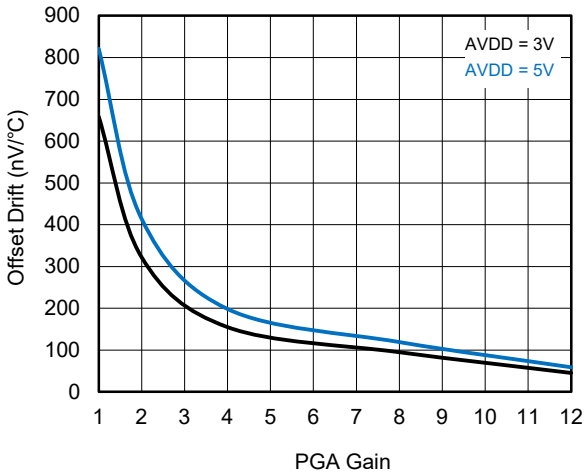
FFT Plot



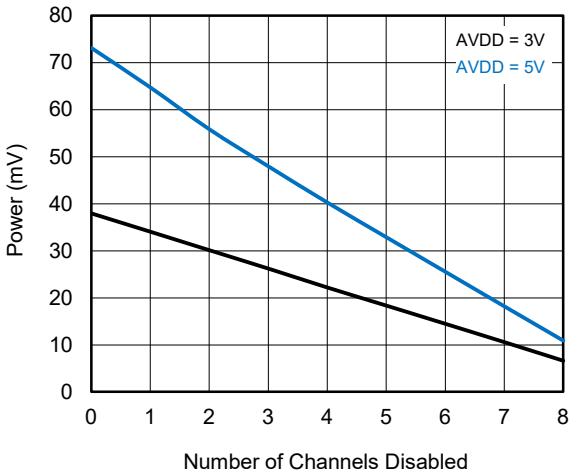
Offset vs. PGA Gain



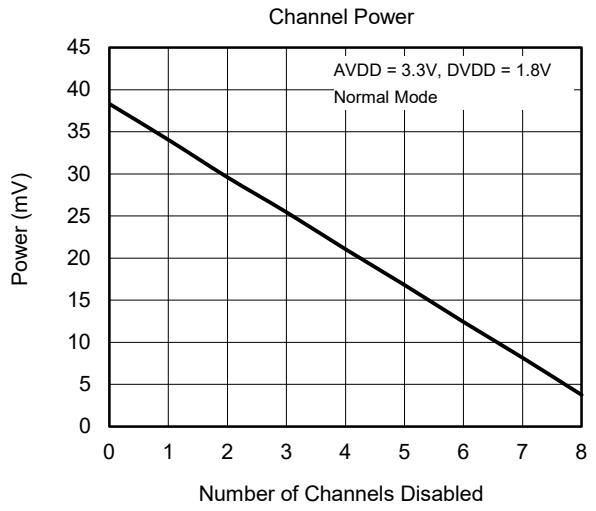
Offset Drift vs. PGA Gain

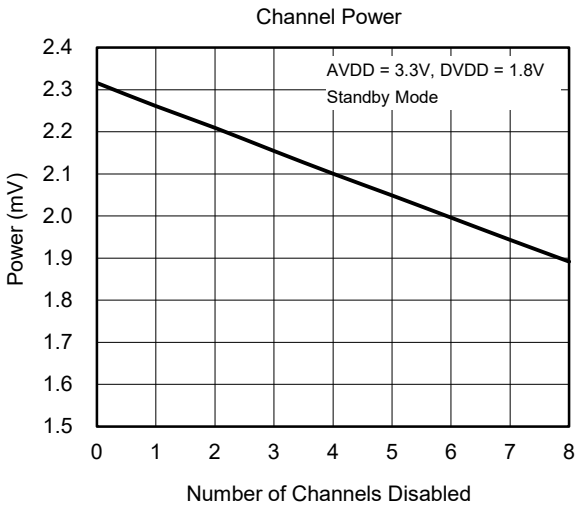


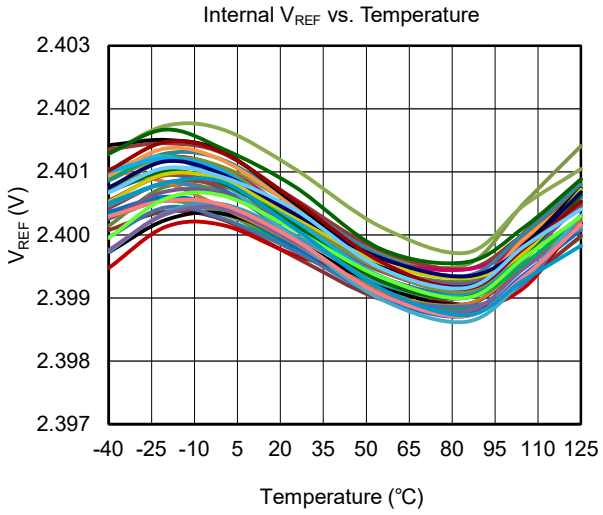
Channel Power

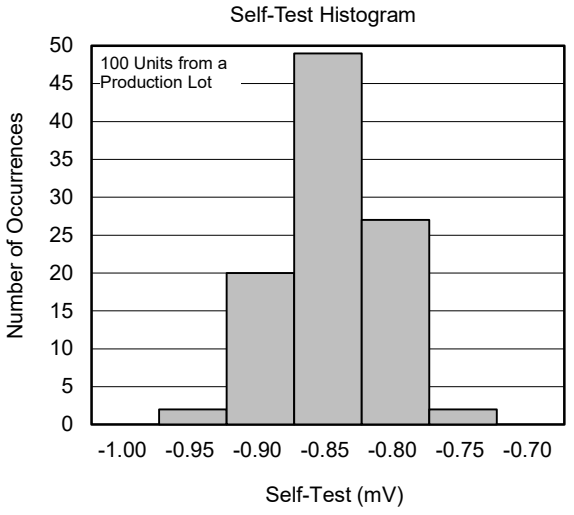


TYPICAL PERFORMANCE CHARACTERISTICS (continued)









SIMPLIFIED SCHEMATIC

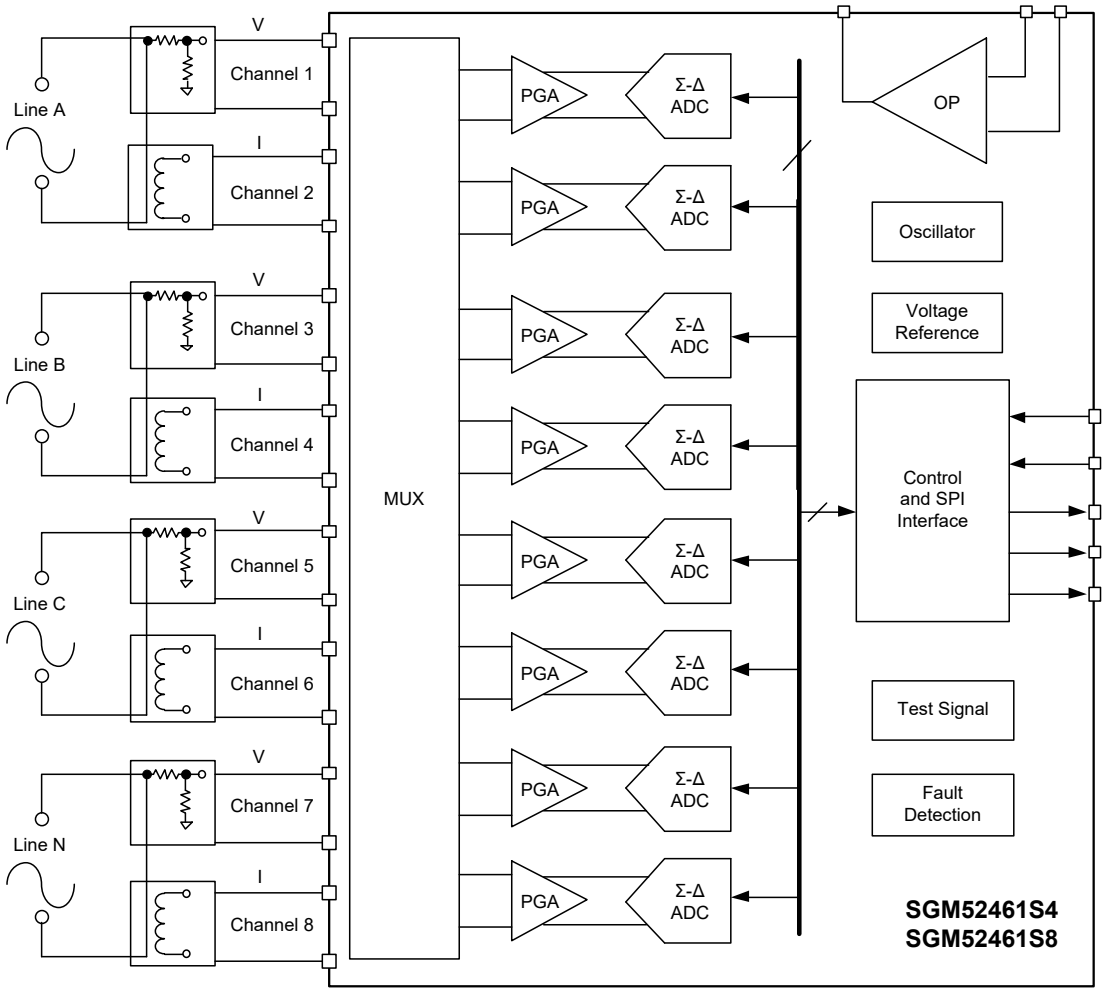
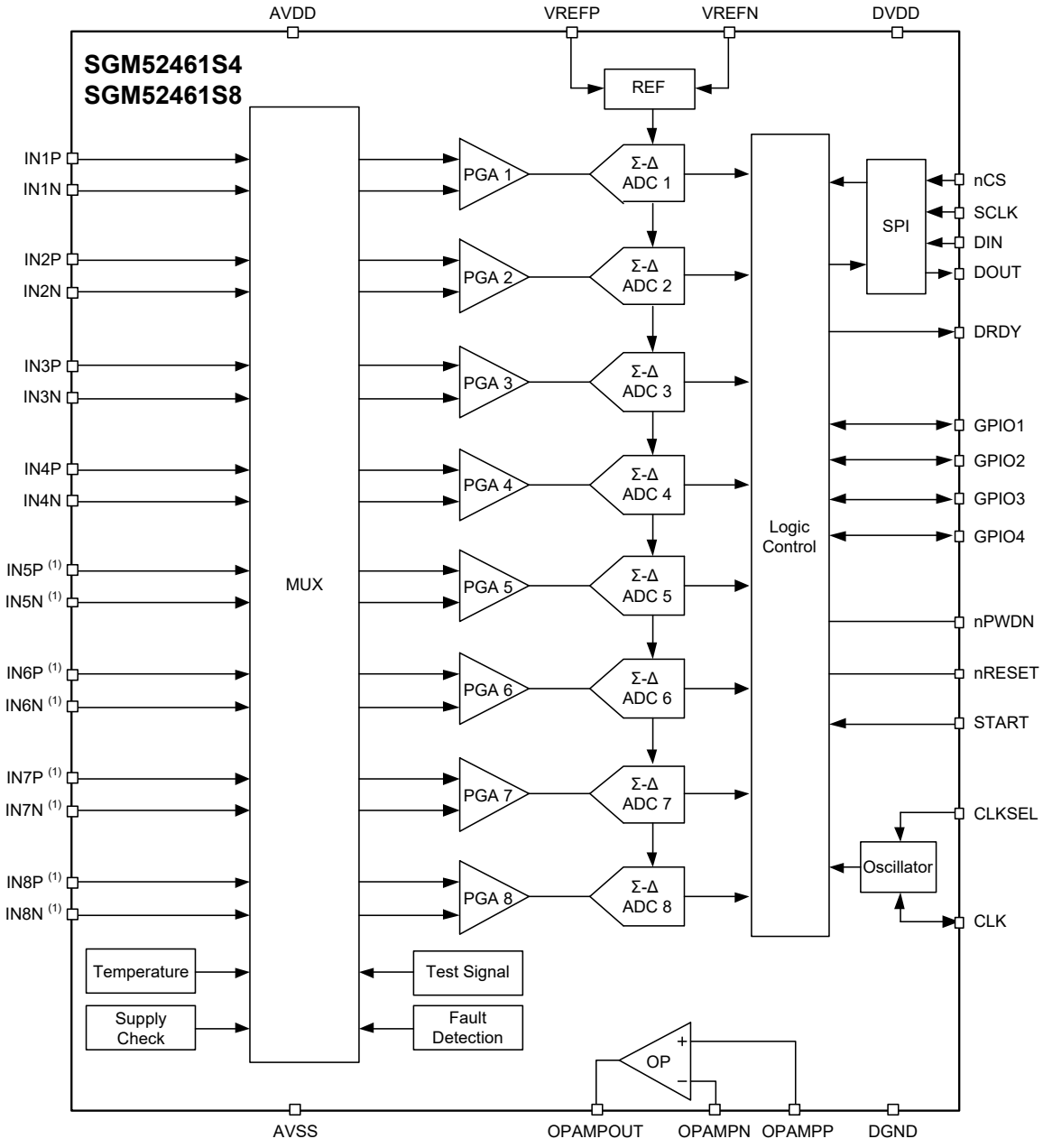


Figure 3. Simplified Schematic

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. SGM52461S8 only.

Figure 4. Block Diagram

PARAMETER MEASUREMENT INFORMATION

Noise Measurements

The SGM52461S4 and SGM52461S8 noise performance can be optimized by adjusting the data rate and PGA gain. When the data rate is reduced, noise improves correspondingly, making it useful for increasing averaging. On the other hand, increasing the PGA gain reduces input-referred noise, which is particularly helpful when measuring low-level signals. Table 1 and Table 2 summarize the noise performance of both devices with a 3V and 5V analog power supply, respectively. The data shown are representative of typical noise performance with inputs shorted together at T_A = +25℃. The RMS noise for each reading was calculated using a minimum of 1000 consecutive readings. The two highest data rates have limited noise due to ADC quantization noise and do not have a Gaussian distribution. Table 1 and Table 2 also show measurements taken with an internal reference, which is representative of the SGM52461S4/SGM52461S8 noise performance in effective number of bits (ENOB) and dynamic range when using a low-noise external reference. The ENOB data in the following table is calculated as Equation 1 and Equation 2, and the dynamic range data is calculated as Equation 3 and Equation 4.

$$ENOB_{Noise-RMS} = \log_2 \left| \frac{2 \times V_{REF}}{V_{RMS\_Noise} \times Gain} \right| \quad (1)$$

$$ENOB_{Noise-Free} = \log_2 \left| \frac{V_{REF}}{\sqrt{2} \times V_{RMS\_Noise} \times Gain} \right| \quad (2)$$

$$Dynamic\ Range_{Noise-RMS} = 20 \times \log_{10} \left| \frac{2 \times V_{REF}}{V_{RMS\_Noise} \times Gain} \right| \quad (3)$$

$$Dynamic\ Range_{Noise-Free} = 20 \times \log_{10} \left| \frac{V_{REF}}{\sqrt{2} \times V_{RMS\_Noise} \times Gain} \right| \quad (4)$$

Table 1. Input-Referred Noise-RMS (Noise-Free), AVDD = 3V, and Internal Reference = 2.4V

DR Bits (CONFIG1 Register)	Output Data Rate (kSPS)	-3dB Bandwidth (Hz)	PGA Gain									
			×1		×2		×4		×8		×12	
			Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB
000	64	16768	79.1 (70)	13.1 (11.6)	79.2 (70.1)	13.1 (11.6)	79 (70)	13.1 (11.6)	79 (69.9)	13.1 (11.6)	79.2 (70.2)	13.2 (11.7)
001	32	8384	96.4 (87.4)	16 (14.5)	96.7 (87.7)	16.1 (14.6)	96.6 (87.6)	16.1 (14.6)	96.3 (87.3)	16 (14.5)	96 (87)	16 (14.5)
010	16	4192	110.5 (101.5)	18.4 (16.9)	109.9 (100.9)	18.3 (16.8)	109.4 (100.3)	18.2 (16.7)	107.5 (98.5)	17.9 (16.4)	106 (97)	17.6 (16.1)
011	8	2096	117.9 (108.9)	19.6 (18.1)	117.1 (108.1)	19.5 (18)	115.7 (106.7)	19.2 (17.7)	112.9 (103.9)	18.8 (17.3)	110.7 (101.7)	18.4 (16.9)
100	4	1048	122 (113)	20.3 (18.8)	121.1 (112.1)	20.1 (18.6)	119.6 (110.6)	19.9 (18.4)	116.4 (107.4)	19.3 (17.8)	114.1 (105.1)	19 (17.5)
101	2	524	125.2 (116.2)	20.8 (19.3)	124.4 (115.4)	20.7 (19.2)	122.8 (113.7)	20.4 (18.9)	119.5 (110.5)	19.9 (18.4)	116.9 (107.9)	19.4 (17.9)
110	1	262	128.3 (119.3)	21.3 (19.8)	127.4 (118.4)	21.2 (19.7)	125.8 (116.8)	20.9 (19.4)	122.5 (113.5)	20.4 (18.9)	120 (111)	19.9 (18.4)

Table 2. Input-Referred Noise-RMS (Noise-Free), AVDD = 5V, and Internal Reference = 4V

DR Bits (CONFIG1 Register)	Output Data Rate (kSPS)	-3dB Bandwidth (Hz)	PGA Gain									
			×1		×2		×4		×8		×12	
			Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB	Dynamic Range (dB)	ENOB
000	64	16768	79.9 (70.8)	13.3 (11.8)	79.7 (70.7)	13.2 (11.7)	80.1 (71.1)	13.3 (11.8)	79.8 (70.8)	13.3 (11.8)	79.8 (70.8)	13.3 (11.8)
001	32	8384	96.5 (87.5)	16 (14.5)	96.5 (87.4)	16 (14.5)	96.5 (87.5)	16 (14.5)	96.3 (87.3)	16 (14.5)	96.2 (87.2)	16 (14.5)
010	16	4192	111 (101.9)	18.4 (16.9)	110.8 (101.8)	18.4 (16.9)	110.3 (101.3)	18.3 (16.8)	109.2 (100.2)	18.1 (16.6)	108 (98.9)	17.9 (16.4)
011	8	2096	119.5 (110.5)	19.9 (18.4)	119 (109.9)	19.8 (18.3)	118.1 (109)	19.6 (18.1)	115.9 (106.9)	19.3 (17.8)	114 (105)	18.9 (17.4)
100	4	1048	124.3 (115.3)	20.7 (19.2)	123.7 (114.6)	20.5 (19)	122.6 (113.6)	20.4 (18.9)	120 (111)	19.9 (18.4)	118 (109)	19.6 (18.1)
101	2	524	127.9 (118.9)	21.3 (19.8)	127.4 (118.4)	21.2 (19.7)	126.2 (117.1)	21 (19.5)	123.5 (114.4)	20.5 (19)	121.2 (112.2)	20.1 (18.6)
110	1	262	131.2 (122.2)	21.8 (20.3)	130.5 (121.4)	21.7 (20.2)	129.5 (120.4)	21.5 (20)	126.5 (117.4)	21 (19.5)	124.5 (115.4)	20.7 (19.2)

DETAILED DESCRIPTION

Overview

The SGM52461S4 and SGM52461S8 are advanced analog-to-digital converters that are designed for low-power, multichannel, simultaneously-sampling applications. These devices offer a scalable data rate, making them ideal for industrial power monitor, control, and protection applications.

The devices include a programmable multiplexer that enables measurement of various internal signals, such as temperature, supply voltage, and input short for noise testing. The PGA gain can be adjusted from one of five settings, and the ADCs offer data rates ranging from 1kSPS to 64kSPS. The devices communicate using an SPI-compatible interface and provide four GPIO pins for general use. Multiple devices can be used to add channels to the system and synchronize them with the START pins.

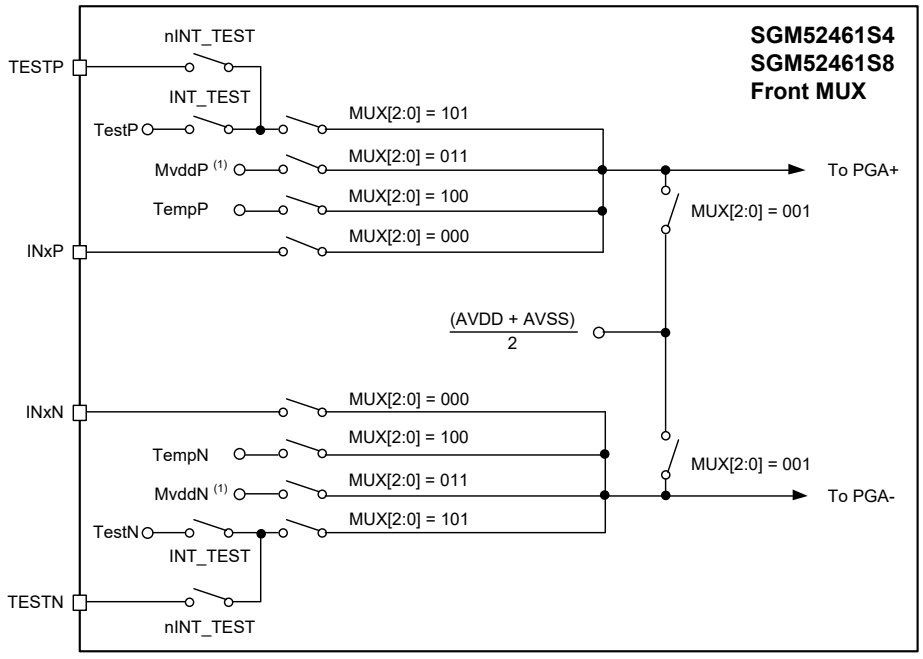
The internal reference can be programmed to either 2.4V or 4V, and the internal oscillator generates a 2.048MHz clock. The devices also feature integrated comparators with programmable trigger-points for input over-range or under-range detection. A detailed diagram of the SGM52461S4/ SGM52461S8 is provided for reference.

Input Multiplexer

The SGM52461S4 and SGM52461S8 input multiplexers offer a high degree of flexibility, with numerous signal-switching options that can be configured to suit specific needs. A diagram of the multiplexer on a single channel is illustrated in Figure 5, with separate INxP and INxN for each block, which can range from four to eight depending on the device. This level of flexibility enables extensive device and subsystem diagnostics, calibration, and configuration. To select switch settings for each channel, appropriate values need to be written to the CHnSET registers, as detailed in the General Register Maps section. Finally, each multiplexer output is connected to the individual channel PGA.

Device Noise Measurements

By setting CHnSET[2:0] = 001, the common mode voltage of [(V_{VREFP} + V_{VREFN})/2] is applied to both channel inputs. This setting is particularly useful for testing inherent device noise in the user system.



NOTE:

1. MVDD monitor voltage supply depends on channel number. Refer to the Power Supply Measurements (MVDDP, MVDDN) section.

Figure 5. Input Multiplexer Block for One Channel

DETAILED DESCRIPTION (continued)

Test Signals (TestP, TestN)

When CHnSET[2:0] = 101, the input multiplexer generates test signals that can be used for sub-system verification during power-up. The amplitude and switching frequency of the test signals are controlled through register settings, which can be found in the CONFIG2: Configuration Register 2 section. The INT_TEST register bit, also found in the CONFIG2 register, deactivates the internal test signals so that an external test signal can be used instead. This feature is particularly useful for testing or calibrating multiple devices with the same signal.

Temperature Sensor (TempP, TempN)

When CHnSET[2:0] = 100, the channel input is set to the temperature sensor. The temperature sensor in the device utilizes two internal diodes, with one diode having a current density 16 times greater than the other, as illustrated in Figure 6. This difference in current densities between the two diodes results in a voltage difference that is proportional to absolute temperature.

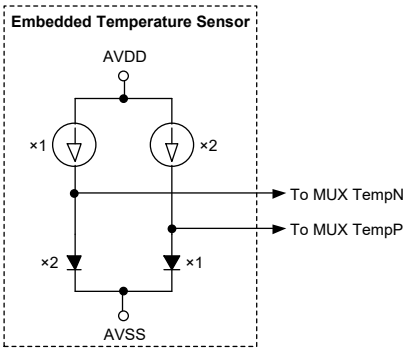


Figure 6. Temperature Sensor Implementation

The temperature of the internal device closely follows the PCB temperature due to the low thermal resistance of the package to the PCB. However, the SGM52461S4 and SGM52461S8 may produce a higher reading than the surrounding PCB due to self-heating. It is strongly suggested to set the channel gain to 1 during temperature measurement. Equation 5's scale factor converts the temperature reading to ℃, but the temperature reading code must first be scaled to μV before using this equation.

$$\text{Temperature (℃)} = \left[\frac{\text{Temperature Reading (μV)-145,000μV}}{\text{470μV / ℃}}\right] + 25℃ \quad (5)$$

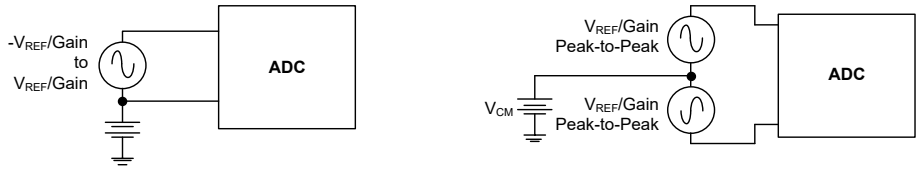
Power Supply Measurements (MVDDP, MVDDN)

When CHnSET[2:0] is set to 011, the channel inputs are configured to different device supply voltages. For channels 1, 2, 5, 6, 7, and 8, (MVDDP - MVDDN) is equal to [0.5 × (AVDD-AVSS)]. Meanwhile, for channels 3 and 4, (MVDDP - MVDDN) equal is to DVDD/4. To prevent the PGA from saturating when measuring power supplies, it is recommended to set the gain to 1.

Analog Input

The device's analog inputs are directly connected to an integrated programmable gain amplifier that has low noise, low drift, and high input impedance. The amplifier is positioned after the individual channel multiplexer.

The analog inputs of the SGM52461S4/SGM52461S8 are fully differential, and the differential input voltage (V_{INxP} - V_{INxN}) can range from - V_{REF}/Gain to V_{REF}/Gain. For details on how the analog input relates to digital codes, please see the Data Format section. There are two primary methods for driving the SGM52461S4/SGM52461S8 analog inputs: pseudo-differential or fully-differential, as depicted in Figure 7, Figure 8, and Figure 9.



(a). Psuedo-Differential Input (b). Differential Input

Figure 7. Methods of Driving the SGM52461S4/SGM52461S8: Pseudo-Differential or Fully Differential

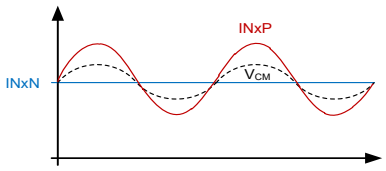


Figure 8. Pseudo-Differential Input Mode

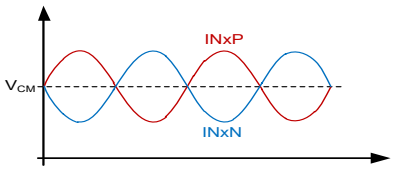


Figure 9. Fully-Differential Input Mode

DETAILED DESCRIPTION (continued)

To configure the fully differential input for a pseudo-differential signal, it is recommended to hold the INxN pin at a common voltage, ideally at mid supply. The INxP pin should be swung between -V_{REF}/Gain and V_{REF}/Gain, while staying within the absolute maximum specifications.

To implement a fully-differential input, set the signals at INxP and INxN to be 180° out of phase, centered around a common mode voltage, V_{CM}. Both inputs will vary from V_{CM} + ½ V_{REF}/Gain to V_{CM} - ½ V_{REF}/Gain. The differential voltage ranges from -V_{REF}/Gain to V_{REF}/Gain at the maximum and minimum points. For maximum dynamic range of the data converter, use the SGM52461S4/SGM52461S8 in a differential configuration. It is recommended to set the common mode voltage at the midpoint of the analog supplies [(AVDD + AVSS)/2] for optimal performance.

To conserve power, it is recommended to power down any unused analog input channels by using register bits. More information on how to power down individual channels can be found in the SPI Command Definitions section. Additionally, any unused or powered-down analog input pins should be tied directly to AVSS.

PGA Settings and Input Range

Each channel has its own PGA following its multiplexer. The gain can be set to one of five settings (1, 2, 4, 8, and12) for each individual channel using the CHnSET registers (refer to the General Register Maps section for details). The SGM52461S4 and SGM52461S8 have CMOS inputs, resulting in negligible current noise. Table 3 presents the typical small-signal bandwidth values corresponding to different gain settings.

Table 3. PGA Gain vs. Bandwidth

Gain	Nominal Bandwidth at T_A = +25℃ (kHz)
1	5206
2	4225
4	3306
8	2174
12	1612

Σ-Δ Modulator

The SGM52461S4 and SGM52461S8 channels are equipped with individual sigma-delta (Σ-Δ) ADCs. These Σ-Δ converters are designed with second-order modulators that are specifically optimized for low-power applications. The modulator takes samples of the input signal at the modulator rate of (f_{MOD} = f_{CLK}/2). Similar to other Σ-Δ modulators, the noise of the SGM52461S4/SGM52461S8 is shaped until f_{MOD}/2, as illustrated in Figure 10.

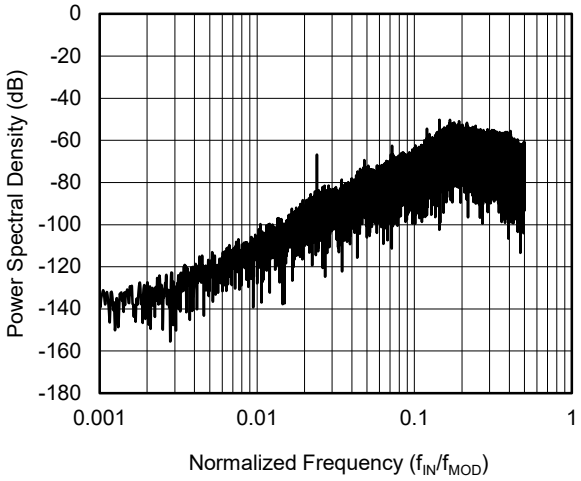


Figure 10. Modulator Noise Spectrum up to 0.5 × f_{MOD}

Clock

The SGM52461S4 and SGM52461S8 offer two distinct device clocking methods: internal and external. Internal clocking utilizes the internal oscillator and is best suited for low-power, non-synchronized systems. The internal oscillator is calibrated for accuracy at room temperature, but its precision may fluctuate across the specified temperature range. Refer to the Electrical Characteristics table for further information. External clocking is recommended for synchronizing multiple SGM52461S4/SGM52461S8 devices or when coordinating with an external event due to the potential variation in the internal oscillator's clock performance across temperature. The CLKSEL pin and the CLK_EN register bit control clock selection. The external clock should be provided after the analog and digital supplies are available.

The function of the CLKSEL pin is to choose between the internal oscillator and external clock. Meanwhile, the CLK_EN bit in the CONFIG1 register can turn on or off the output of the oscillator clock on the CLK pin. Table 4 shows a truth table for both the CLKSEL pin and CLK_EN bit. The CLK_EN bit is particularly useful in a daisy-chain setup with multiple devices. To conserve power during power-down, it is recommended to turn off the external clock.

Table 4. CLKSEL Pin and CLK_EN Bit

CLKSEL Pin	CLK_EN Bit	Clock Source	CLK Pin Status
0	X	External Clock	Input: External Clock
1	0	Internal Oscillator	3-State
1	1	Internal Oscillator	Output: Internal Oscillator

DETAILED DESCRIPTION (continued)

Digital Decimation Filter

The digital filter is responsible for receiving the bit stream output from the modulator and performing decimation on the data stream. The decimation ratio is determined by dividing the modulator rate by the data rate (f_{MOD}/f_{DR}), and this ratio influences the number of samples taken to generate the output data word. By adjusting the decimation ratio, it is possible to balance between resolution and data rate. A higher decimation ratio results in higher resolution, leading to lower data rates, while a lower decimation ratio decreases resolution but allows for wider bandwidths with higher data rates. Power applications typically require higher data rates, which can be achieved through software re-sampling techniques to aid with channel-to-channel phase adjustment for voltage and current.

Each channel's digital filter is comprised of a third-order sinc filter. It takes three conversion cycles for the filter to stabilize after an input step change. To modify the decimation ratio of the sinc3 filters, use the DR[2:0] bits in the CONFIG1 register (refer to the General Register Maps section for specific details). The data rate setting is a global setting that applies to all channels, ensuring that they operate at the same data rate.

The sinc filter is a low-pass filter with a variable decimation rate and third-order. It receives data from the modulator at the f_{MOD} rate. The sinc3 filter's primary function is to attenuate high-frequency modulator noise before decimating the data stream into parallel data. The decimation rate has a direct impact on the converter data rate.

Equation 6 provides the scaled Z-domain transfer function for the same filter.

$$\left|H(z)\right| = \left|\frac{1-Z^{-N}}{1-Z^{-1}}\right|^3 \quad (6)$$

Equation 7 illustrates the frequency domain transfer function of the sinc3 filter.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N\times\sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3 \quad (7)$$

where:

• N = Decimation ratio

The sinc3 filter exhibits notches or zeroes at the output data rate and its multiples, resulting in infinite attenuation at these frequencies. The frequency response and roll-off of the filter are illustrated in Figure 11 and Figure 12, respectively. Figure 13 and Figure 14 depict the filter transfer function up to $f_{MOD}/2$ and $f_{MOD}/16$, respectively, at varying data rates. The transfer function is extended up to 4 f_{MOD} in Figure 15, which shows that the SGM52461S4 and SGM52461S8 passband repeats itself every f_{MOD}. It should be noted that the digital filter response and notches are directly proportional to the master clock frequency.

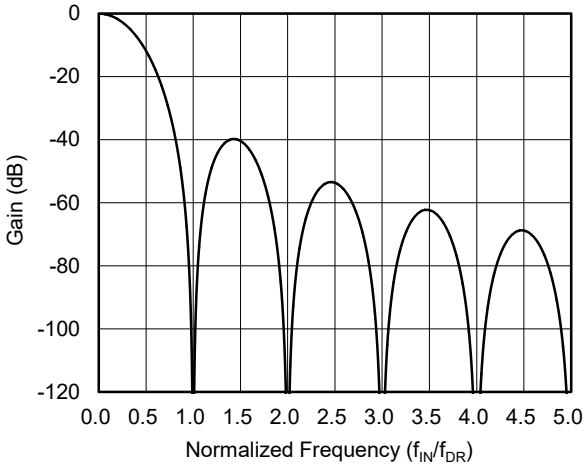


Figure 11. Sinc Filter Frequency Response

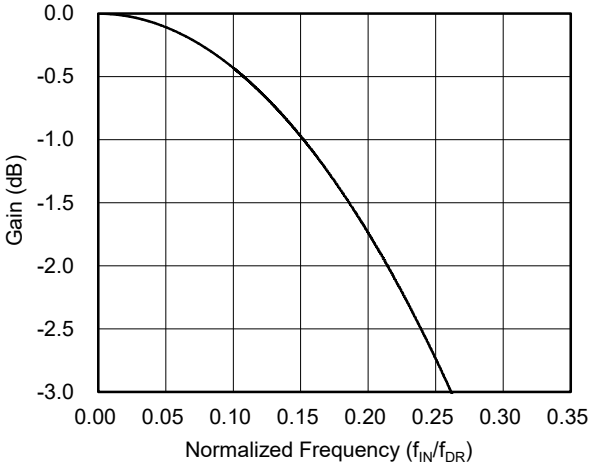


Figure 12. Sinc Filter Roll-Off

DETAILED DESCRIPTION (continued)

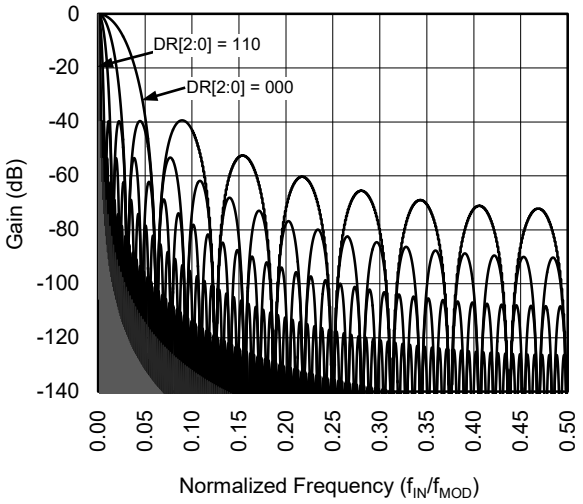


Figure 13. Transfer Function of Decimation Filters until $f_{MOD}/2$

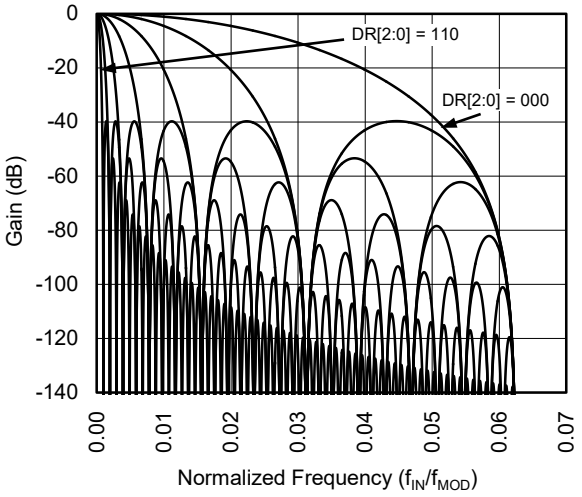


Figure 14. Transfer Function of Decimation Filters until $f_{MOD}/16$

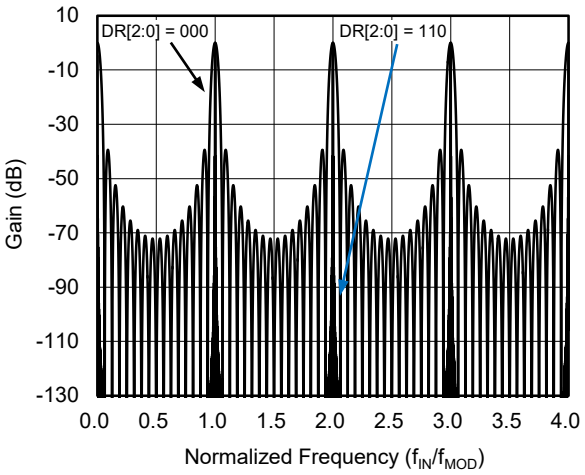
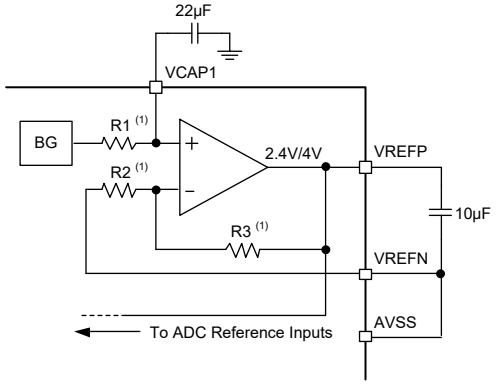


Figure 15. Transfer Function of Decimation Filters until 4 f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

DETAILED DESCRIPTION (continued)

Voltage Reference

A simplified block diagram of the internal reference for SGM52461S4/SGM52461S8 is presented in Figure 16. The reference voltage is generated in relation to AVSS. If the internal voltage reference is utilized, VREFN should be connected to AVSS.



NOTE: 1. For V_{REF} = 2.4V, R1 = 3.6kΩ, R2 = 25kΩ, and R3 = 25kΩ. For V_{REF} = 4V, R1 = 3.6kΩ, R2 = 15kΩ, and R3 = 35kΩ.

Figure 16. Internal Reference

The contribution of reference noise is determined by the external band-limiting capacitors. For the high-end systems, capacitor values should be selected to limit the bandwidth to less than 10Hz, preventing the reference noise from dominating the system noise. If a 3V analog supply is utilized, the internal reference must be set to 2.4V. For a 5V analog supply, the internal reference can be configured to 4V by adjusting the VREF_4V bit in the CONFIG2 register.

An external reference can also be used by powering down the internal reference buffer and driving VREFP externally. The PD_REFBUF bit in the CONFIG3 register controls the power-down function. This power-down feature is also utilized to share the internal references when two devices are cascaded. The device starts up in external reference mode by default.

Input Out-of-Range Detection

Integrated comparators are incorporated into the SGM52461S4/SGM52461S8 to detect out-of-range conditions on input signals. The input voltage is compared against a threshold voltage established by a 3-bit digital-to-analog converter (DAC) that is based on the analog power supply. The COMP_TH[2:0] bits in the FAULT register are responsible for setting the comparator trigger threshold level.

When powered by a ±2.5V supply and with COMP_TH[2:0] = 000 (95% and 5%), the SGM52461S4 and SGM52461S8 have a high-side trigger threshold of 2.25V [equivalent to AVSS + (AVDD - AVSS) × 95%] and a low-side threshold of -2.25V [equivalent to AVSS + (AVDD - AVSS) × 5%]. The threshold calculation formula is applicable to both unipolar and bipolar supplies.

To detect a fault condition, adjust the threshold level using the COMP_TH[2:0] bits accordingly. To identify which input is outside of the acceptable range, refer to the FAULT_STATP and FAULT_STATN registers separately or review the FAULT_STATx bits as part of the output data stream as described in the Data Output (DOUT) section.

General-Purpose Digital I/O (GPIO)

There are four general-purpose digital I/O (GPIO) pins available on the SGM52461S4/SGM52461S8. These pins can be configured as inputs or outputs using the GPIOC bits. The GPIOD bits in the GPIO register reflect the current status of the pins. The logic high voltage level for the GPIO is set by the DVDD voltage level. When reading the GPIOD bits, the returned data reflects the logic level of the pins, regardless of their input/output configuration. If a GPIO pin is set as an input, writing to the corresponding GPIOD bit will have no effect. However, if the pin is set as an output, writing to the GPIOD bit will set the output level.

If the GPIO pins are set as inputs, they must be driven to a defined state. The pins are configured as inputs after power-up or a reset. Figure 17 illustrates the GPIO pin structure. Any unused GPIO pins should be connected directly to DGND through 10kΩ resistors.

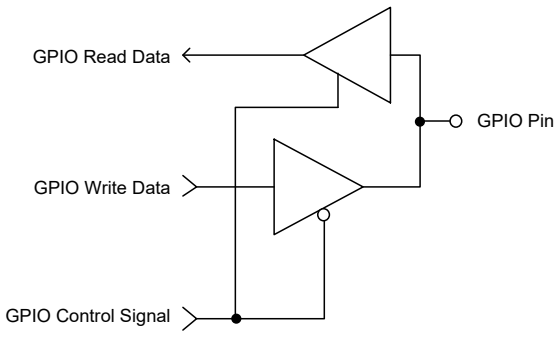


Figure 17. GPIO Pin Structure

DETAILED DESCRIPTION (continued)

Device Functional Modes

Start

To initiate conversions, either pull the START pin high for a minimum of 2 t_{CLK} periods or send the START command. If the START pin is low and the START command hasn't been issued, the device won't generate an nDRDY signal, and conversions will stop.

When managing conversions with the START command, ensure that the START pin remains in a low state. In configurations with multiple devices, the START pin is utilized to synchronize the devices.

Settling Time

The settling time (t_{SETTLE}) refers to the amount of time it takes for the converter to output fully-settled data after the START signal is activated and nDRDY is pulled high. The settling time is dependent on f_{CLK} and the decimation ratio, which is controlled by the DR[2:0] bits in the CONFIG1 register. Table 5 provides settling time data for different data rates as a function of t_{CLK}. After the initial settling time has passed, the falling edge of nDRDY occurs at the set data rate, t_{DR}. If data is not read from DOUT and the output shift register requires updating, the nDRDY signal will go high for 4 clock cycles (4 t_{CLK}) before returning low, signaling that new data is available. It is important to note that if there is a step change in the input signal while START is held high, it takes 3 × t_{DR} for the filter to settle to the new value. Settled data can be accessed on the fourth nDRDY pulse. See Figure 18.

Table 5. Settling Time for Different Data Rates

DR[2:0]	Normal Mode	Units
000	175	t_{CLK}
001	287	t_{CLK}
010	511	t_{CLK}
011	959	t_{CLK}
100	1855	t_{CLK}
101	3647	t_{CLK}
110	7231	t_{CLK}

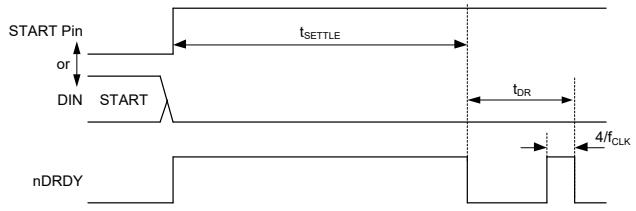


Figure 18. Settling Time

Input Signal Step

If the input signal experiences a step change while the device is converting, it takes 3 t_{DR} for the output data to fully settle. The settled data can be accessed on the fourth nDRDY pulse. While data can be accessed at each nDRDY low transition prior to the fourth pulse, it is recommended to ignore them. Figure 19 displays the necessary wait time for complete settling in the event of an input step or input transient on the analog input.

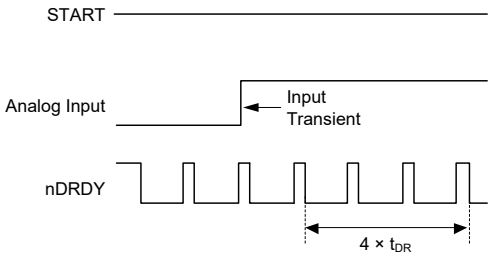


Figure 19. Settling Time for the Input Transient

Reset (nRESET)

There are two ways to reset the SGM52461S4/ SGM52461S8: either by pulling the nRESET pin low or by sending the RESET command. If using the nRESET pin, it is important to follow the minimum pulse duration timing specifications before returning the pin to a high state. The RESET command is activated on the eighth falling edge of the SCLK during the command sequence. Following a reset, it takes 18 t_{CLK} cycles to initialize the configuration registers to their default states and begin the conversion cycle. Additionally, it is important to note that whenever the CONFIG1 register is set to a new value using a WREG command, an internal reset is automatically triggered for the digital filter.

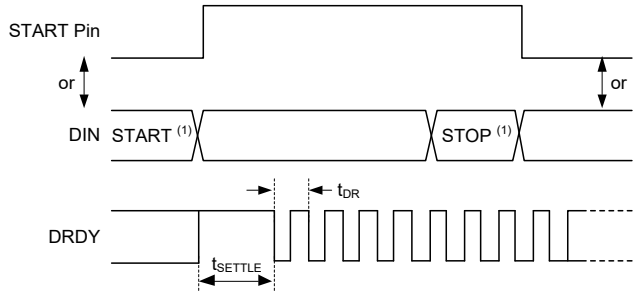
Power-Down (nPWDN)

Setting the nPWDN pin to a low state will shut down all on-chip circuitry. To exit power-down mode, the nPWDN pin should be set to a high state. Once out of power-down mode, the internal oscillator and reference will need time to wake up. To save power during power-down, it is advised to turn off the external clock.

DETAILED DESCRIPTION (continued)

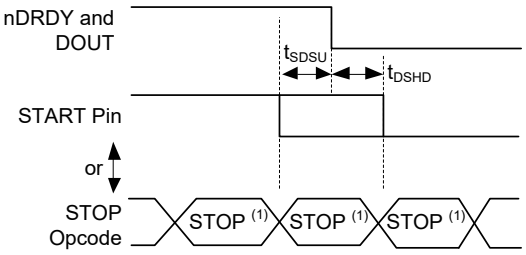
Continuous Conversion Mode

Conversions can begin either by taking the START pin high or by sending the START command. When conversions are initiated, the DRDY output goes high and then low when data is ready, as illustrated in Figure 20. The conversion process continues until the START pin is taken low or the STOP command is transmitted. If the START pin is pulled low or the STOP command is issued, the current conversion is allowed to complete before halting further conversions. The DRDY timing requirements for controlling conversions in this mode are shown in Figure 21 and Table 6. The t_{SDSU} timing specifies when to set the START pin to low or issue the STOP command before the DRDY falling edge to stop further conversions. The t_{DSHD} timing indicates when to set the START pin to low or send the STOP command after the DRDY falling edge to finish the current conversion and then stop further conversions. To maintain continuous conversion, the START pin can be permanently tied high.



NOTE: 1. The START and STOP commands are executed on the 7th falling edge of SCLK.

Figure 20. Continuous Conversion Mode



NOTE: 1. The START and STOP commands are executed on the 7th falling edge of SCLK at the end of the transmission.

Figure 21. START to nDRDY Timing

Table 6. Timing Characteristics for Figure 21 (1)

PARAMETER	SYMBOL	MIN	UNITS
Setup Time: START pin low or STOP command before the nDRDY falling edge to stop further conversions	t_{SDSU}	16	t_{CLK}
Delay Time: Time taken to set the START pin low or issue the STOP command in order to finish the current conversion and stop any additional conversions.	t_{DSHD}	16	t_{CLK}

NOTE: 1. The START and STOP commands are executed on the 7th falling edge of SCLK at the end of the transmission.

Data Retrieval

Data Ready (nDRDY)

The nDRDY signal is an output that switches from a high to a low state to indicate the availability of new conversion data. The nCS signal does not affect the nDRDY signal. The behavior of nDRDY depends on whether the device is in RDATAC mode or if the RDATA command is used to read data as needed. Please refer to the RDATAC: Start Read Data Continuous Mode and RDATA: Read Data subsections of the SPI Command Definitions section for more information.

When using the RDATA command to read data, it is possible to overlap the read operation with the next nDRDY occurrence without corrupting the data. The device can be placed in either normal data capture mode or pulse data capture mode by using the START pin or the START command.

Figure 22 illustrates the correlation between nCS, nDRDY, DOUT, and SCLK when retrieving data for an SGM52461S4/ SGM52461S8. DOUT is captured at the SCLK rising edge, while nDRDY is raised at the SCLK falling edge. It is important to note that nDRDY goes high on the initial SCLK falling edge, regardless of whether data retrieval is taking place or a command is being sent via the DIN pin.

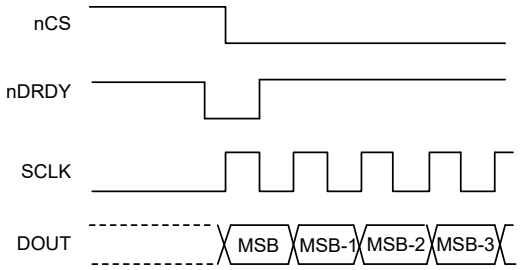


Figure 22. nDRDY Behavior with Data Retrieval

Regardless of the state of nCS, the nDRDY signal is reset on the first SCLK falling edge. This must be considered when using the SPI bus to communicate with other devices on the same bus. Figure 23 depicts the behavior of nDRDY when SCLKs are transmitted with nCS high. The diagram indicates that no data is transmitted, but the nDRDY signal is reset.

DETAILED DESCRIPTION (continued)

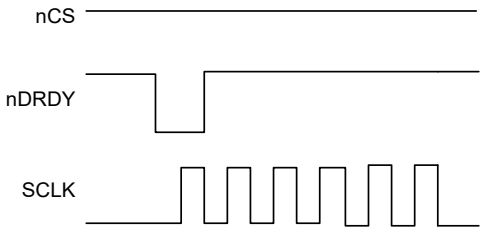


Figure 23. nDRDY and SCLK Behavior when nCS is High

Reading Back Data

There are two ways to retrieve data:

1. RDATAC: The read data continuous command enables the device to continuously read data without the need for commands. For more information, refer to the RDATAC: Start Read Data Continuous Mode section.

2. RDATA: To read the latest data, a command must be sent to the device to load the output shift register. For more information, refer to the RDATA: Read Data section.

Conversion data is obtained by shifting data out on DOUT. The most significant bit (MSB) of the data on DOUT is clocked out on the first SCLK rising edge. On the first SCLK falling edge, nDRDY returns high. DIN should remain low throughout the entire read operation.

Status Word

Before data readback, a status word is transmitted to provide information on the state of the SGM52461S4/SGM52461S8. The status word length is 24 bits and contains information for FAULT_STATP, FAULT_STATN, and the GPIO data bits. The alignment of the content is illustrated in Figure 24.

Note that the status word length is always 24 bits. The length does not change for 32kSPS and 64kSPS data rates.

Readback Length

The number of output bits is determined by the number of channels and bits per channel. Each channel's data format is twos complement and MSB first.

For the SGM52461S4/SGM52461S8 with data rates of 32kSPS and 64kSPS, the number of bits is 24 status bits + 16 bits per channel × 8 channels = 152, while for all other data rates, the number of data bits is: 24 status bits + 24 bits per channel × 8 channels 216.

When channels are powered down, their outputs are set to 0, but the sequence remains unchanged.

The SGM52461S4 and SGM52461S8 offer a multiple data readback feature, allowing data to be read out multiple times by providing more SCLKs. The DAISY_IN bit in the CONFIG1 register must be set to 1 for this feature.

Programming

Data Format

The CONFIG1 register's DR[2:0] bits determine the output resolution for the SGM52461S4/SGM52461S8. If DR[2:0] = 000 or 001, the 16 bits of each channel are transmitted in binary two's complement format, with the MSB first. Equation 8 is used to calculate the size of one code (LSB).

$$1LSB = (2 \times V_{REF}/Gain)/2^{16} = FS/2^{15} \quad (8)$$

If the input voltage is equal to or greater than the positive full-scale input [(FS - 1LSB) = (V_{REF}/Gain - 1LSB)], the output code will be 7FFFh. Conversely, if the input voltage is equal to or less than the negative full-scale input (-FS = -V_{REF}/Gain), the output code will be 8000h. If the input signal exceeds full-scale, the output will be clipped at these codes.

Table 7 provides a summary of the ideal output codes corresponding to various input signals.

Table 7. 16-Bit Ideal Output Code versus Input Signal

Input Signal, V_{IN} (V_{INxP} - V_{INxN})	Ideal Output Code (1)
≥ FS (2^{15} - 1)/2^{15}	7FFFh
FS/2^{15}	0001h
0	0000h
-FS/2^{15}	FFFFh
≤ -FS	8000h

NOTE:
1. Eliminate the impacts of noise, integral nonlinearity (INL), offset, and gain errors.

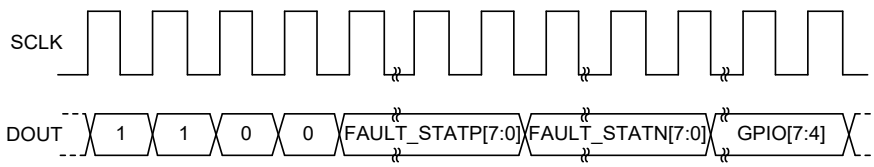


Figure 24. Status Word Content

DETAILED DESCRIPTION (continued)

When DR[2:0] is set to 010, 011, 100, 101, or 110, the SGM52461S4 and SGM52461S8 output 24 bits of each channel in binary two's complement format, starting with the most significant bit (MSB). Use Equation 9 to determine the size of one code (LSB).

$$1LSB = (2 \times V_{REF}/Gain)/2^{24} = FS/2^{23} \quad (9)$$

A positive full-scale input [$V_{IN} \geq (FS - 1LSB) = (V_{REF}/Gain - 1LSB)$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -FS = -V_{REF}/Gain$) produces an output code of 800000h. The output will clip at these codes for signals that go beyond full scale.

The ideal output codes for various input signals are shown in Table 8.

Table 8. 24-Bit Ideal Output Code versus Input Signal

Input Signal, V_{IN} (V_{INxP} - V_{INxN})	Ideal Output Code (1)
≥ FS (2^{23} - 1)/2^{23}	7FFFFFh
FS/2^{23}	000001h
0	000000h
-FS/2^{23}	FFFFFFh
≤ -FS	800000h

NOTE:
1. Eliminate the impact of noise, integral nonlinearity (INL), offset, and gain errors.

SPI Interface

The SGM52461S4 and SGM52461S8 utilize an SPI-compatible serial interface comprising four signals: nCS SCLK, DIN, and DOUT. This interface is responsible for reading conversion data, as well as reading and writing registers to control device operation. The nDRDY output serves as a status signal, indicating when ADC data are available for readback. When new data is available, nDYDR goes low.

Chip Select (nCS)

The SPI communication is initiated by activating the nCS pin. Before data transactions, nCS must be low and remain low throughout the entire SPI communication period. When nCS is high, the DOUT pin enters a high-impedance state, and any attempts to read from or write to the serial interface are ignored, and the interface is reset. The nDRDY pin operation is independent of nCS. Even when nCS is high, nDRDY will still indicate that a new conversion has completed and will be driven high in response to SCLK.

Raising nCS (chip select) to a high state only disables SPI (serial peripheral interface) communication with the device and resets the serial interface. However, data conversion still occurs and the nDRDY (data ready) signal can be monitored to determine if a new conversion result is available. If a master device is monitoring the nDRDY signal, it can select the appropriate slave device by lowering the nCS pin. After the serial communication is complete, it is important to wait for at least four t_{CLK} cycles before raising nCS to a high state.

Serial Clock (SCLK)

Serial communication is clocked by SCLK, which is a Schmitt-trigger input. However, it is recommended to minimize noise on SCLK to avoid unintentional data shifts caused by glitches. The data is shifted into DIN on the falling edge of SCLK and shifted out of DOUT on the rising edge of SCLK.

Figure 1 specifies the absolute maximum limit for SCLK. When sending commands with SCLK, it is important to issue the complete set of SCLKs to the device. Failure to do so can cause the device's serial interface to enter an unknown state, which can only be recovered by raising nCS to a high state.

The minimum speed required for SCLK for a single device depends on factors such as the number of channels, number of bits of resolution, and output data rate. However, for multiple devices, refer to the Multiple Device Configuration section for guidance on SCLK speed requirements.

As an example, when using SGM52461S4/SGM52461S8 in 8kSPS mode with 24-bit resolution, the minimum SCLK speed required is 1.755MHz to ensure that all data is shifted out.

The data can be retrieved from the device by either placing it in RDATAC mode or issuing an RDATA command for data on demand. The SCLK rate limitation specified in Equation 10 applies to the RDATAC mode. For the RDATA command, the restriction only applies when data must be read between two consecutive nDRDY signals. It is important to note that Equation 10 assumes that no other commands are issued between data captures.

$$t_{SCLK} < (t_{DR} - 4\ t_{CLK})/(N_{BITS} \times 8 + 24) \quad (10)$$

where

• N_{BITS} = Data resolution for the current data rate, 16 or 24

DETAILED DESCRIPTION (continued)

Data Input (DIN)

DIN is utilized in conjunction with SCLK to transmit information to the device. The device receives data from DIN on the falling edge of SCLK.

The communication method of this device is full-duplex, meaning that it can receive commands while simultaneously transmitting data. When transmitting a command, any data in present the output shift register will also be transmitted. Therefore, it is important to ensure that the data being sent on the DIN pin is valid when transmitting data out. If no command is being sent when reading data, the NOP command should be sent on DIN. When transmitting multiple byte commands on DIN, it is crucial to meet the $t_{SDECODE}$ timing in the Sending Multibyte Commands section.

Data Output (DOUT)

To retrieve conversion and register data from the device, DOUT is utilized in conjunction with SCLK. The data is transmitted on the rising edge of SCLK, with the MSB being transmitted first. When nCS is high, DOUT enters a high-impedance state. In read data continuous mode, DOUT can also be used to indicate when new data is available. If nCS is low when new data is available, a high-to-low transition will occur on the DOUT line simultaneously with a high-to-low transition on nDRDY. This feature is illustrated in Figure 25 and can be used to reduce the number of connections required between the device and system controller.

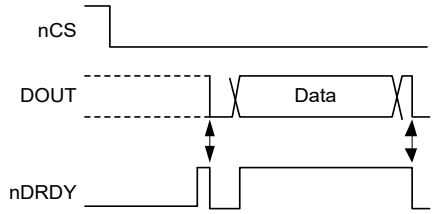
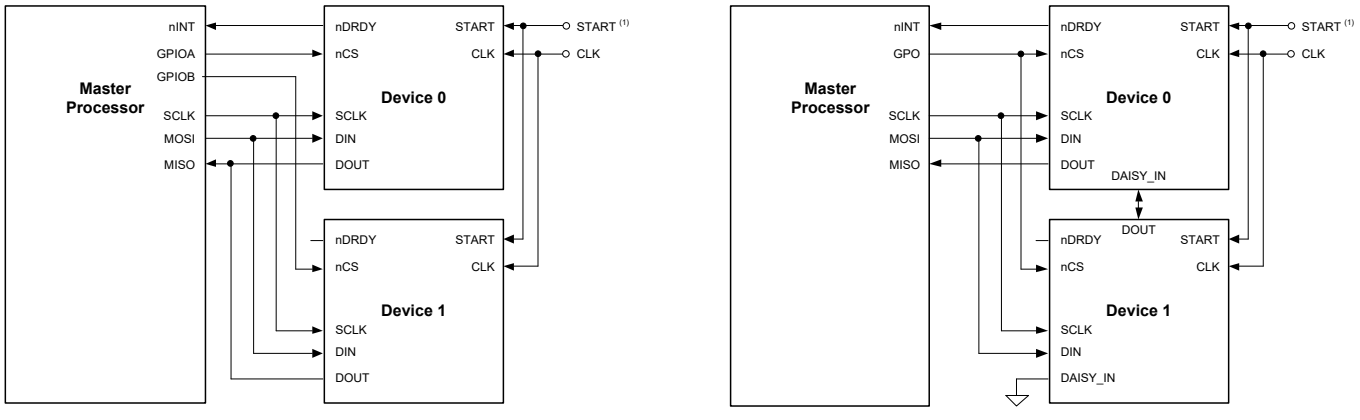


Figure 25. Using DOUT as nDRDY

Daisy-Chain Configuration

Daisy-chain mode is enabled through the configuration of the DAISY_IN bit in the CONFIG1 register, with the connection diagram provided in Figure 26. This mode allows the SCLK, DIN, and nCS pins to be shared among multiple devices in cascade. By connecting the DOUT pin of Device 1 to the DAISY_IN pin of Device 0, a daisy-chain data link is established. If Device 1 is not deployed in the system, its DAISY_IN pin must be connected to DGND. Timing specifications for the SPI interface under daisy-chain configuration are illustrated in Figure 2. The DOUT signal sequence starts with data from SGM52461S4/SGM52461S8 Device 0, followed by a don't-care bit, and then the status and data words from SGM52461S4/SGM52461S8 Device 1. Note that the internal oscillator cannot be enabled here. Since all devices in the chain share a single DIN pin, an external clock is required to ensure synchronous operation of the entire system.



NOTE:
1. For pin count optimization in system integration, the START pin is held at a low level, and the START command is adopted as the alternative control mechanism to synchronize and trigger the conversion process.

Figure 26. Multiple Device Configurations

DETAILED DESCRIPTION (continued)

SPI Command Definitions

The SGM52461S4 and SGM52461S8 offer versatile configuration control options. The device operation can be controlled and configured using the commands listed in Table 9. These commands are self-contained, with the exception of register read and register write operations that require an additional second command byte to include more data. It is possible to take nCS high or keeps it low between commands, but it must remain low for the entire command operation, including multibyte commands.

The SGM52461S4 and SGM52461S8 decode system commands and the RDATA command on the 7th falling edge of SCLK. Register and read write commands, on the other hand, are decoded on the 8th falling edge of SCLK. It is important to adhere to the SPI requirements timing when pulling nCS high after issuing a command.

Sending Multibyte Commands

The SGM52461S4 and SGM52461S8 serial interfaces utilize byte-based command decoding and necessitate a 4 t_{CLK} cycle duration for each command to be decoded and executed. Consequently, when transmitting multi-byte commands (e.g RREG or WREG), a 4 t_{CLK} interval must be observed between the conclusion of one byte or command and the initiation of the next.

Assuming a CLK frequency of 2.048MHz, the $t_{SDECODE}$ duration (4 t_{CLK}) is 1.96μs. If SCLK operates at 16MHz, a single byte can be transmitted in 0.5μs. However, this byte transfer time falls short of the $t_{SDECODE}$ requirement. Therefore, a delay of 1.46μs (1.96μs - 0.5μs) must be introduced between the first and second bytes. On the other hand, if SCLK operates at 4MHz, a byte transfer takes 2μs, which exceeds the $t_{SDECODE}$ specification (2μs > 1.96μs). As a result, the processor can send subsequent bytes without any delay.

WAKEUP: Exit Standby Mode

The WAKEUP command is responsible for exiting the low-power standby mode, as described in the "STANDBY: Enter Standby Mode" section. It is essential to provide sufficient time for all circuits in standby mode to power up, as specified in the Electrical Characteristics table. This command can be issued at any time.

Table 9. Command Definitions

Command	Description	First Byte	Second Byte
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start or restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversions	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
Data Read Commands			
RDATAC	Enable read data continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop read data continuous mode	0001 0001 (11h)	
RDATA	Read data by command	0001 0010 (12h)	
Register Read Commands			
RREG (3)	Read n nnnn registers starting at address r rrrr	001r rrrr (2xh) (2)	000n nnnn (2)
WREG (3)	Write n nnnn registers starting at address r rrrr	010r rrrr (4xh) (2)	000n nnnn (2)
RREG_PHASE (3)	Read n nnnn registers starting at address r rrrr	011r rrrr	000n nnnn
WREG_PHASE (3)	Write n nnnn registers starting at address r rrrr	110r rrrr	000n nnnn

NOTES:

1. When in RDATAC mode, the RREG command is ignored.
2. n nnnn represents the number of registers to be read or written - 1. For example, to read or write three registers, set n nnnn to 0 (0010). r rrrr indicates the starting register address for the read and write commands.
3. Command RREG and WREG are used to operate general registers (0x00 ~ 0x14), RREG_PHASE and WREG_PHASE are used to operate phase registers (0x00 ~ 0x0F).

DETAILED DESCRIPTION (continued)

STANDBY: Enter Standby Mode

The STANDBY command is responsible for initiating the low-power standby mode, whereby all circuits in the device, except for the reference section, are powered down. The power consumption during standby mode is specified in the Electrical Characteristics table. However, it is critical to note that once the device enters standby mode, no other commands, except for the WAKEUP command, should be transmitted.

After the START pin is pulled high, a START/OFFSETCAL/RESET command is issued, or the CONFIG1 register is rewritten, 35 t_{CLK} cycles should be waited before sending the STANDBY command.

RESET: Reset Registers to Default Values

The RESET command is responsible for resetting the digital filter and restoring all register settings to their default values, as specified in the Reset (nRESET) section. This command can be issued at any time. However, it is crucial to note that executing the RESET command requires 18 t_{CLK} cycles. During this period, it is advisable to refrain from transmitting any other commands.

START: Start Conversions

The START command initiates data conversions and can be controlled by setting the START pin to a low. However, if conversions are already in progress, this command will not have any effect. On the other hand, the STOP command is used to halt ongoing conversions. It is important to note that if the START and STOP commands are used consecutively, there must be a delay of at least 4 t_{CLK} cycles between them. The current conversion will be completed before further conversions are stopped. It is worth mentioning that this command can be executed at any time.

STOP: Stop Conversions

The STOP command is responsible for halting ongoing data conversions. It can be controlled by setting the START pin to a low. Once the STOP command is sent, the current conversion will be completed before further conversions are stopped. However, if conversions are already stopped, this command will not have any effect. It is worth noting that this command can be executed at any time.

OFFSETCAL: Channel Offset Calibration

The OFFSETCAL command is used to nullify the offset of each channel. It is suggested to issue the OFFSETCAL command every time there is a modification in the PGA gain settings.

The START pin shall be pulled high or the START command shall be sent before the OFFSETCAL command is issued.

When the OFFSETCAL command is issued, the device automatically sets the data rate to the lowest (DR[2:0] = 110, 1kSPS) and performs the following steps for each channel:

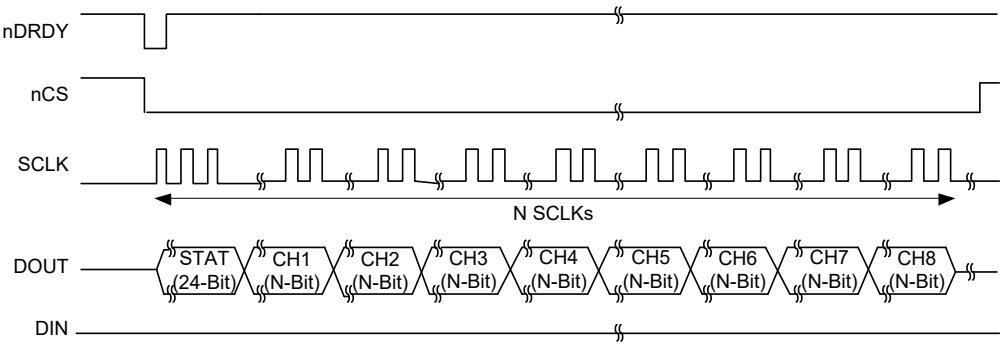
• Connect the analog inputs of each channel together and to the mid-supply voltage [(AVDD + AVSS)/2].
• Reset the digital filter (this requires a settling time of 4 t_{DR}).
• Gather 16 data points for calibration, taking 15 t_{DR}.

The total calibration time is calculated as (19 t_{DR} × 8) + 1ms, resulting in 153ms.

RDATAC: Start Read Data Continuous Mode

The RDATAC command is responsible for activating the read data continuous mode. In this mode, the data conversions can be accessed from the device without needing to send additional RDATA commands.

With every nDRDY falling edge, the conversion data is placed in the output register, which can be directly shifted out with the following SCLKs. To prevent data loss, it is important to shift out all data from the device before the data is updated with a new nDRDY falling edge. By default, the device operates in the read data continuous mode upon power-up. Figure 27 illustrates the SGM52461S4 and SGM52461S8 data output protocol when using RDATAC mode.



NOTE: X SCLKs = (N bits) (8 channels) + 24 bits. The N-bit depends on the DR[2:0] bits settings (N = 16 or 24).

Figure 27. SGM52461S4 and SGM52461S8 SPI Bus Data Output (Eight Channels)

DETAILED DESCRIPTION (continued)

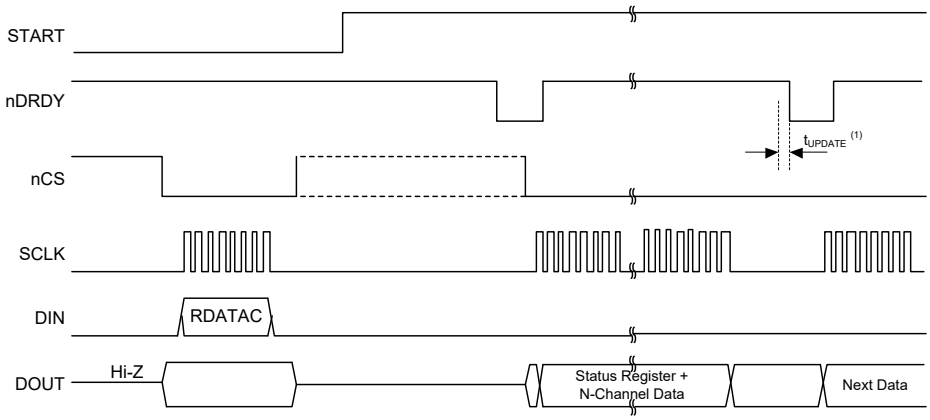
The Stop Read Data Continuous command cancels the RDATAC mode. If the device is in this mode, an SDATAC command must be sent before any other commands can be used. The subsequent data retrieval SCLKs or the SDATAC command shall wait for a minimum of 4 t_{CLK} cycles prior to completion. Figure 28 shows the timing for RDATAC, indicating a 4 t_{CLK} cycle keep-out zone around the nDRDY pulse during which this command cannot be issued. If no data is, retrieved a high-to-low DOUT transition occurs synchronously with nDRDY when nCS is held low to retrieve data. Ensure that the START pin is high or that the START command is issued after the RDATAC command. RDATAC ideal is for applications such as loggers or data recorders where registers are set once and do not require reconfiguration.

SDATAC: Stop Read Data Continuous Mode

The SDATAC command cancels the Read Data Continuous mode. It is worth noting that the next command must wait for at least 4 t_{CLK} cycles before completing.

RDATA: Read Data

When not in Read Data Continuous mode, the RDATA command loads the output shift register with the latest data. It should be issued after nDRDY goes low to read the conversion result. Unlike the SDATAC and RDATAC commands, subsequent commands or data retrieval SCLKs do not need to wait when this command is executed. To retrieve data from the device after issuing the RDATA command, ensure that the START pin is high or issue START command. The read operation can overlap the next nDRDY occurrence without data corruption, and the RDATA command can be sent multiple times after new data is available, supporting multiple data readback. Figure 29 illustrates the optimal usage of the RDATA command. This command is ideal for systems where it's necessary to read register settings or when timing control is not precise. Utilizing the RDATA command for data reading helps prevent corruption, especially if the nDRDY signal is not being monitored.



NOTE: 1. $t_{UPDATE} = 4/f_{CLK}$. Do not read data during this period.

Figure 28. Reading Data in RDATAC Mode

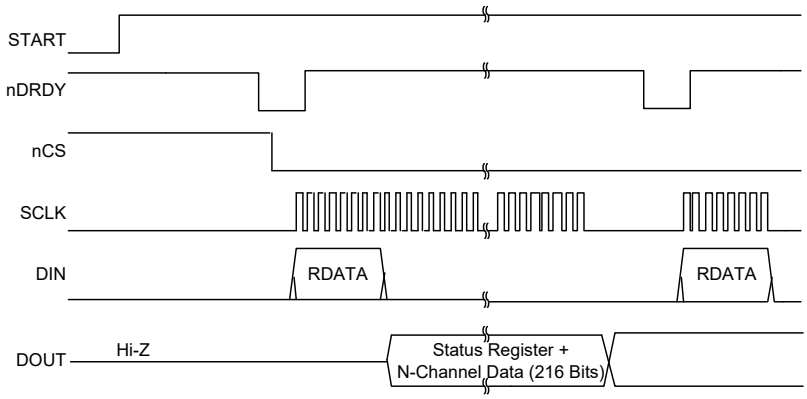


Figure 29. RDATA Usage

DETAILED DESCRIPTION (continued)

RREG: Read from Register

The RREG command is used to retrieve the contents of one or more configuration registers from the device. This two-byte command consists of a command and register address in the first byte, and the number of registers to read minus one in the second byte.

The first byte follows the format 001r rrrr, where r rrrr is the starting register address, while the second byte follows the format 000n nnnn, where n nnnn is the number of registers to read minus one.

During the operation, the MSB of the first register is clocked out on the 17th rising edge of SCLK, as illustrated in Figure 30. Before issuing the RREG command in read data continuous mode, an SDATAC command must be issued. Although the RREG command can be issued at any time, it is a multi-byte command that is subject to SCLK rate restrictions based on how the SCLKs are issued to meet the $t_{SDECODE}$ timing. For more information, refer to the Serial Clock (SCLK) subsection of the SPI Interface section. Note that nCS must remain low throughout the entire command.

WREG: Write to Register

The WREG command is used to write data to one or more configuration registers in the device. This two-byte command consists of a command and register address in the first byte, and the number of registers to write minus one in the second byte.

The first byte follows the format 010r rrrr, where r rrrr is the starting register address, while the second byte follows the format 000n nnnn, where n nnnn is the number of registers to write minus one.

Following the command bytes, the register data is inputted in MSB-first format, as illustrated in Figure 31. When performing multiple writes to the reserved registers (0Dh - 11h), you must include these registers in the total count and ensure that the default settings for the reserved registers are written as well.

The WREG command can be issued at any time, but it is a multi-byte command that is subject to SCLK rate restrictions based on how the SCLKs are issued to meet $t_{SDECODE}$ timing. Refer to Figure 1 for more details. Note that nCS must remain low throughout the entire command.

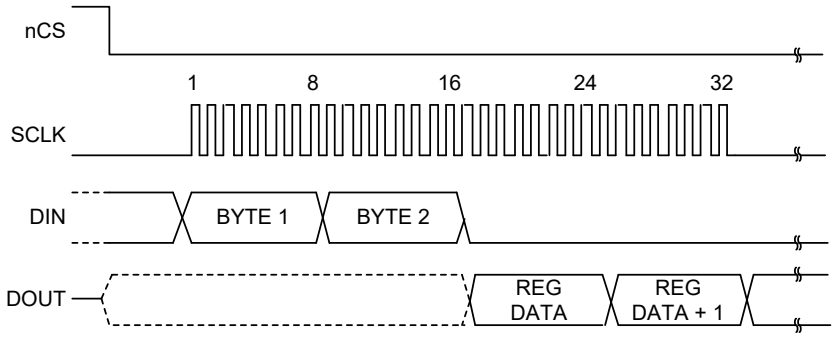


Figure 30. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (BYTE 1 = 0010 0000, BYTE 2 = 0000 0001)

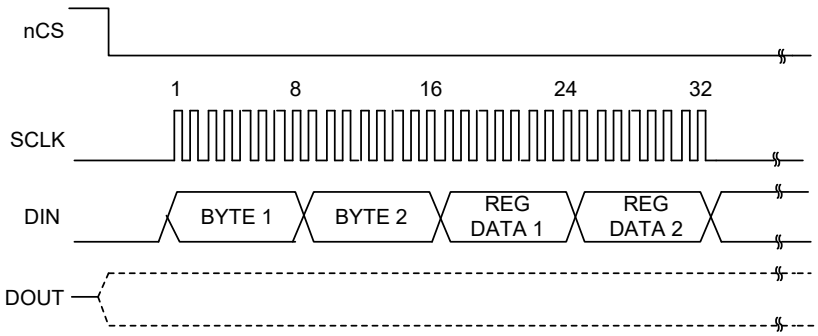


Figure 31. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (BYTE 1 = 0100 0000, BYTE 2 = 0000 0001)

GENERAL REGISTER MAPS

Table 10 shows the various SGM52461S4 and SGM52461S8 general registers.

Table 10. General Register Maps (1)

Register Address	Register Name	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Settings (Read-Only Registers)										
0x00	ID	xxh	REV_ID[2:0]			1	0	0	NU_CH2	NU_CH1
Global Settings across Channels										
0x01	CONFIG1	91h	1	DAISY_IN	CLK_EN	1	0	DR[2:0]		
0x02	CONFIG2	E0h	1	1	1	INT_TEST	0	TEST_AMP0	TEST_FREQ[1:0]	
0x03	CONFIG3	40h	PDB_REFBUF	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
0x04	FAULT	00h	COMP_TH[2:0]			0	0	0	0	0
Channel-Specific Settings										
0x05	CH1SET	10h	PD1	GAIN1[2:0]			0	MUX1[2:0]		
0x06	CH2SET	10h	PD2	GAIN2[2:0]			0	MUX2[2:0]		
0x07	CH3SET	10h	PD3	GAIN3[2:0]			0	MUX3[2:0]		
0x08	CH4SET	10h	PD4	GAIN4[2:0]			0	MUX4[2:0]		
0x09	CH5SET	10h	PD5	GAIN5[2:0]			0	MUX5[2:0]		
0x0A	CH6SET	10h	PD6	GAIN6[2:0]			0	MUX6[2:0]		
0x0B	CH7SET	10h	PD7	GAIN7[2:0]			0	MUX7[2:0]		
0x0C	CH8SET	10h	PD8	GAIN8[2:0]			0	MUX8[2:0]		
Fault Detect Status Registers (Read-Only Registers)										
0x12	FAULT_STATP	00h	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
0x13	FAULT_STATN	00h	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO Settings										
0x14	GPIO	0Fh	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

NOTE:

1. When executing multiple register write commands, make sure to set registers 0x0D, 0x0E, 0x0F, 0x10, and 0x11 to 00h.

REG0x00: ID Control Register (ID) (Factory-Programmed, Read-Only) [Reset = xxh]

This register is set during manufacturing to specify the device's characteristics.

Table 11. ID Control Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	REV_ID[2:0]	101	R	Device Family Identification 101 = SGM52461S4/SGM52461S8 (default) 000, 001, 010, 011, 100, 110, 111 = Reserved
D[4]	Reserved	1	R	Reserved. Always reads 1.
D[3:2]	Reserved	00	R	Reserved. Always reads 0.
D[1:0]	NU_CH[1:0]	xx	R	Device Identification Bits 00 = 4-channel device 01 = Reserved 10 = 8-channel device 11 = Reserved

GENERAL REGISTER MAPS (continued)

REG0x01: Configuration Register 1 (CONFIG1) [Reset = 91h]

The clock setting, daisy-chain, and each ADC channel sample rate are configured in this registers.

Table 12. Configuration Register 1 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	1	R/W	Reserved. Must be set to 1. This bit reads high.
D[6]	DAISY_IN	0	R/W	Daisy-Chain and Multiple Data Readback Mode 0 = Daisy-chain mode (default) 1 = Multiple data readback mode This bit is used to select which mode is enabled.
D[5]	CLK_EN	0	R/W	CLK Connection (1) 0 = Oscillator clock output disabled (default) 1 = Oscillator clock output enabled This bit determines whether the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1.
D[4]	Reserved	1	R/W	Reserved. Must be set to 1. This bit reads high.
D[3]	Reserved	0	R/W	Reserved. Must be set to 0. This bit reads low.
D[2:0]	DR[2:0]	001	R/W	Output Data Rate These bits are used to select the output data rate and resolution. Refer to Table 13 for details.

NOTE: 1. Driving external devices increases power consumption.

Table 13. Data Rate Settings

DR[2:0]	Resolution	Data Rate (kSPS) (1)
000	16-bit output	64
001	16-bit output	32 (default)
010	24-bit output	16
011	24-bit output	8
100	24-bit output	4
101	24-bit output	2
110	24-bit output	1
111	Do not use	NA

NOTE: 1. Where f_{CLK} = 2.048MHz. Data rates scale with master clock frequency.

REG0x02: Configuration Register 2 (CONFIG2) [Reset = E0h]

This register controls the generation of test signals. For more information, refer to the Input Multiplexer section.

Table 14. Configuration Register 2 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	111	R/W	Reserved. Must be set to 1. This bit reads high.
D[4]	INT_TEST	0	R/W	Test Signal Source 0 = Test signals are driven externally (default) 1 = Test signals are generated internally This bit determines the source for the test signal.
D[3]	Reserved	0	R/W	Reserved. Must be set to 0. This bit reads low.
D[2]	TEST_AMP	0	R/W	Test Signal Amplitude 0 = 1 × -(V_{VREFP} - V_{VREFN})/2400 (default) 1 = 2 × -(V_{VREFP} - V_{VREFN})/2400 This bit determines the calibration signal amplitude.
D[1:0]	TEST_FREQ[1:0]	00	R/W	Test Signal Frequency 00 = Pulsed at $f_{CLK}/2^{21}$ (default) 01 = Pulsed at $f_{CLK}/2^{20}$ 10 = Not used 11 = At DC These bits determine the test signal frequency.

GENERAL REGISTER MAPS (continued)

REG0x03: Configuration Register 3 (CONFIG3) [Reset = 40h]

This register sets up the operation of the reference and internal amplifier.

Table 15. Configuration Register 3 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PDB_REFBUF	0	R/W	Power-Down Reference Buffer 0 = Power-down internal reference buffer (default) 1 = Enable internal reference buffer This bit determines the power-down reference buffer state.
D[6]	Reserved	1	R/W	Reserved. Must be set to 1. This bit reads high.
D[5]	VREF_4V	0	R/W	Internal Reference Voltage 0 = VREF is set to 2.4V (default) 1 = VREF is set to 4V This bit determines the internal reference voltage (VREF).
D[4]	Reserved	0	R/W	Reserved. Must be set to 0. This bit reads low.
D[3]	OPAMP_REF	0	R/W	Operational Amplifier Reference 0 = Non-inverting input is linked to the OPAMPP pin (default) 1 = Non-inverting input is connected to (AVDD + AVSS)/2 This bit specifies if the non-inverting input of the operational amplifier is connected to the OPAMPP pin or to the internally generated supply (AVDD + AVSS)/2.
D[2]	PDB_OPAMP	0	R/W	Operational Amplifier Power-Down 0 = Power down the operational amplifier (default) 1 = Enable the operational amplifier This bit powers down the operational amplifier.
D[1]	Reserved	0	R/W	Reserved. Must be set to 0. Read back as 0.
D[0]	Reserved	0	R	Reserved. Reads back as either 1 or 0.

REG0x04: Fault Detect Control Register (FAULT) [Reset = 00h]

This register configures the fault detection operation.

Table 16. Fault Detect Control Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	COMP_TH[2:0]	000	R/W	Fault Detection Comparator Threshold These bits set the threshold level for the fault detection comparator. For a detailed explanation, refer to the Input Out-of-Range Detection section. Comparator High-side Threshold 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator Low-side Threshold 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
D[4:0]	Reserved	0 0000	R/W	Reserved. Must be set to 0. This bit reads low.

GENERAL REGISTER MAPS (continued)

REG0x05 ~ REG0x0C: Individual Channel Settings (CHnSET) [Reset = 10h]

This register allows for the customization of power mode, PGA gain, and multiplexer settings for individual channels. To learn more about the specific input multiplexer settings, please refer to the Input Multiplexer section. Each channel has its own corresponding CHnSET, which can be found in Table 10.

Table 17. CHnSET (1): Individual Channel Settings Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	PDn	0	R/W	Power-Down 0 = Normal operation (default) 1 = Channel power-down This bit selects the power mode for the specified channel. n = Individual channel number.
D[6:4]	GAINn[2:0]	001	R/W	PGA Gain 000 = Do not use 001 = 1 (default) 010 = 2 011 = Do not use 100 = 4 101 = 8 110 =12 111 = Do not use n = Individual channel number. These bits configure the gain setting for the PGA.
D[3]	Reserved	0	R/W	Reserved. Must be set to 0. This bit reads low.
D[2:0]	MUXn[2:0]	000	R/W	Channel Input 000 = Normal input (default) 001 = Input shorted to (AVDD + AVSS)/2 (for offset or noise measurements) 010 = Do not use 011 = MVDD for supply measurement 100 = Temperature sensor 101 = Test signal 110 = Do not use 111 = Do not use n = Individual channel number. These bits select the input for the channel.

NOTE:

1. n = 1 to 8.

GENERAL REGISTER MAPS (continued)

REG0x12: Fault Detect Positive Input Status (FAULT_STATP) [Reset = 00h]

The purpose of this register is to keep track of the status of the positive input on each channel and determine whether there is a fault or not. The threshold for detecting faults is set by Table 16, which can be found in the Input Out-of-Range Detection section.

Table 18. Fault Detect Positive Input Status Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	IN8P_FAULT	0	R	IN8P Threshold Detect 0 = Positive input pin of channel 8 does not exceed threshold set (default) 1 = Positive input pin of channel 8 exceeds threshold set
D[6]	IN7P_FAULT	0	R	IN7P Threshold Detect 0 = Positive input pin of channel 7 does not exceed threshold set (default) 1 = Positive input pin of channel 7 exceeds threshold set
D[5]	IN6P_FAULT	0	R	IN6P Threshold Detect 0 = Positive input pin of channel 6 does not exceed threshold set (default) 1 = Positive input pin of channel 6 exceeds threshold set
D[4]	IN5P_FAULT	0	R	IN5P Threshold Detect 0 = Positive input pin of channel 5 does not exceed threshold set (default) 1 = Positive input pin of channel 5 exceeds threshold set
D[3]	IN4P_FAULT	0	R	IN4P Threshold Detect 0 = Positive input pin of channel 4 does not exceed threshold set (default) 1 = Positive input pin of channel 4 exceeds threshold set
D[2]	IN3P_FAULT	0	R	IN3P Threshold Detect 0 = Positive input pin of channel 3 does not exceed threshold set (default) 1 = Positive input pin of channel 3 exceeds threshold set
D[1]	IN2P_FAULT	0	R	IN2P Threshold Detect 0 = Positive input pin of channel 2 does not exceed threshold set (default) 1 = Positive input pin of channel 2 exceeds threshold set
D[0]	IN1P_FAULT	0	R	IN1P Threshold Detect 0 = Positive input pin of channel 1 does not exceed threshold set (default) 1 = Positive input pin of channel 1 exceeds threshold set

GENERAL REGISTER MAPS (continued)

REG0x13: Fault Detect Negative Input Status (FAULT_STATN) [Reset = 00h]

Similar to the previous register, this register also keeps track of the status of each channel. However, it specifically monitors the negative input and determines whether there is a fault or not based on a threshold set by Table 16 in the Input Out-of-Range Detection section.

Table 19. Fault Detect Negative Input Status Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	IN8N_FAULT	0	R	IN8N Threshold Detect 0 = Negative input pin of channel 8 does not exceed threshold set (default) 1 = Negative input pin of channel 8 exceeds threshold set
D[6]	IN7N_FAULT	0	R	IN7N Threshold Detect 0 = Negative input pin of channel 7 does not exceed threshold set (default) 1 = Negative input pin of channel 7 exceeds threshold set
D[5]	IN6N_FAULT	0	R	IN6N Threshold Detect 0 = Negative input pin of channel 6 does not exceed threshold set (default) 1 = Negative input pin of channel 6 exceeds threshold set
D[4]	IN5N_FAULT	0	R	IN5N Threshold Detect 0 = Negative input pin of channel 5 does not exceed threshold set (default) 1 = Negative input pin of channel 5 exceeds threshold set
D[3]	IN4N_FAULT	0	R	IN4N Threshold Detect 0 = Negative input pin of channel 4 does not exceed threshold set (default) 1 = Negative input pin of channel 4 exceeds threshold set
D[2]	IN3N_FAULT	0	R	IN3N Threshold Detect 0 = Negative input pin of channel 3 does not exceed threshold set (default) 1 = Negative input pin of channel 3 exceeds threshold set
D[1]	IN2N_FAULT	0	R	IN2N Threshold Detect 0 = Negative input pin of channel 2 does not exceed threshold set (default) 1 = Negative input pin of channel 2 exceeds threshold set
D[0]	IN1N_FAULT	0	R	IN1N Threshold Detect 0 = Negative input pin of channel 1 does not exceed threshold set (default) 1 = Negative input pin of channel 1 exceeds threshold set

REG0x14: General-Purpose IO Register (GPIO) [Reset = 0Fh]

This register controls the format and state of the four GPIO pins.

Table 20. General-Purpose IO Register Details

BITS	BIT NAME		DEFAULT	TYPE	DESCRIPTION
D[7:4]	GPIOD[3:0]	GPIOD4	0000	R/W	GPIO Data These bits allow reading from and writing to the GPIO ports. When read this register, it shows the current state of the GPIO external pins, regardless of whether they are configured as inputs or outputs. Writing to the GPIOD sets the output value if the pins are configured as outputs. However, writing to the GPIOD has no effect if the pins are set as inputs.
		GPIOD3			
		GPIOD2			
		GPIOD1			
D[3:0]	GPIOC[3:0]	GPIOC4	1111	R/W	GPIO Control (Corresponding to GPIOD) 0 = Output 1 = Input (default) These bits indicate whether the specified GPIOD pin is configured as an input or an output.
		GPIOC3			
		GPIOC2			
		GPIOC1			

PHASE REGISTER MAPS

Table 21 shows the various SGM52461S4 and SGM52461S8 channel phase calibration registers.

Table 21. Phase Register Maps

Register Address	Register Name	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Phase Calibration										
0x00	CH1_PHASE	00h	PHASE1[9:2]							
0x01		00h	PHASE1[1:0]		Reserved					
0x02	CH2_PHASE	00h	PHASE2[9:2]							
0x03		00h	PHASE2[1:0]		Reserved					
0x04	CH3_PHASE	00h	PHASE3[9:2]							
0x05		00h	PHASE3[1:0]		Reserved					
0x06	CH4_PHASE	00h	PHASE4[9:2]							
0x07		00h	PHASE4[1:0]		Reserved					
0x08	CH5_PHASE	00h	PHASE5[9:2]							
0x09		00h	PHASE5[1:0]		Reserved					
0x0A	CH6_PHASE	00h	PHASE6[9:2]							
0x0B		00h	PHASE6[1:0]		Reserved					
0x0C	CH7_PHASE	00h	PHASE7[9:2]							
0x0D		00h	PHASE7[1:0]		Reserved					
0x0E	CH8_PHASE	00h	PHASE8[9:2]							
0x0F		00h	PHASE8[1:0]		Reserved					

REG0x00/01: CH1_PHASE Register [Reset = 00h/00h]

Table 22. CH1_PHASE Register in REG0x00 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE1[9:2]	0000 0000	R/W	Channel 1 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 23. CH1_PHASE Register in REG0x01 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE1[1:0]	00	R/W	Channel 1 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

PHASE REGISTER MAPS (continued)

REG0x02/03: CH2_PHASE Register [Reset = 00h/00h]

Table 24. CH2_PHASE Register in REG0x02 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE2[9:2]	0000 0000	R/W	Channel 2 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 25. CH2_PHASE Register in REG0x03 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE2[1:0]	00	R/W	Channel 2 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

REG0x04/05: CH3_PHASE Register [Reset = 00h/00h]

Table 26. CH3_PHASE Register in REG0x04 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE3[9:2]	0000 0000	R/W	Channel 3 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 27. CH3_PHASE Register in REG0x05 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE3[1:0]	00	R/W	Channel 3 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

REG0x06/07: CH4_PHASE Register [Reset = 00h/00h]

Table 28. CH4_PHASE Register in REG0x06 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE4[9:2]	0000 0000	R/W	Channel 4 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 29. CH4_PHASE Register in REG0x07 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE4[1:0]	00	R/W	Channel 4 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

PHASE REGISTER MAPS (continued)

REG0x08/09: CH5_PHASE Register [Reset = 00h/00h]

Table 30. CH5_PHASE Register in REG0x08 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE5[9:2]	0000 0000	R/W	Channel 5 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 31. CH5_PHASE Register in REG0x09 Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE5[1:0]	00	R/W	Channel 5 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

REG0x0A/0B: CH6_PHASE Register [Reset = 00h/00h]

Table 32. CH6_PHASE Register in REG0x0A Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE6[9:2]	0000 0000	R/W	Channel 6 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 33. CH6_PHASE Register in REG0x0B Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE6[1:0]	00	R/W	Channel 6 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

REG0x0C/0D: CH7_PHASE Register [Reset = 00h/00h]

Table 34. CH7_PHASE Register in REG0x0C Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE7[9:2]	0000 0000	R/W	Channel 7 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 35. CH7_PHASE Register in REG0x0D Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE7[1:0]	00	R/W	Channel 7 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

PHASE REGISTER MAPS (continued)

REG0x0E/0F: CH8_PHASE Register [Reset = 00h/00h]

Table 36. CH8_PHASE Register in REG0x0E Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	PHASE8[9:2]	0000 0000	R/W	Channel 8 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.

Table 37. CH8_PHASE Register in REG0x0F Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	PHASE8[1:0]	00	R/W	Channel 8 Phase Delay Phase day in modulator clock cycles provided in two's complement format, see Table 38.
D[5:0]	Reserved	00 0000	R	Reserved. Default read 000000b.

Channel Phase Calibration

The valid settling range is from -OSR/2 to OSR/2 - 1. If a value outside of -OSR/2 and OSR/2 - 1 is programmed, the device internally clips the value to the nearest limit.

Table 38. Phase Calibration Settling Limits for Different OSR Settlings

OSR Setting	Data Rate (SPS)	Phase Offset Range	PHASEn[9:0] Bits Range (1)
16	64k	-8 to 7	11 1111 1000b to 00 0000 0111b
32	32k	-16 to 15	11 1111 0000b to 00 0000 1111b
64	16k	-32 to 31	11 1110 0000b to 00 0001 1111b
128	8k	-64 to 63	11 1100 0000b to 00 0011 1111b
256	4k	-128 to 127	11 1000 0000b to 00 0111 1111b
512	2k	-256 to 255	11 0000 0000b to 00 1111 1111b
1024	1k	-512 to 511	10 0000 0000b to 01 1111 1111b

NOTE:
1. n = 1 to 8.

Follow these steps to create a phase shift larger than half the sample period for OSRs:

• Create a phase shift corresponding to an integer number of sample periods by modifying the indices between channel data in software.

• Use the phase calibration function to create the remaining fractional sample period phase shift.

REVISION HISTORY

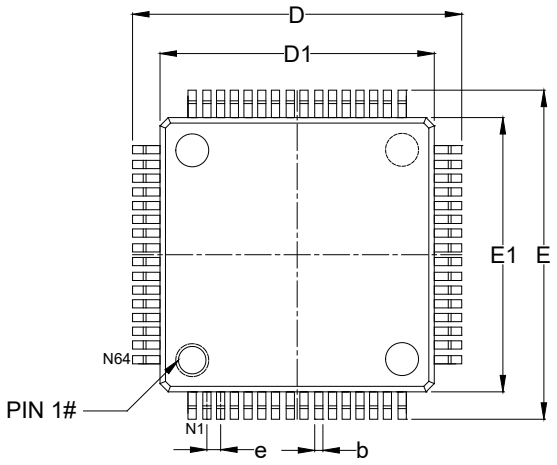
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2026 – REV.A to REV.A.1 **Page**

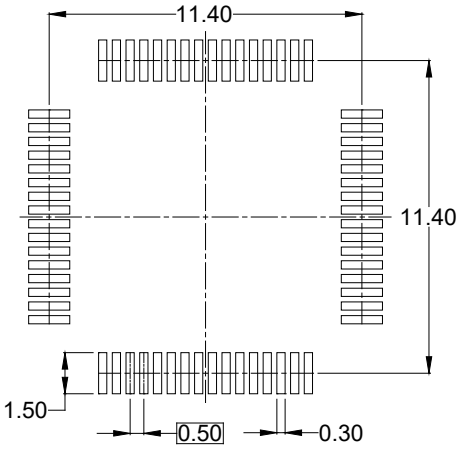
Changes from Original to REV.A (DECEMBER 2025) **Page**

PACKAGE OUTLINE DIMENSIONS

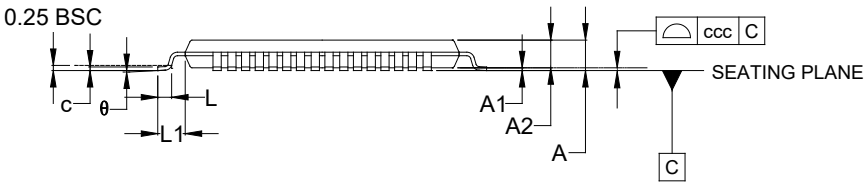
TQFP-10×10-64L



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



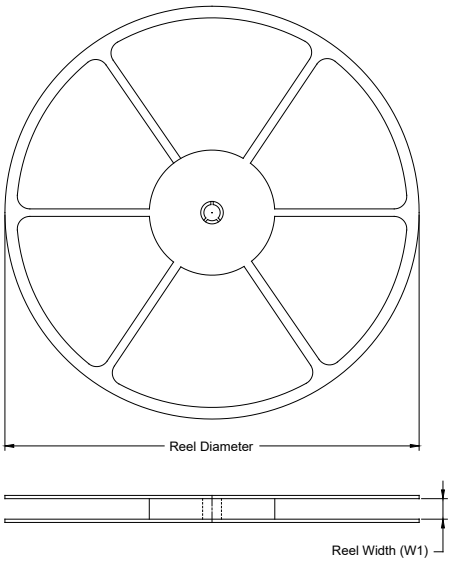
SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2		1.000 REF	
b	0.170	-	0.270
c	0.090	-	0.180
D	11.800	-	12.200
D1	9.900	-	10.100
E	11.800	-	12.200
E1	9.900	-	10.100
e		0.500 BSC	
L	0.450	-	0.750
L1		1.000 REF	
θ	0°	-	7°
ccc		0.080	

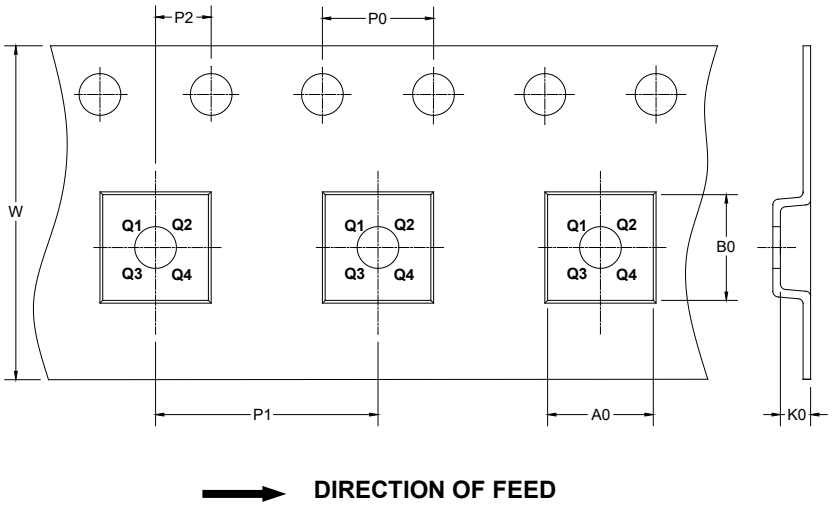
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-026.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



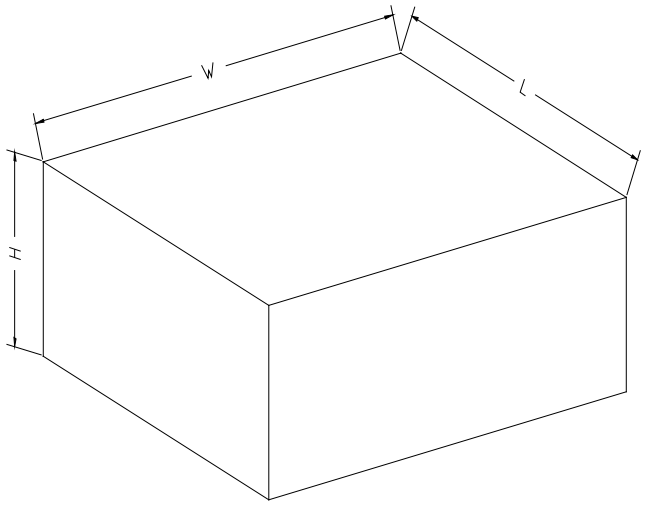
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFP-10×10-64L	13″	24.4	12.70	12.70	1.70	4.0	16.0	2.0	24.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002