SGM51623D
16-Bit, 2MSPS, 1-Channel, True-Differential Input, Serial Interface ADC

GENERAL DESCRIPTION

The SGM51623D is a 16-bit, 1-channel input, successive approximation (SAR) analog-to-digital converter (ADC).

The SGM51623D is a low power and low noise ADC. It is powered with 1.8V. The differential input range is $-V_{REF}$ to $+V_{REF}$. The external reference voltage range is 4.096V to 5.1V.

The SGM51623D has an SPI-compatible interface. And it has a separate digital power supply for the digital interface circuitry. The digital power supply range is 1.71V to 5.5V.

The SGM51623D is available in Green MSOP-10 and TDFN-3×3-10L packages. It is specified from -40℃ to +125℃.

APPLICATIONS

Battery-Powered Equipment
Machine Automation
Medical Equipment
Precision Data Acquisition Systems
Automatic Test Equipment

FEATURES

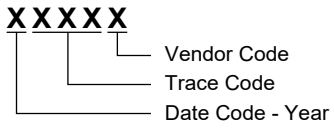
- **Throughput: 2MSPS**
- **Guaranteed 16-Bit No Missing Codes**
- **Integral Nonlinearity (INL):**
  - **-2.5LSB to +2.5LSB (-38.1ppm to +38.1ppm) for MSOP Package**
  - **-2LSB to +2LSB (-30.5ppm to +30.5ppm) for TDFN Package**
- **Differential Nonlinearity (DNL):**
  - **-0.999LSB to +1.5LSB for MSOP Package**
  - **-0.999LSB to +1LSB for TDFN Package**
- **Low Power Consumption:**
  - **11.2mW (TYP) at 1MSPS, VDD Only**
  - **13.9mW (TYP) at 1MSPS, 27.4mW (TYP) at 2MSPS Total**
- **Signal-to-Noise Ratio (SNR):**
  - **96dBFS (TYP) for MSOP Package at 1kHz and V_{REF} = 5V**
  - **96dBFS (TYP) for TDFN Package at 1kHz and V_{REF} = 5V**
- **Total Harmonic Distortion (THD):**
  - **-109.4dBFS (TYP) for MSOP Package at 1kHz and V_{REF} = 5V**
  - **-117.3dBFS (TYP) for TDFN Package at 1kHz and V_{REF} = 5V**
- **True-Differential Input**
- **First Accurate Conversion**
- **SPI-Compatible Serial Interface**
- **Support Daisy-Chain Multiple ADCs**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in Green MSOP-10 and TDFN-3×3-10L Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51623D	MSOP-10	-40℃ to +125℃	SGM51623DXMS10G/TR	SGM1S9 XMS10 XXXXX	Tape and Reel, 4000
			SGM51623DXMS10SG/TR	SGM1S9 XMS10 XXXXX	Tape and Reel, 500
	TDFN-3×3-10L	-40℃ to +125℃	SGM51623DXTD10G/TR	SGM 1S8D XXXXX	Tape and Reel, 4000
			SGM51623DXTD10SG/TR	SGM 1S8D XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs

AINP, AINM to GND (1)

..... (-0.3V to V_{REF} + 0.4V) or ±50mA (2)

Supply Voltage

REF, VIO to GND..... -0.3V to 6V

VDD to GND ..... -0.3V to 2.1V

VDD to VIO ..... -6V to 2.4V

Digital Inputs to GND ..... -0.3V to V_{IO} + 0.3V

Digital Outputs to GND ..... -0.3V to V_{IO} + 0.3V

Package Thermal Resistance

MSOP-10, θ_{JA} ..... 131.8℃/W

MSOP-10, θ_{JB} ..... 77℃/W

MSOP-10, θ_{JC} ..... 43.4℃/W

TDFN-3×3-10L, θ_{JA} ..... 40.5℃/W

TDFN-3×3-10L, θ_{JB} ..... 14.8℃/W

TDFN-3×3-10L, $\theta_{JC\ (TOP)}$ ..... 41.7℃/W

TDFN-3×3-10L, $\theta_{JC\ (BOT)}$ ..... 3.2℃/W

Junction Temperature .....+150℃

Storage Temperature Range .....-65℃ to +150℃

Lead Temperature (Soldering, 10s) .....+260℃

ESD Susceptibility (3) (4)

HBM.....±4000V

CDM .....±1250V

NOTES:

1. For an explanation of IN+ and IN-, refer to Analog Inputs section.

2. Test the current condition over a 10ms time interval.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

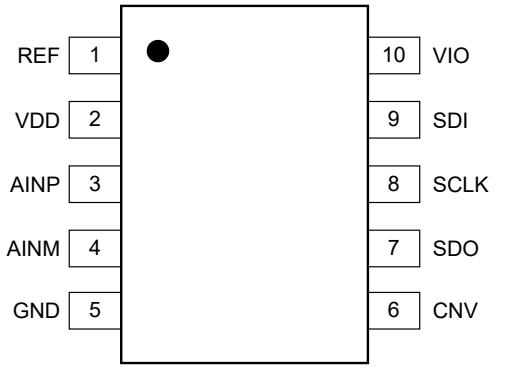
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

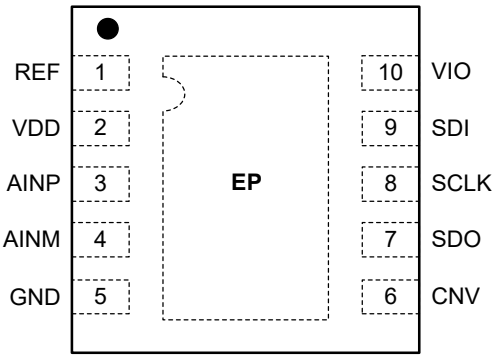
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-10

(TOP VIEW)



TDFN-3×3-10L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
MSOP-10	TDFN-3×3-10L			
1	1	REF	AI	Reference Voltage Input Pin.
2	2	VDD	P	Power Supply Pin. The VDD range is 1.71V to 1.89V. A 1.8V power is recommended.
3	3	AINP	AI	Differential Positive Analog Input.
4	4	AINM	AI	Differential Negative Analog Input.
5	5	GND	P	Ground.
6	6	CNV	DI	It is a multi-function pin. In each communication frame, at the first rising edge if SDI is high, this pin selects nCS mode. At the first rising edge if SDI is low, this pin selects daisy-chain mode.
7	7	SDO	DO	Serial Data Output.
8	8	SCLK	DI	Serial Data Clock Input.
9	9	SDI	DI	Serial Data Input Pin. It has two modes, daisy-chain mode and nCS mode. Daisy-chain mode: SDI is used as a data input to daisy-chain. The digital data on SDI is output on SDO with a delay of 16 SCLKs. nCS mode: the serial interface can be enabled by either SDI or CNV pin. After a conversion is completed, the busy indicator feature is enabled.
10	10	VIO	P	Digital Input/Output Interface Power Supply Pin.
—	Exposed Pad	EP	P	Exposed Pad. It should be connected to GND.

NOTE: AI = analog input, DI = digital input, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.71V to 1.89V, V_{IO} = 1.71V to 5.5V, V_{REF} = 5V, T_A = -40℃ to +125℃, turbo mode enabled, and f_{SAMPLE} = 2MSPS, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution				16			Bits
Analog Input							
Voltage Range		AINP - AINM		$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage		AINP, AINM to GND		-0.1		V_{REF} + 0.1	V
Common Mode Input Range				$V_{REF}/2$ - 0.125	$V_{REF}/2$	$V_{REF}/2$ + 0.125	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 500kHz	MSOP-10		88		dB
			TDFN-3×3-10L		79		
Analog Input Current		Acquisition phase, T_A = +25℃			0.3		nA
Throughput							
Complete Cycle				500			ns
Conversion Time		Excluded the turbo mode			458		ns
Acquisition Phase (1)					230		ns
Throughput Rate (2)				0		2	MSPS
Transient Response (3)					250		ns
DC Accuracy							
No Missing Codes				16			Bits
Integral Nonlinearity (4)	INL	MSOP-10		-2.5		2.5	LSB
				-38.1		38.1	ppm
		TDFN-3×3-10L		-2		2	LSB
				-30.5		30.5	ppm
Differential Nonlinearity (4)	DNL	MSOP-10		-0.999		1.5	LSB
		TDFN-3×3-10L		-0.999		1	
Transition Noise					0.38		LSB
Zero Error					0.5	10	LSB
Zero Error Drift (4)				-1.5		1.5	ppm/℃
Gain Error	E_G				1		LSB
Gain Error Drift (4)				-1.6		1.6	ppm/℃
Power Supply Sensitivity	PSRR	V_{DD} = 1.8V ± 5%			1		LSB
1/f Noise		Bandwidth = 0.1Hz to 10Hz	MSOP-10		2		μV_{P-P}
			TDFN-3×3-10L		2.1		
AC Accuracy							
Dynamic Range		MSOP-10			96.5		dBFS
		TDFN-3×3-10L			96.7		
Total RMS Noise					58		μVrms
Signal-to-Noise Ratio (4)	SNR	f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10	93.5	96		dBFS
			TDFN-3×3-10L	93.5	96		
		f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 4.096V	MSOP-10	92.5	95.1		
			TDFN-3×3-10L	92.5	95.7		
		f_{IN} = 100kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10		93.4		
			TDFN-3×3-10L		93.8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.71V to 1.89V, V_{IO} = 1.71V to 5.5V, V_{REF} = 5V, T_A = -40℃ to +125℃, turbo mode enabled, and f_{SAMPLE} = 2MSPS, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC Accuracy							
Spurious-Free Dynamic Range (4)	SFDR	f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10	93.2	111.1		dBFS
			TDFN-3×3-10L	102	119.3		
		f_{IN} = 1kHz, -0.5dBFS, VREF = 4.096V	MSOP-10	93.5	112.7		
			TDFN-3×3-10L	102	122.6		
		f_{IN} = 100kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10		106.4		
			TDFN-3×3-10L		107.7		
Signal-to-Noise-and-Distortion Ratio (4)	SINAD	f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10	91.2	95.8		dBFS
			TDFN-3×3-10L	93	96		
		f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 4.096V	MSOP-10	91	95.1		
			TDFN-3×3-10L	92	95.6		
		f_{IN} = 100kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10		93.1		
			TDFN-3×3-10L		93.6		
Total Harmonic Distortion (4)	THD	f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10		-109.4	-92.8	dBFS
			TDFN-3×3-10L		-117.3	-100	
		f_{IN} = 1kHz, -0.5dBFS, V_{REF} = 4.096V	MSOP-10		-110	-92.5	
			TDFN-3×3-10L		-119.6	-100	
		f_{IN} = 100kHz, -0.5dBFS, V_{REF} = 5V	MSOP-10		-105.3		
			TDFN-3×3-10L		-107.3		
-3dB Input Bandwidth		MSOP-10			60		MHz
		TDFN-3×3-10L			55		
Aperture Delay					2		ns
Aperture Jitter					1		ps rms
Reference							
Voltage Range	V_{REF}			4.096		5.1	V
Current		V_{REF} = 5V, 2MSPS			0.96		mA
Input Over-Voltage Clamp							
AINP/AINM Current	I_{AINP}/I_{AINM}	V_{REF} = 5V				55	mA
		V_{REF} = 2.5V				55	
V_{AINP}/V_{AINM} at Maximum I_{AINP}/I_{AINM}		V_{REF} = 5V			5.5		V
		V_{REF} = 2.5V			3		
V_{AINP}/V_{AINM} Clamp On/Off Threshold		V_{REF} = 5V		5.15	5.32		V
		V_{REF} = 2.5V		2.69	2.83		
Deactivation Time					500		ns
REF Current at Maximum I_{AINP}/I_{AINM}		$V_{IN+}/V_{IN-} > V_{REF}$			42		μA
Digital Inputs							
Input Low Voltage	V_{IL}	V_{IO} > 2.7V		-0.3		+0.3 × V_{IO}	V
		V_{IO} ≤ 2.7V		-0.3		+0.2 × V_{IO}	
Input High Voltage	V_{IH}	V_{IO} > 2.7V		0.7 × V_{IO}		V_{IO} + 0.3	V
		V_{IO} ≤ 2.7V		0.8 × V_{IO}		V_{IO} + 0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.71V to 1.89V, V_{IO} = 1.71V to 5.5V, V_{REF} = 5V, T_A = -40℃ to +125℃, turbo mode enabled, and f_{SAMPLE} = 2MSPS, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs							
Input Low Current	I_{IL}	Input Voltage = 0V		-1		1	μA
Input High Current	I_{IH}	Input Voltage = V_{IO}		-1		1	μA
Input Pin Capacitance		MSOP-10			2		pF
		TDFN-3×3-10L			6		
Digital Outputs							
Data Format				Serial 16 bits, two's complement			
Pipeline Delay				Conversion results available immediately after the conversion completed			
Output Low Voltage	V_{OL}	I_{SINK} = 500μA				0.05	V
Output High Voltage	V_{OH}	I_{SOURCE} = 500μA		V_{IO} - 0.05			V
Power Supplies							
V_{DD}				1.71	1.8	1.89	V
V_{IO}				1.71		5.5	V
Standby Current		V_{DD} = 1.8V, V_{IO} = 1.8V	T_A = +25℃		2.4	18	μA
			T_A = +85℃			30	
			T_A = +125℃			75	
Power Dissipation		V_{DD} = 1.8V, V_{IO} = 1.8V, V_{REF} = 5V	10kSPS		156	400	μW
			500kSPS		7	10.5	mW
			1MSPS		13.9	20.4	
			2MSPS		27.4	40.2	
VDD Only		V_{DD} = 1.8V, V_{IO} = 1.8V, V_{REF} = 5V	500kSPS		5.6		mW
			1MSPS		11.2		
			2MSPS		22		
REF Only		V_{DD} = 1.8V, V_{IO} = 1.8V, V_{REF} = 5V	500kSPS		1.2		mW
			1MSPS		2.4		
			2MSPS		4.8		
VIO Only		V_{DD} = 1.8V, V_{IO} = 1.8V, V_{REF} = 5V	500kSPS		0.17		mW
			1MSPS		0.32		
			2MSPS		0.63		
Energy per Conversion					13.7		nJ/ sample
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		+125	℃

NOTES:

1. The acquisition phase is the time required for the input sampling capacitor to obtain a new input that has the ADC running at a 2MSPS throughput rate.

2. The 2MSPS throughput rate can be achieved only when the turbo mode is enabled and the minimum SCLK rate is 100MHz, V_{IO} ≥ 2.7V.

3. The transient response is the time required for the ADC to obtain a full-scale input step to ±1LSB accuracy.

4. Guaranteed by characterization.

TIMING CHARACTERISTICS

(V_{DD} = 1.71V to 1.89V, V_{IO} = 1.71V to 5.5V, V_{REF} = 5V, turbo mode enabled, and f_{SAMPLE} = 2MSPS, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Interface Timing						
Conversion Time, CNV Rising Edge to Data Available	t_{CONV}	Excluded the turbo mode		458		ns
Acquisition Phase (1)	t_{ACQ}			230		ns
Time between Conversions	t_C		500			ns
CNV Pulse Width (nCS Mode) (2)	t_1		10			ns
SCLK Period (nCS Mode) (3)	t_3	V_{IO} > 2.7V	10			ns
		V_{IO} > 1.7V	10			
SCLK Period (Daisy-Chain Mode) (4)		V_{IO} > 2.7V	21			ns
		V_{IO} > 1.7V	26			
SCLK Low Time	t_5		3			ns
SCLK High Time	t_4		3			ns
SCLK Falling Edge to Data Remains Valid Delay	t_9	V_{IO} > 2.7V	1.5			ns
		V_{IO} > 1.7V	1.5			
SCLK Falling Edge to Data Valid Delay	t_{10}	V_{IO} > 2.7V			11	ns
		V_{IO} > 1.7V			14.5	
CNV or SDI Low to SDO D15 Most Significant Bit (MSB) Valid Delay (nCS Mode)	t_8	V_{IO} > 2.7V			10	ns
		V_{IO} > 1.7V			13	
CNV Pulse Width (Turbo Mode)	t_{QUIET1}		260			ns
Last SCLK Falling Edge to CNV Rising Edge Delay	t_{QUIET2}		50			ns
CNV or SDI High or Last SCLK Falling Edge to SDO High Impedance (nCS Mode)	t_{11}				20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$		3			ns
SDI Valid Hold Time from CNV Rising Edge (nCS Mode)	$t_{HSDICNV}$		3			ns
SCLK Valid Hold Time from CNV Rising Edge (Daisy-Chain Mode)	$t_{HSCLKCNV}$		12			ns
SDI Valid Setup Time from SCLK Rising Edge (Daisy-Chain Mode)	t_6		3			ns
SDI Valid Hold Time from SCLK Rising Edge (Daisy-Chain Mode)	t_7		3			ns

NOTES:

1. The acquisition phase is the time required for the input sampling capacitors to obtain a new input that has the ADC running at a 2MSPS throughput rate.

2. For the turbo mode, t_1 must correspond to the minimum value of t_{QUIET1}.

3. The 2MSPS throughput rate can be achieved only when turbo mode is enabled and the minimum SCLK rate is 100MHz, $V_{IO} \geq$ 2.7V.

4. It is assumed that the SCLK has a 50% duty cycle.

TIMING CHARACTERISTICS (continued)

(V_{DD} = 1.71V to 1.89V, V_{IO} = 1.71V to 5.5V, V_{REF} = 5V, turbo mode enabled, and f_{SAMPLE} = 2MSPS, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Register Read/Write Timing						
Read/Write Operation						
CNV Pulse Width (2)	t_1		10			ns
SCLK Period	t_3	V_{IO} > 2.7V	10			ns
		V_{IO} > 1.7V	10			
SCLK Low Time	t_5		3			ns
SCLK High Time	t_4		3			ns
Read Operation						
CNV Low to SDO D15 MSB Valid Delay	t_8	V_{IO} > 2.7V			10	ns
		V_{IO} > 1.7V			13	
SCLK Falling Edge to Data Remains Valid Delay	t_9	V_{IO} > 2.7V	1.5			ns
		V_{IO} > 1.7V	1.5			
SCLK Falling Edge to Data Valid Delay	t_{10}	V_{IO} > 2.7V			11	ns
		V_{IO} > 1.7V			14.5	
CNV Rising Edge to SDO High Impedance	t_{11}				20	ns
Write Operation						
SDI Valid Setup Time from SCLK Rising Edge	t_6		3			ns
SDI Valid Hold Time from SCLK Rising Edge	t_7		3			ns
CNV Rising Edge to SCLK Edge Hold Time	t_{13}		0			ns
CNV Falling Edge to SCLK Active Edge Setup Time	t_2		6			ns

TIMING DIAGRAMS

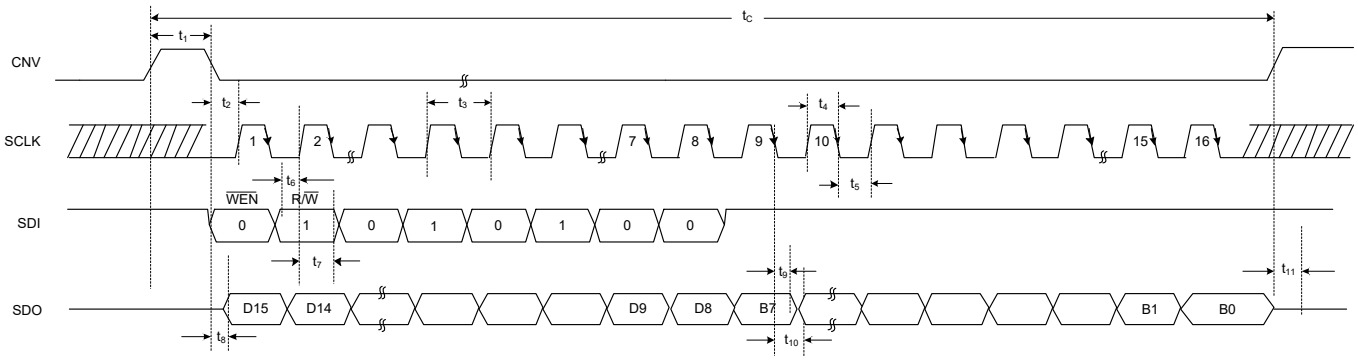
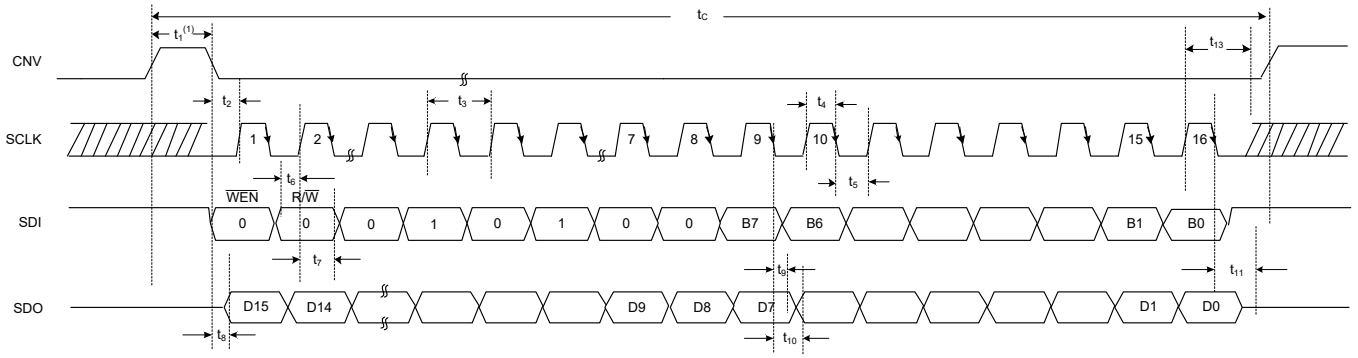


Figure 1. Register Read Timing Diagram



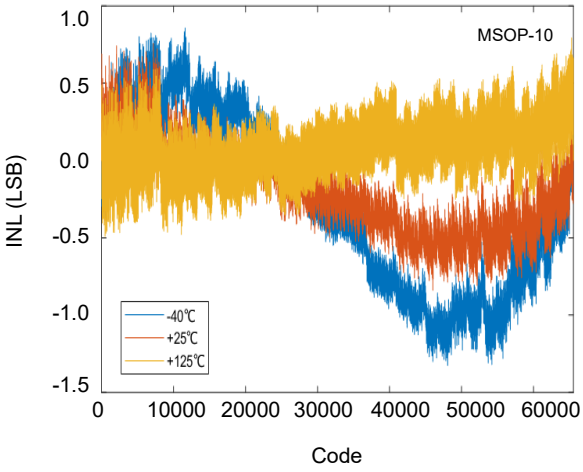
NOTE 1: Must wait for enough conversion time t_1 and then read back the conversion result and issue a register write at the same time.

Figure 2. Register Write Timing Diagram

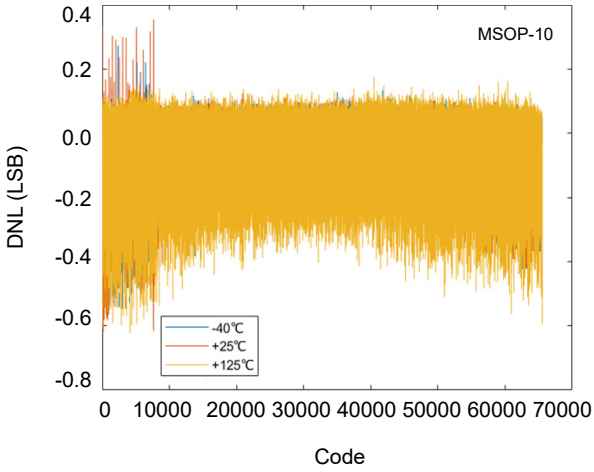
TYPICAL PERFORMANCE CHARACTERISTICS

For MSOP-10 package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

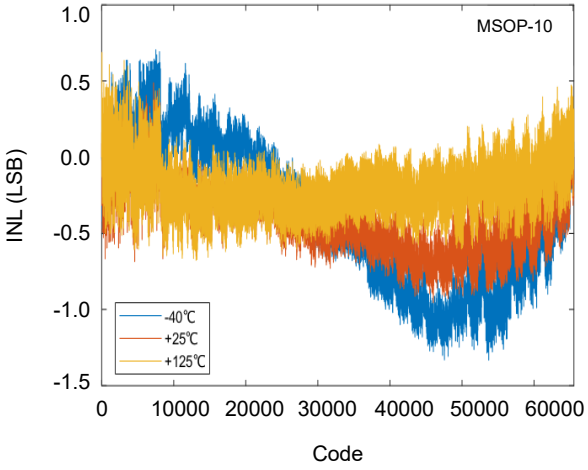
INL vs. Code for Various Temperatures (V_{REF} = 5V)



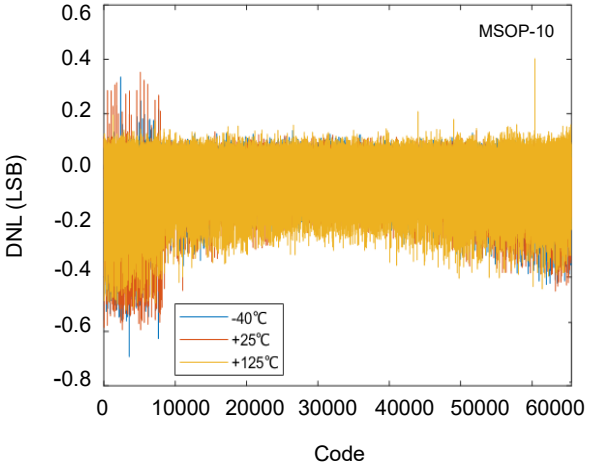
DNL vs. Code for Various Temperatures (V_{REF} = 5V)



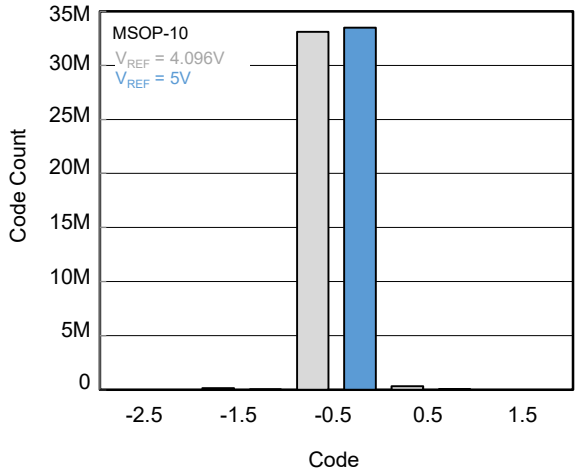
INL vs. Code for Various Temperatures (V_{REF} = 4.096V)



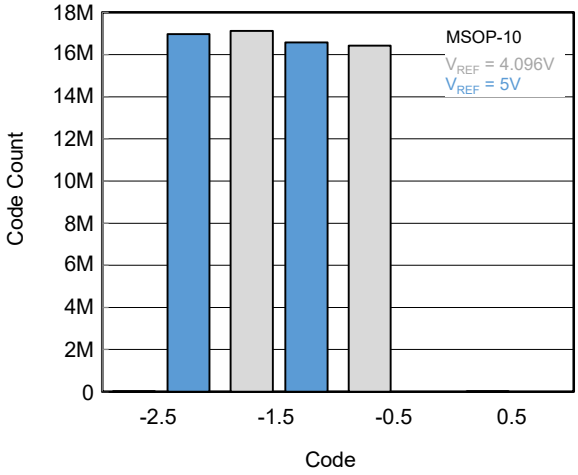
DNL vs. Code for Various Temperatures (V_{REF} = 4.096V)



Histogram of a DC Input at Code Center



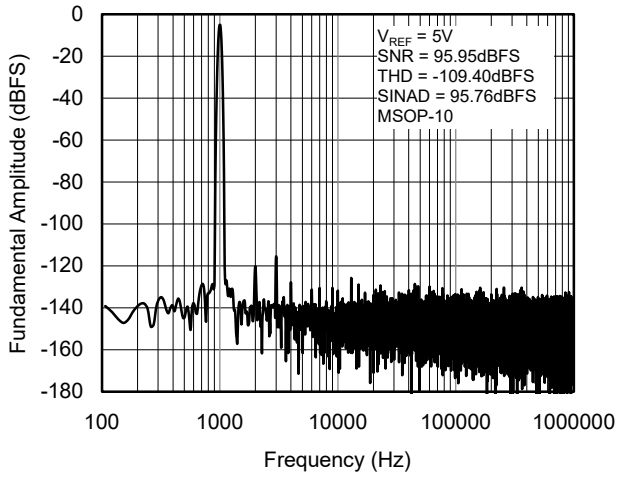
Histogram of a DC Input at Code Transition



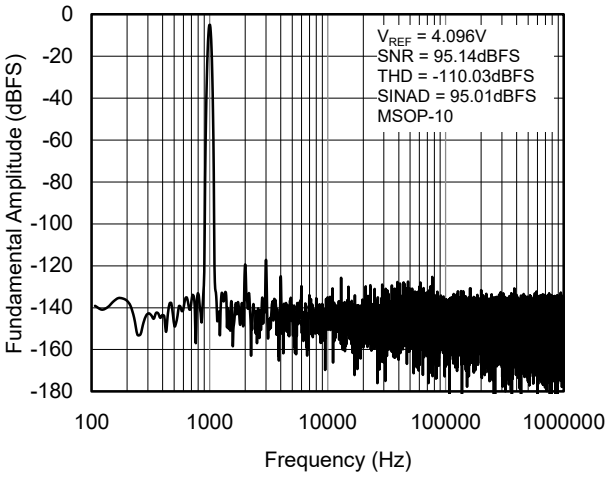
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For MSOP-10 package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

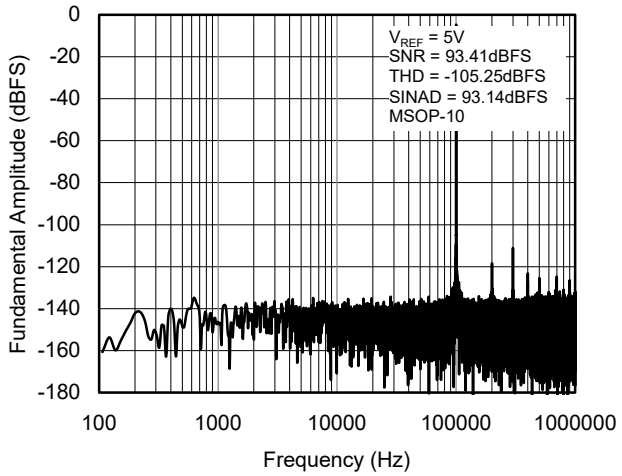
1kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



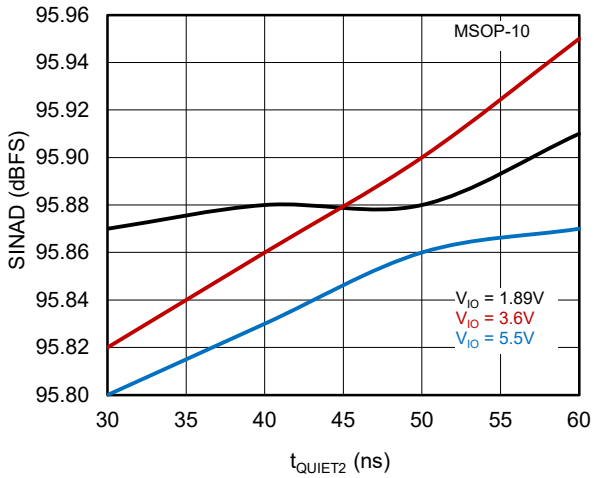
1kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



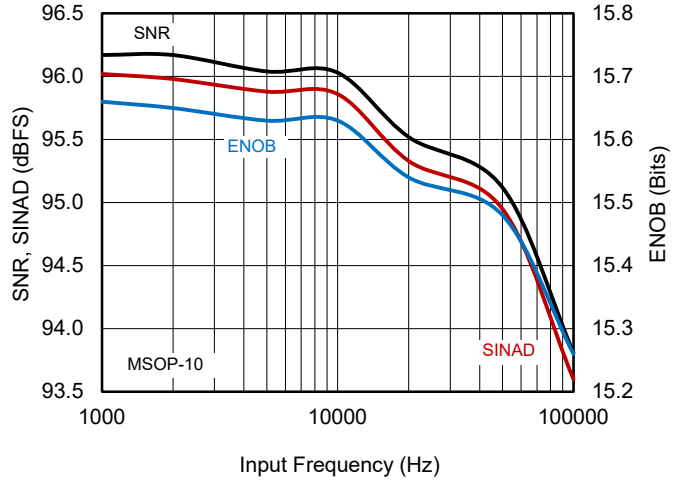
100kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



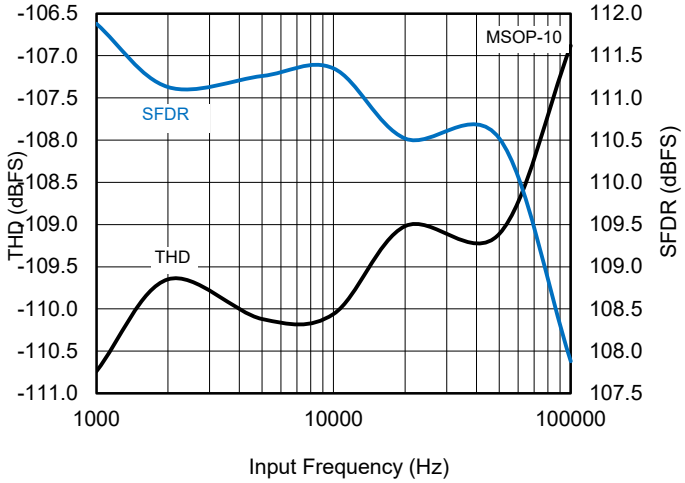
SINAD vs. t_{QUIET2}



SNR, SINAD, and Effective Number of Bits (ENOB) vs. Input Frequency



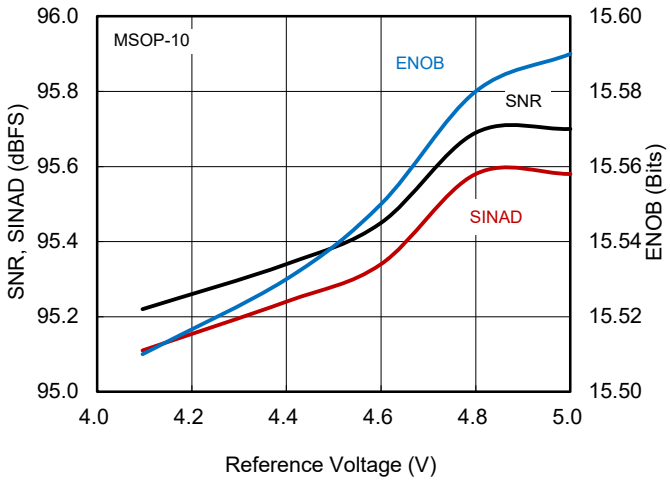
THD and SFDR vs. Input Frequency



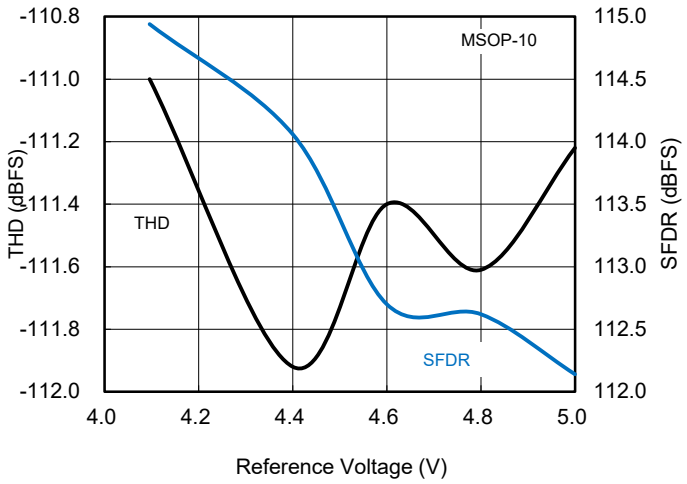
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For MSOP-10 package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

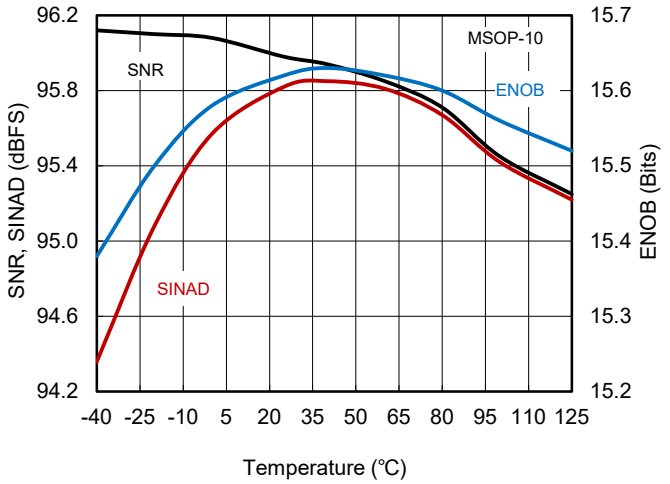
SNR, SINAD, and ENOB vs. Reference Voltage, f_{IN} = 1kHz



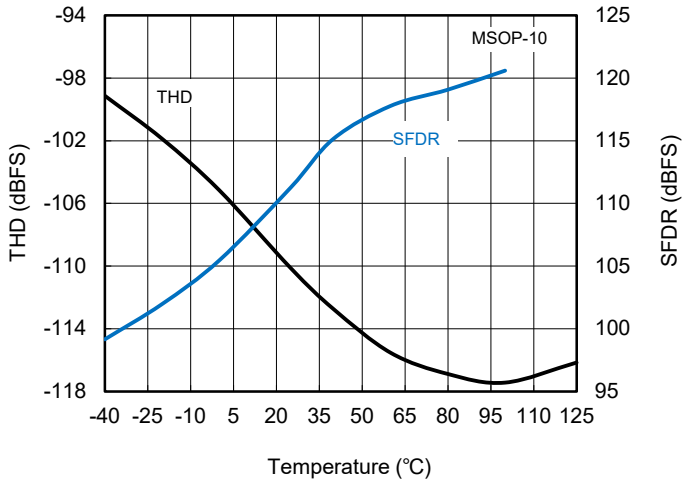
THD and SFDR vs. Reference Voltage, f_{IN} = 1kHz



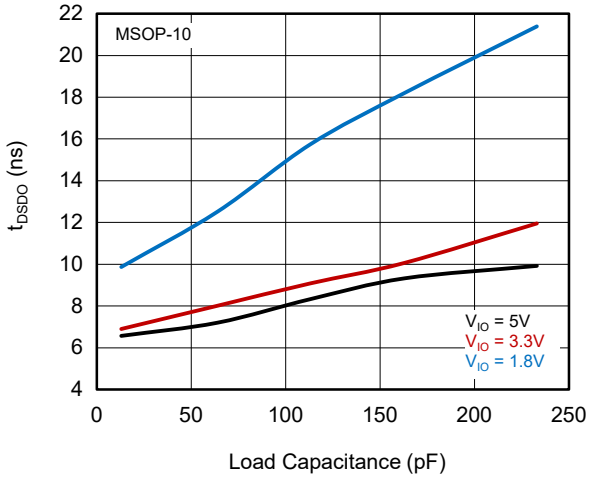
SNR, SINAD, and ENOB vs. Temperature, f_{IN} = 1kHz



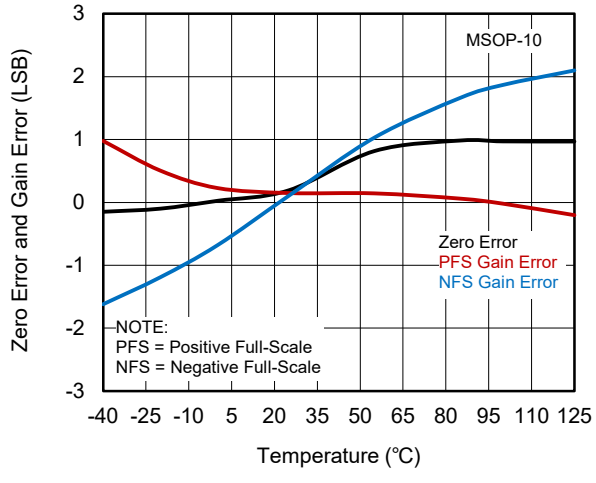
THD and SFDR vs. Temperature, f_{IN} = 1kHz



t_{DSDO} vs. Load Capacitance



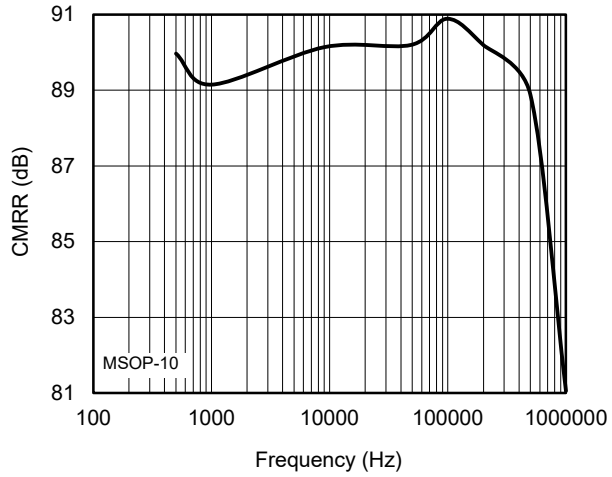
Zero Error and Gain Error (PFS and NFS) vs. Temperature



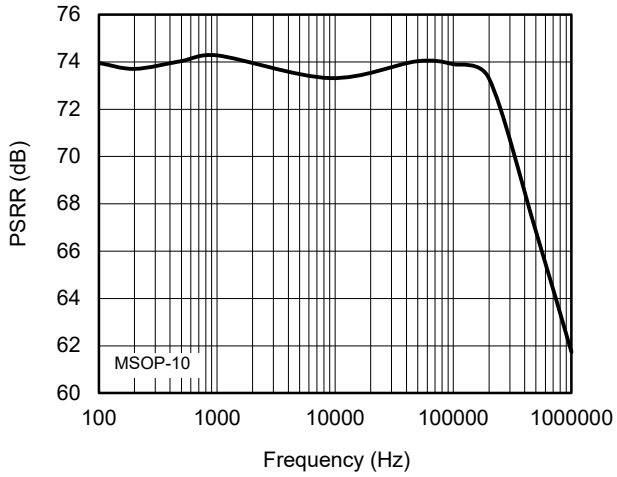
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For MSOP-10 package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

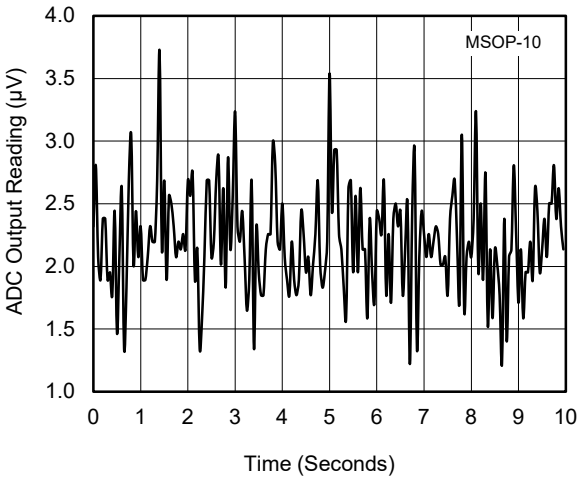
CMRR vs. Frequency



PSRR vs. Frequency



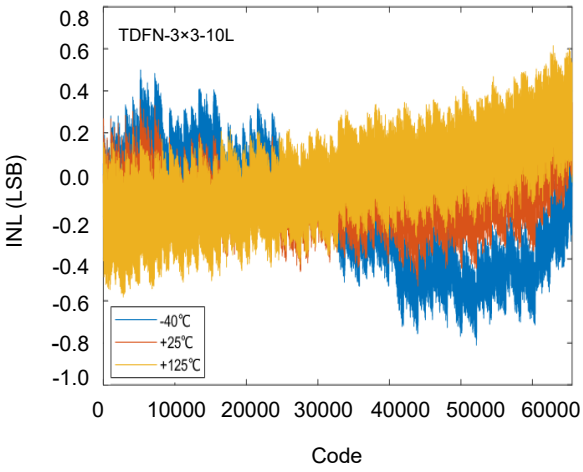
1/f Noise for 0.1Hz to 10Hz Bandwidth,
50kSPS, 2500 Samples Averaged per Reading



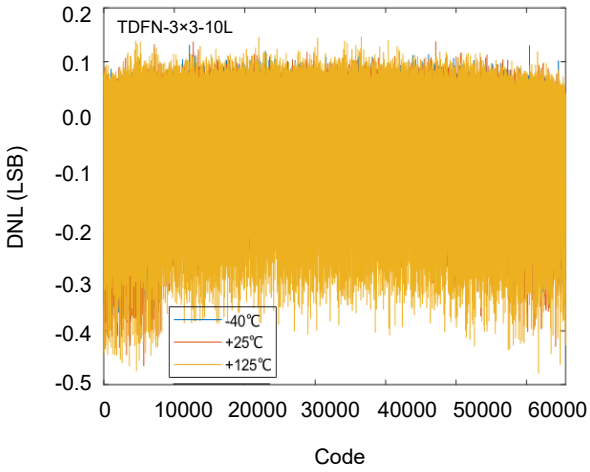
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For TDFN-3×3-10L package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

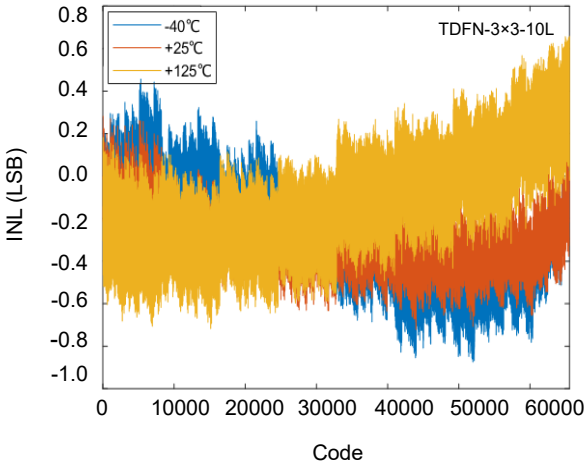
INL vs. Code for Various Temperatures (V_{REF} = 5V)



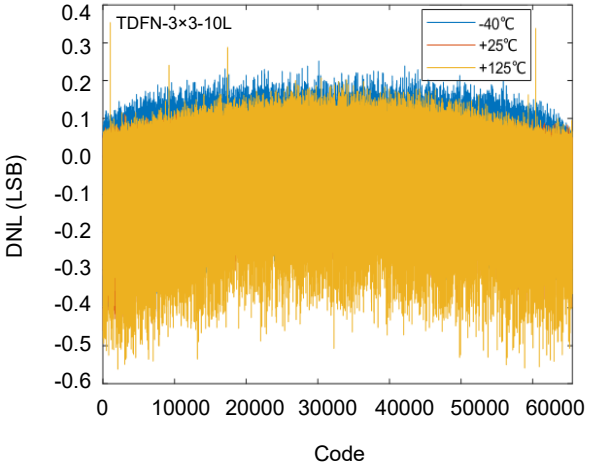
DNL vs. Code for Various Temperatures (V_{REF} = 5V)



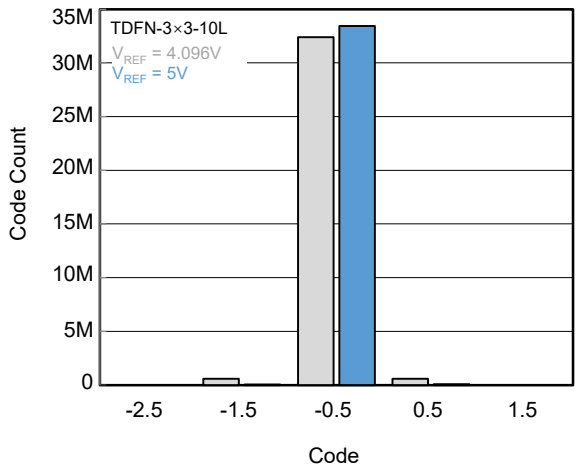
INL vs. Code for Various Temperatures (V_{REF} = 4.096V)



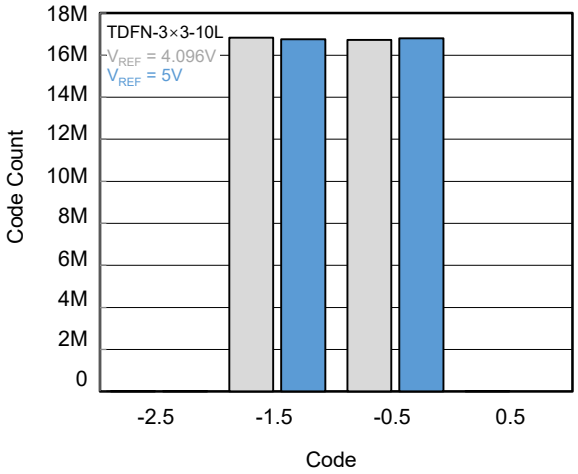
DNL vs. Code for Various Temperatures (V_{REF} = 4.096V)



Histogram of a DC Input at Code Center



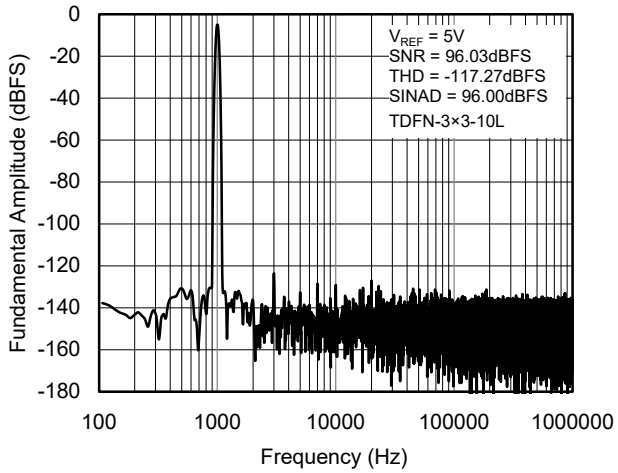
Histogram of a DC Input at Code Transition



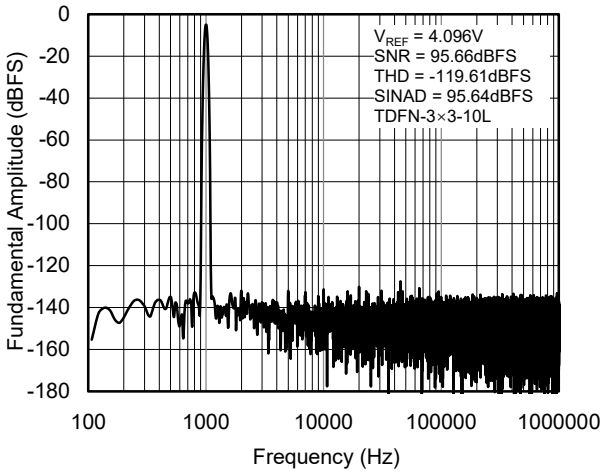
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For TDFN-3×3-10L package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

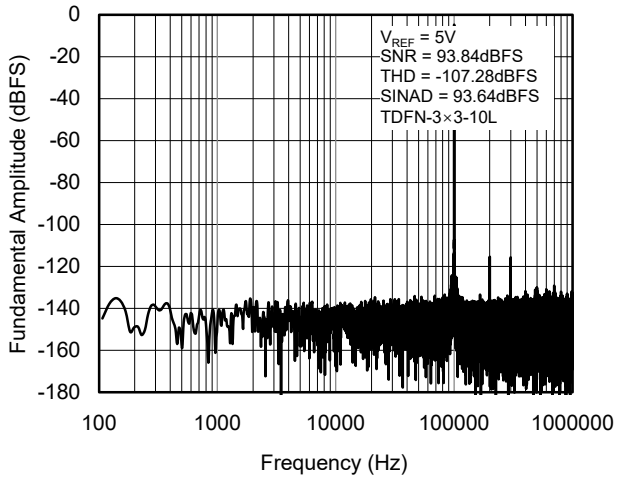
1kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



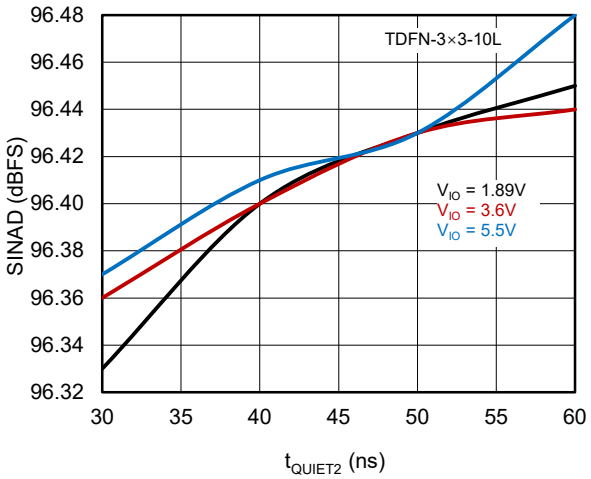
1kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



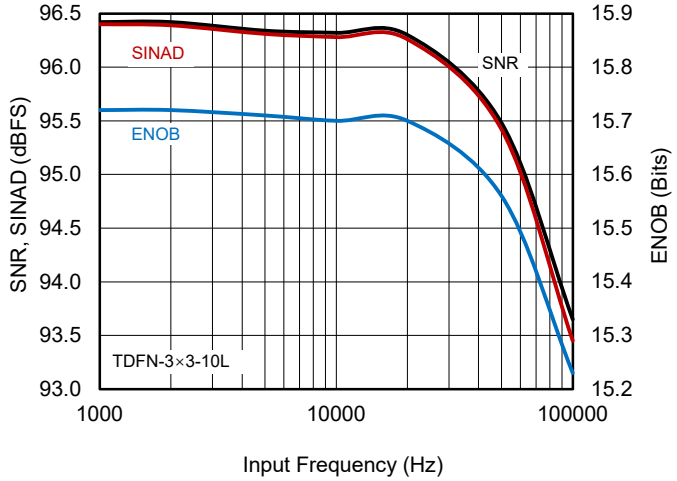
100kHz, -0.5dBFS Input Tone Fast Fourier Transform (FFT)



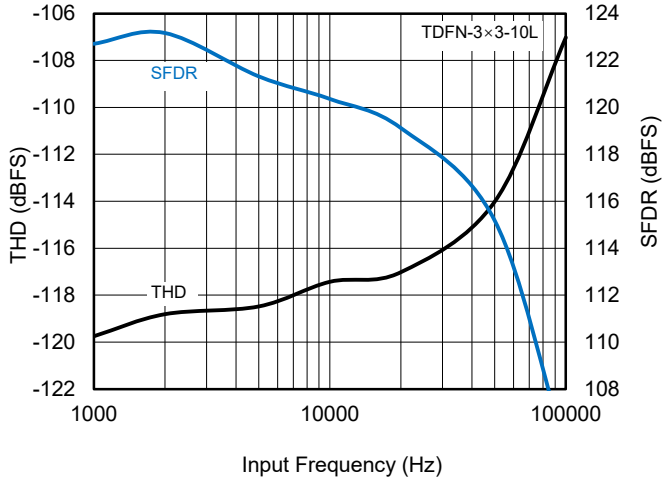
SINAD vs. t_{QUIET2}



SNR, SINAD, and Effective Number of Bits (ENOB) vs. Input Frequency



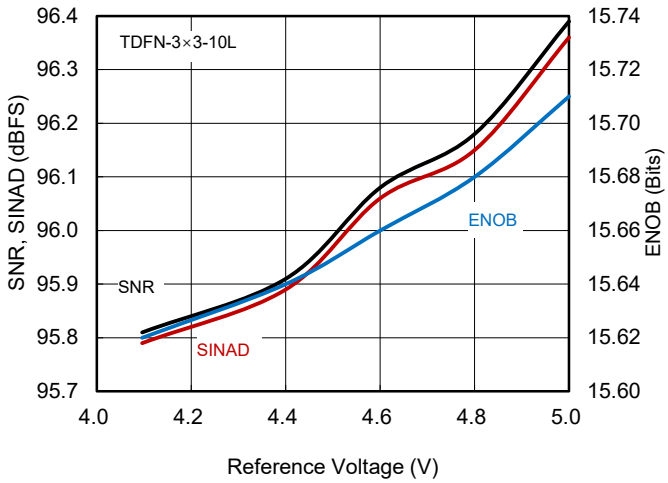
THD and SFDR vs. Input Frequency



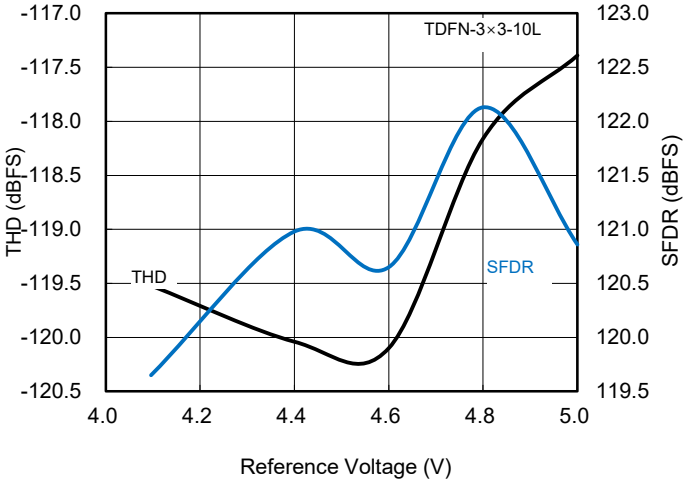
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For TDFN-3×3-10L package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

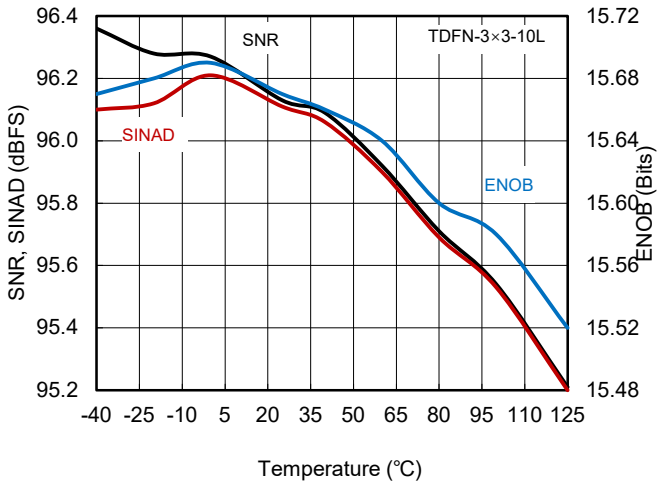
SNR, SINAD, and ENOB vs. Reference Voltage, f_{IN} = 1kHz



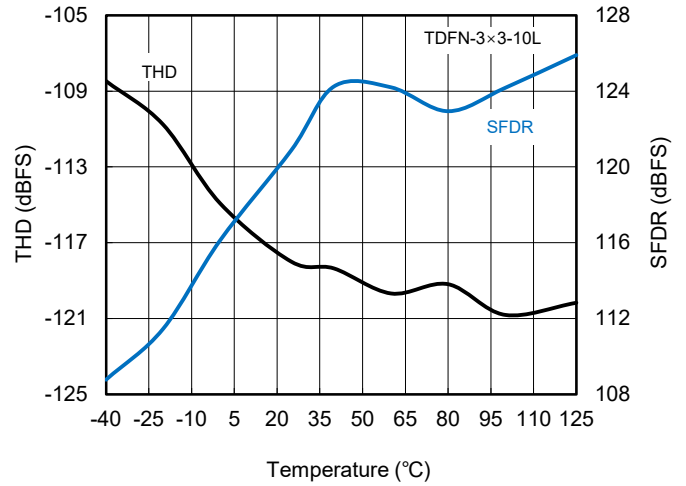
THD and SFDR vs. Reference Voltage, f_{IN} = 1kHz



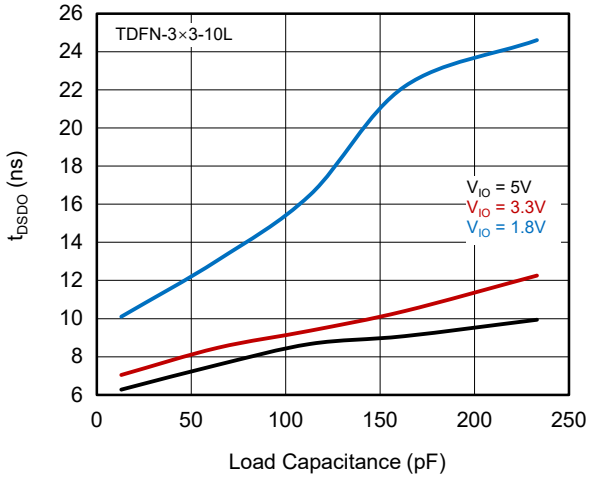
SNR, SINAD, and ENOB vs. Temperature, f_{IN} = 1kHz



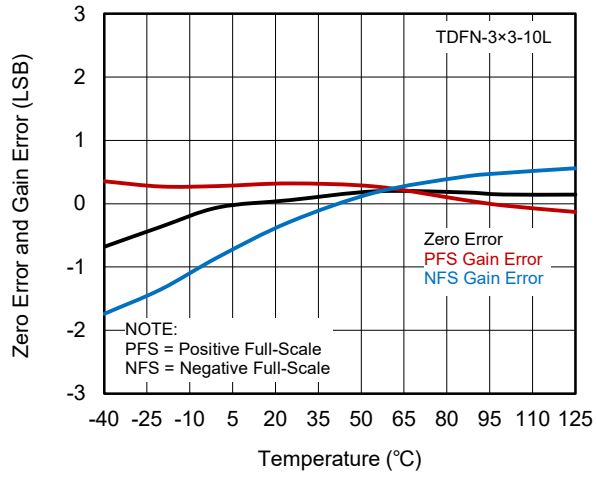
THD and SFDR vs. Temperature, f_{IN} = 1kHz



t_{DSDO} vs. Load Capacitance



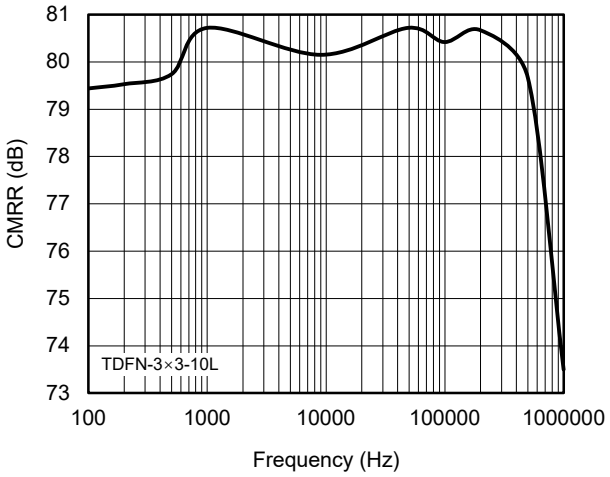
Zero Error and Gain Error (PFS and NFS) vs. Temperature



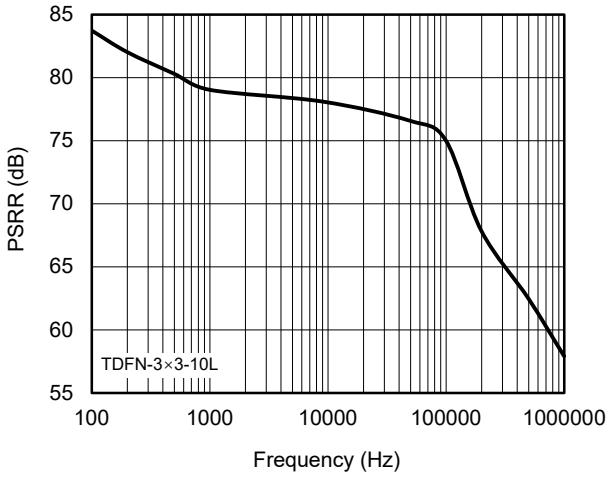
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For TDFN-3×3-10L package, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

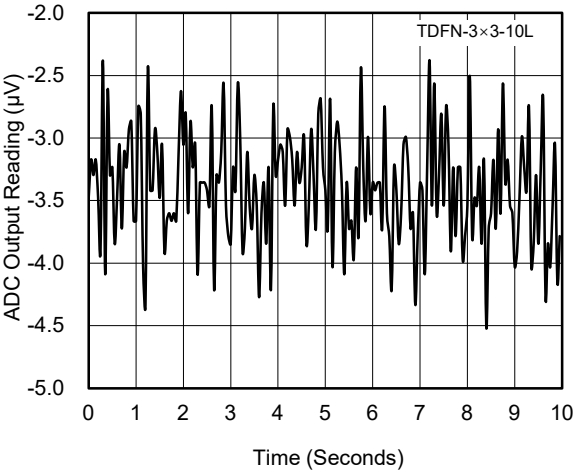
CMRR vs. Frequency



PSRR vs. Frequency



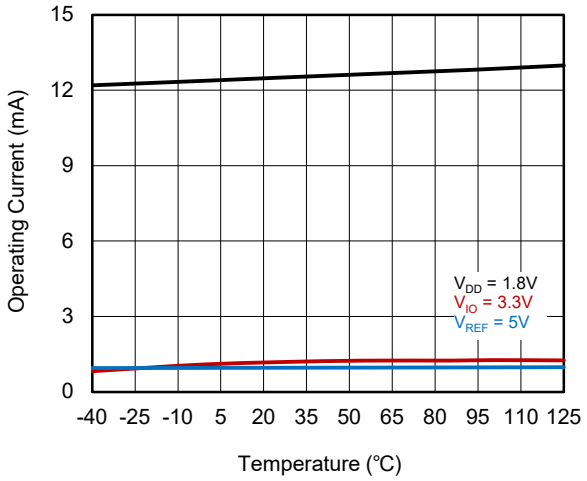
1/f Noise for 0.1Hz to 10Hz Bandwidth, 50kSPS, 2500 Samples Averaged per Reading



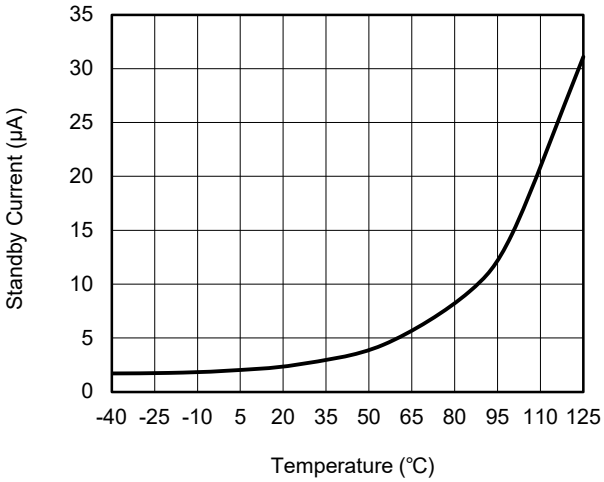
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Both MSOP-10 and TDFN-3×3-10L packages, V_{DD} = 1.8V, V_{IO} = 3.3V, V_{REF} = 5V, T_A = +25℃, turbo mode enabled, and f_S = 2MSPS, unless otherwise noted.

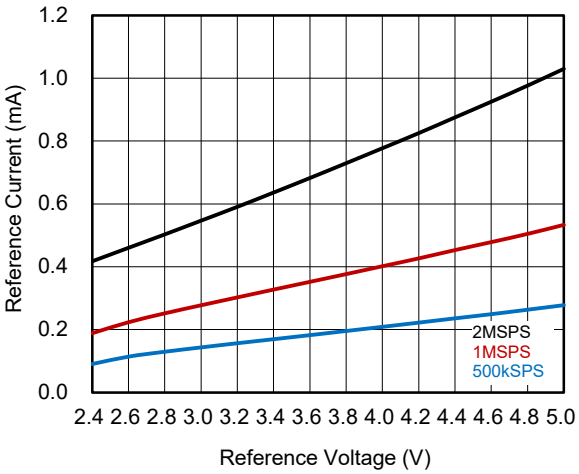
Operating Current vs. Temperature



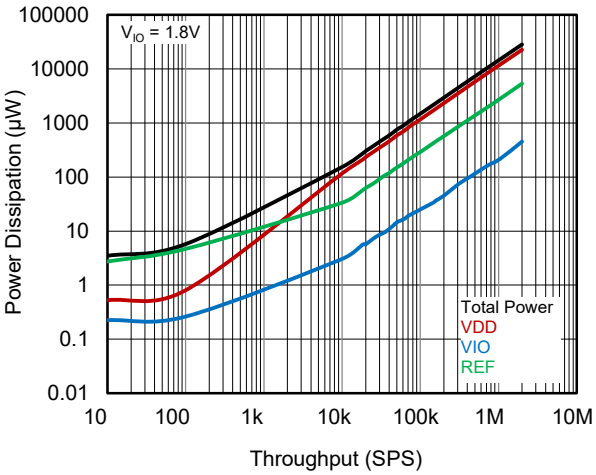
Standby Current vs. Temperature



Reference Current vs. Reference Voltage



Power Dissipation vs. Throughput



FUNCTIONAL BLOCK DIAGRAM

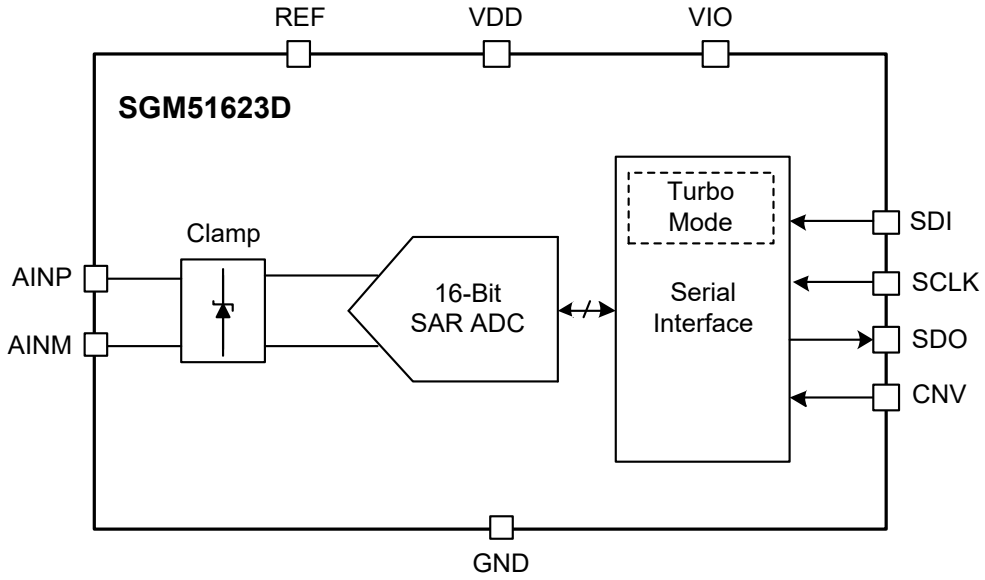


Figure 3. Block Diagram

DETAILED DESCRIPTION

Circuit Information

The SGM51623D is a 1-channel 16-bit successive approximation ADC, which is based on the switched capacitor array architecture.

The SGM51623D works with 1.8V power supply for VDD, and the interface power supply range is 1.8V to 5V for VIO power supply.

The SGM51623D requires a quick setting time and low noise driving amplifier, as there is a charging and kickback current seen from the ADC inputs when ADC is working.

The maximum conversion rate of 2MSPS for the SGM51623D is only achieved by turbo mode enabled and a minimum SCLK rate of 100MHz, V_{IO} ≥ 2.7V.

Converter Operation

The SGM51623D has an on-chip internal oscillator which is used to the clock source of internal conversion. The SCLK is not required for the conversion process.

A complete conversion process contains two phases: the acquisition phase and the conversion phase.

In the acquisition phase, the internal capacitor arrays are connected to the IN+ and IN- inputs and acquire the input signals.

In the conversion phase, the internal capacitor arrays are disconnected from the input pins. The internal control logic stator machine controls the conversion process. Once this process is completed, the control logic generates the ADC output code and a busy signal indicator.

Transfer Functions

The ideal transfer characteristics for the SGM51623D are shown in Figure 4 and Table 1.

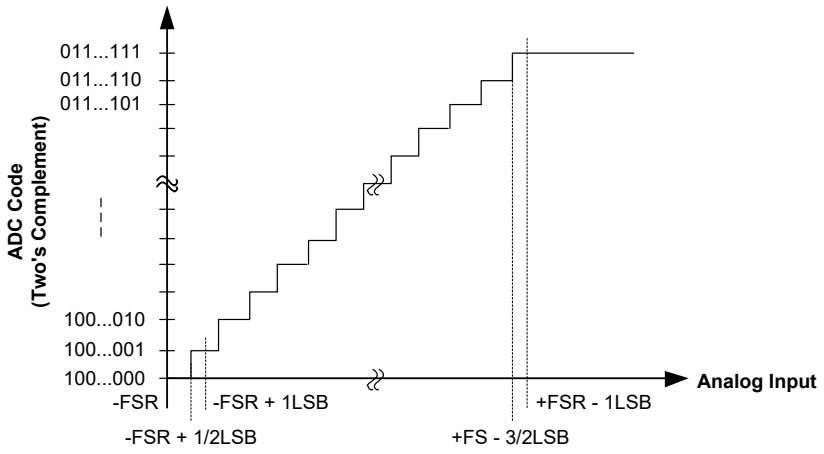
Table 1. Output Codes and Ideal Input Voltages

Description	Analog Input, V_{REF} = 5V	Digital Output Code (Hex)
FSR - 1LSB	+4.999847V	0x7FFF (1)
Mid-Scale + 1LSB	+152.6μV	0x0001
Mid-Scale	0V	0x0000
Mid-Scale - 1LSB	-152.6μV	0xFFFF
-FSR + 1LSB	-4.999847V	0x8001
-FSR	-5V	0x8000 (2)

NOTES:

1. The output code is also the code for an over-ranged analog input (V_{IN+} - V_{IN-} above V_{REF}).

2. The output code is also the code for an under-ranged analog input (V_{IN+} - V_{IN-} below -V_{REF}).



NOTE: FSR = Full-Scale Range.

Figure 4. Ideal Transfer Characteristics

APPLICATION INFORMATION

Typical Application Diagrams

In Figure 5, it shows a typical bipolar power supply connection for the ADC application. In this application, as the driver amplifier is powered by bipolar power supply, it provides the best dynamic range for input signal and enough headroom for ADC can reference source chip.

In the connected diagram, all resistor and capacitor parameters are suggested values, for specific devices, please select the right chip according to the datasheet recommendation.

If the system supply power is a unipolar power supply, the power supply rail drop must be considered. As there are saturation drops from the ground rail and the positive power rail, the amplitude shrink of input signal and nonlinearity of the input signal in front of the driver amplifier must be counted in.

In Figure 6, it shows a typical connection when using a fully differential amplifier as a driver. In the connection, it will get the best system SNR and THD performance.

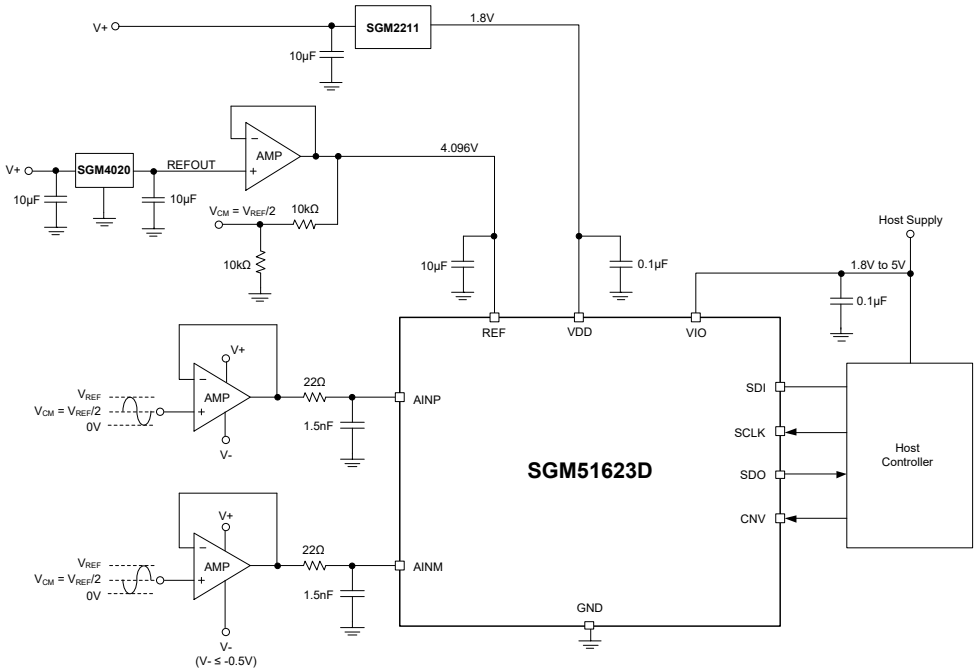


Figure 5. Typical Application Diagram with Multiple Supplies

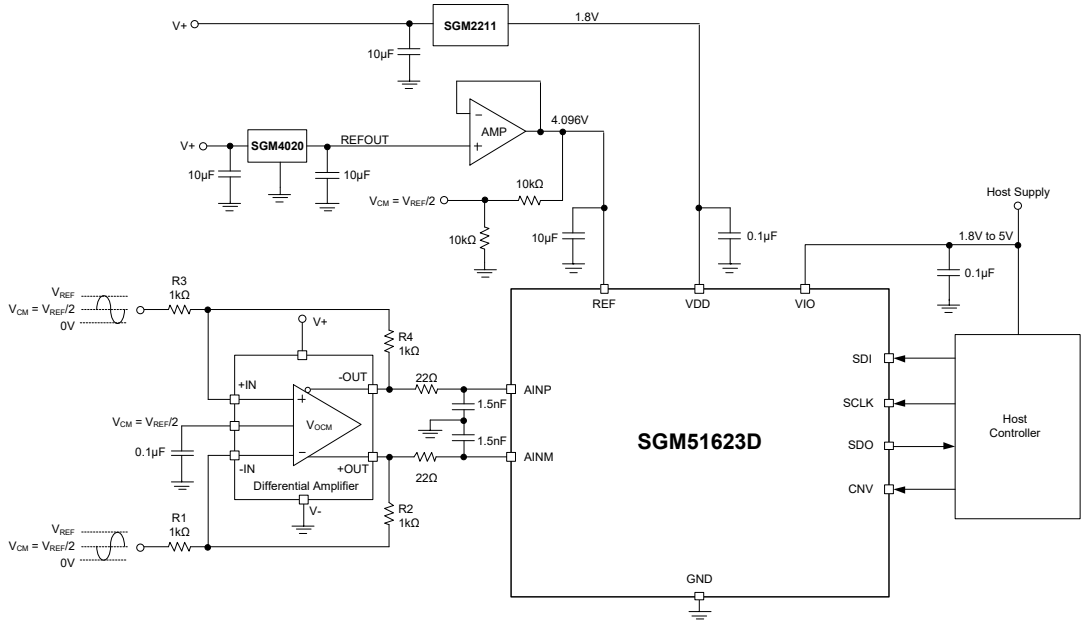


Figure 6. Recommended Connection Diagram When Using a Fully Differential Amplifier

APPLICATION INFORMATION (continued)

Analog Inputs

In Figure 7, it shows the equivalent input circuit of SGM51623D. If the input voltage exceeds the V_{REF} + 0.4V, the clamp diode turns on and the over-voltage flag (OV bit is logic low active) in the configuration register is set. The OV is cleared by a read operation. Only when the over-voltage condition is not present is the clearing of the OV bit by a read operation effective.

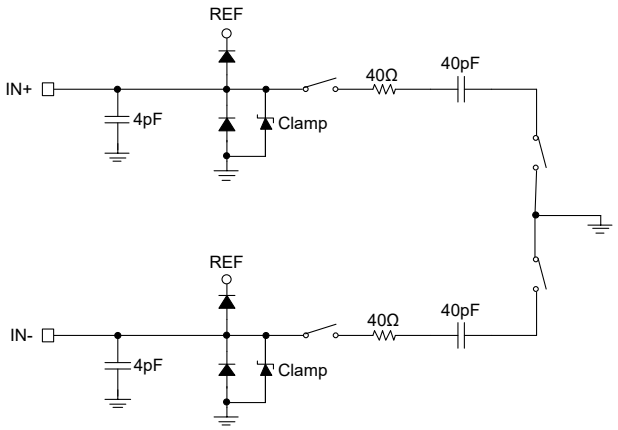


Figure 7. Equivalent Analog Input Circuit

Driving Amplifier

In the driving circuits shown in Figure 5 and Figure 6, it needs a true differential input to driver ADC, and keep the common mode voltage of the input signal within the specified range around V_{REF}/2.

The driver amplifier needs to meet the following requirements:

1. The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the SGM51623D.

2. For AC applications, the driver should have a THD performance commensurate with the SGM51623D.

3. For multi-channel multiplexed applications, the driver amplifier and the SGM51623D analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15.25ppm). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This can differ significantly from the settling time at a 16-bit level and it should be verified prior to driver selection.

Voltage Reference Input

A reference buffer amplifier is recommended between the reference source and ADC. And a suitable decoupling capacitor is needed at the reference output.

Power Supply

The SGM51623D has two power supply inputs. One is VDD pin, which is used to power for the analog and core digital. The other is VIO pin, which is used to power for the digital interface, its available range is from 1.8V to 5.5V.

The SGM51623D doesn't have power-up sequence requirement.

Digital Interface

The SGM51623D supports both 3-wire SPI mode and 4-wire SPI mode. In 3-wire mode, it is configured as CNV, SDO and SCLK. In 4-wire mode, it is configured as CNV, SDO, SCLK and SDI. And in 4-wire mode, CNV is used to initiate the conversion, which is independent of the reading timing (SDI).

In both 3-wire mode and 4-wire mode, a busy signal can be enabled to inform the host controller that the conversion result is ready. And the busy signal can also be used as an interrupt indication signal sent to the host controller.

The SGM51623D provides a daisy-chain feature that uses the SDI input for cascading multiple ADCs on a single data line, similar to a shift register.

The SGM51623D features the turbo mode. The turbo mode allows the use of slower SPI clock rates by extending the amount of time available to clock out conversion results. The maximum throughput of 2MSPS for the SGM51623D can only be achieved with turbo mode enabled and a minimum SCLK rate of 100MHz, V_{IO} ≥ 2.7V. Refer to nCS Mode, 3-Wire Turbo Mode and nCS Mode, 4-Wire Turbo Mode sections for descriptions of the turbo mode operation.

The status bits can be shifted out at the tail of the conversion results. It is enabled in the configuration register.

After the system power-up, the state of SDO depends on the states of CNV and SDI. Details are in Table 2.

Table 2. State of SDO on Power-Up

CNV	SDI	SDO
0	0	Low
0	1	Low
1	0	Low
1	1	High-Z

APPLICATION INFORMATION (continued)

Table 3. Configuration Register Details

Bits	Bit Name	Default	Type	Description
D[7:5]	Reserved	000	R	Reserved.
D[4]	Status Bits Enable	0	R/W	Status Bits Configure Bit 0 = Disable status bits (default) 1 = Enable status bits
D[3:2]	Reserved	00	R	Reserved.
D[1]	Turbo Mode Enable	0	R/W	Turbo Mode Configure Bit 0 = Disable turbo mode (default) 1 = Enable turbo mode
D[0]	nOV Clamp Flag	1	R	It is logic low effective bit. If it is low, it indicates an over-voltage events happened or is happening. It is cleared by read. The read operation can clear this flag only when the over-voltage event has disappeared. 0 = Indicate an over-voltage event has occurred 1 = Indicate no over-voltage event has occurred (default)

NOTE: R = read only and R/W = read/write. Read only bits cannot be updated with a register write operation. Read/write bits can be updated with a register write operation.

Table 4. SCLK Frequency Requirements for Various Throughputs

nCS Mode	Throughput (MSPS)	Minimum SCLK Frequency (MHz)
3-Wire and 4-Wire Turbo Modes	2	100
	1	30
	0.5	11
	0.1	2
3-Wire and 4-Wire Turbo Modes with Six Status Bits (1)	1.5	100
	1	35
	0.5	15
	0.1	2.5
3-Wire and 4-Wire Modes	1.5	100
	1	33
	0.5	12
	0.1	2
3-Wire and 4-Wire Modes with Six Status Bits (1)	1.35	100
	1	50
	0.5	16
	0.1	2.5

NOTE:

1. It is not necessary to clock out all six status bits. The minimum required SCLK frequency is reduced when clocking out fewer than six status bits.

APPLICATION INFORMATION (continued)

Register Read/Write Functionality

In Figure 1 and Figure 2, they show a register read operation and a register write operation, respectively. The read/write access command format is shown in Table 5.

If issuing a register read command, the read instruction consists of the 8-bit register access command, and the total instruction is 16-bit. The feedback data is MSB first.

If issuing a register write command, the instruction consists of the 8-bit register access command and an 8-bit register data. The configuration register is updated after the device receives the full byte.

When performing a read/write access command, the data on SDI pin is locked into device on the rising edge of the SCLK. The data is shifted out on SDO pin on the falling edge of the SCLK.

In daisy mode, the SGM51623D doesn't support register read operation.

Status Word

In Table 6, the status bit 5 to bit 0 can be shifted out by appended to the end of conversion result data. To shift out these 6 bits, it must enable this function in configuration register firstly.

In single chip application system, the status bits don't need be shifted out all 6 bits together. The status bits are shifted out on each falling edge of the SCLK, and MSB is the first bit.

In daisy-chain application system, once status bit shifting out is enabled, all six status bits of each device must be clocked out.

nCS Mode, 3-Wire Turbo Mode

The device can only get the maximum throughput rate of 2MSPS in turbo mode. The turbo mode is enabled by setting configuration register. In turbo mode, it provides more time for host controller to read out the previous conversion result.

In 3-wire turbo, the SDI is set to high, and a rising edge of CNV starts a conversion. Once the CNV goes low, the previous ADC conversion result is shifted out on SDO. The MSB is in the first bit. The following bits are shifted out on the subsequent falling edges of SCLK. The host controller can read the data at both SCLK edges. Reading at the falling edges will get a faster reading throughout rate. Refer to Figure 8.

Table 5. Register Access Command Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{WEN}$	R/$\overline{W}$	0	1	0	1	0	0

Table 6. Status Bits (Default Conditions)

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Over-Voltage (OV) Clamp Flag	Reserved	Reserved	Turbo Mode	Reserved	Reserved

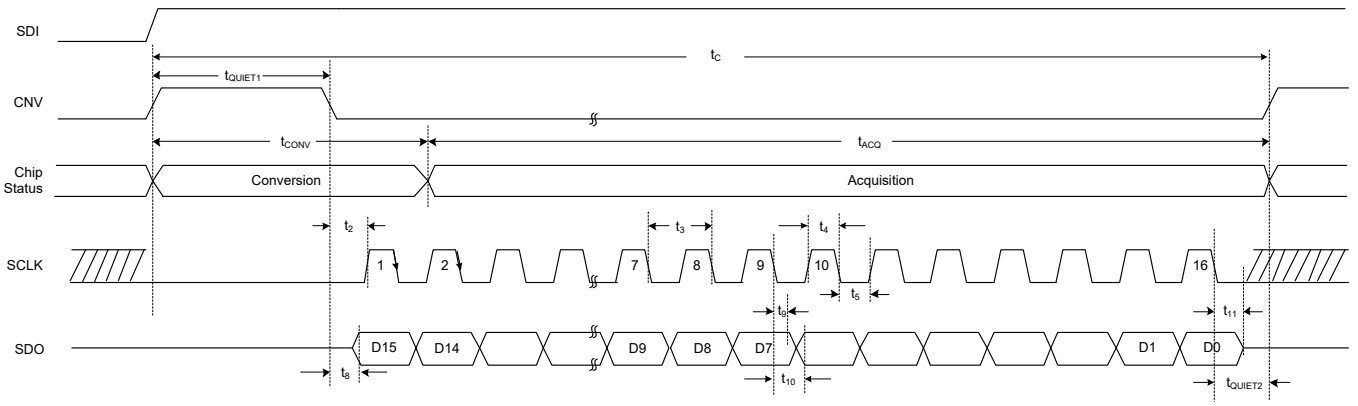


Figure 8. nCS Mode, 3-Wire Turbo Mode Serial Interface Timing Diagram (Status Bits Not Shown)

APPLICATION INFORMATION (continued)

nCS Mode, 3-Wire without Busy Indicator

In this mode, the turbo mode enable bit in configuration register must be cleared. And in this mode, the device shifts out the current frame conversion result, not the previous conversion results.

In this mode, a low to high change edge of CNV triggers a start of a conversion. During the conversion time, the device ignores the status of the CNV, CNV can be used for other operating in the system if needed. CNV must be pulled high before the conversion time elapses. During the conversion time, SCLK must be quiet (stay in a fixed logic), otherwise the logic flipping noise will decrease ADC SNR performance.

After the conversion completes, CNV goes low, the ADC conversion result is shifted out on SDO. The MSB is in the first bit. The following bits are shifted out on the subsequent falling edges of SCLK. The host controller can read the data at both SCLK edges. Reading at the falling edges will get a faster reading throughout rate. Refer to Figure 9 and Figure 10.

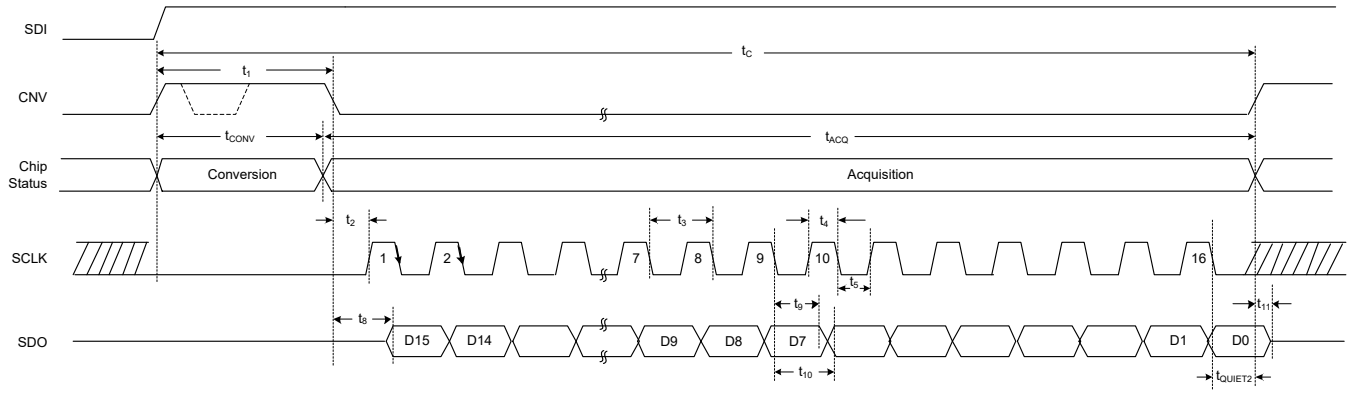


Figure 9. nCS Mode, 3-Wire without Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

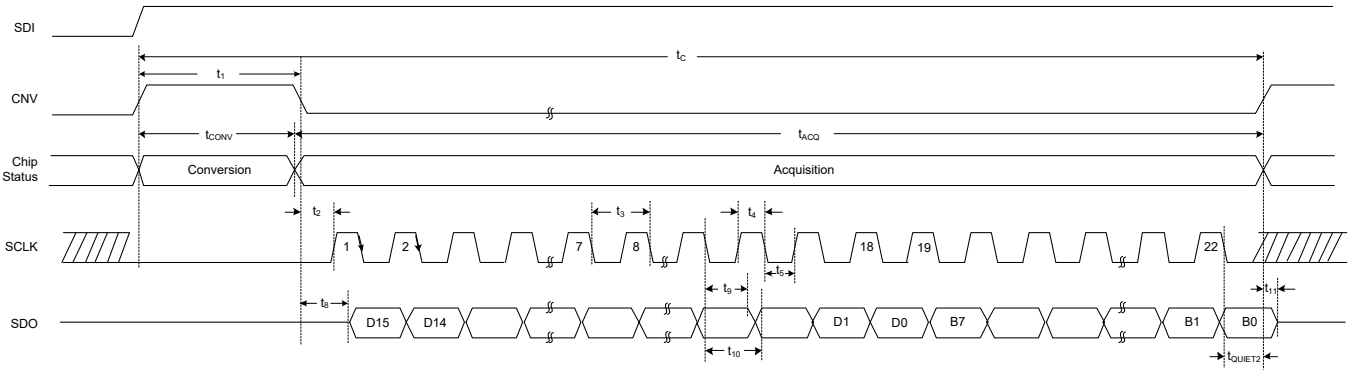


Figure 10. nCS Mode, 3-Wire without Busy Indicator Serial Interface Timing Diagram (Including Status Bits)

APPLICATION INFORMATION (continued)

nCS Mode, 3-Wire with Busy Indicator

In this mode, the turbo mode enable bit in configuration register must be cleared. And in this mode, the device shifts out the current frame conversion result, not the previous conversion results.

In this mode, a low to high change edge of CNV triggers a start of a conversion. During the conversion time, the device ignores the status of the CNV, CNV can be used for other operation in the system if needed. CNV must be pulled high before the conversion time elapses. During the conversion time, SCLK must be quiet (stay in a fixed logic), otherwise the logic flipping noise will decrease ADC SNR performance.

With the busy indicator mode enabled, after the conversion completes, SDO pin outputs low (during conversion, SDO is high impedance tri-state output). This transition can be used as an indicating signal to inform host controller. Then the MSB and other following data bits are shifting out on the SCLK falling edges.

The host controller can read the data at both SCLK edges. Reading at the falling edges will get a faster reading throughout rate. Refer to Figure 11.

nCS Mode, 4-Wire Turbo Mode

The device can only get the maximum throughput rate of 2MSPS in turbo mode. The turbo mode is enabled by setting configuration register. To enable this mode, the main controller must be enabled to write data over SDI to perform register reads and writes.

In turbo mode, it provides more time for host controller to read out the previous conversion result.

In 4-wire turbo mode, after SDI is set to high, a rising edge of CNV starts a conversion and forces SDO to high impedance. During all the cycle, CNV keeps in logic high. During the quiet time t_1, the device ignores the status of SDI. SDI can be used for other operation in the system if needed. SDI must be pulled high before the quiet time t_1 elapses.

Once the SDI goes low, the previous ADC conversion result is shifted out on SDO. The MSB is in the first bit. The remain following bits are shifted out on the subsequent falling edges of SCLK. The host controller can read the data at both SCLK edges. Reading at the falling edges will get a faster reading throughout rate. Refer to Figure 12.

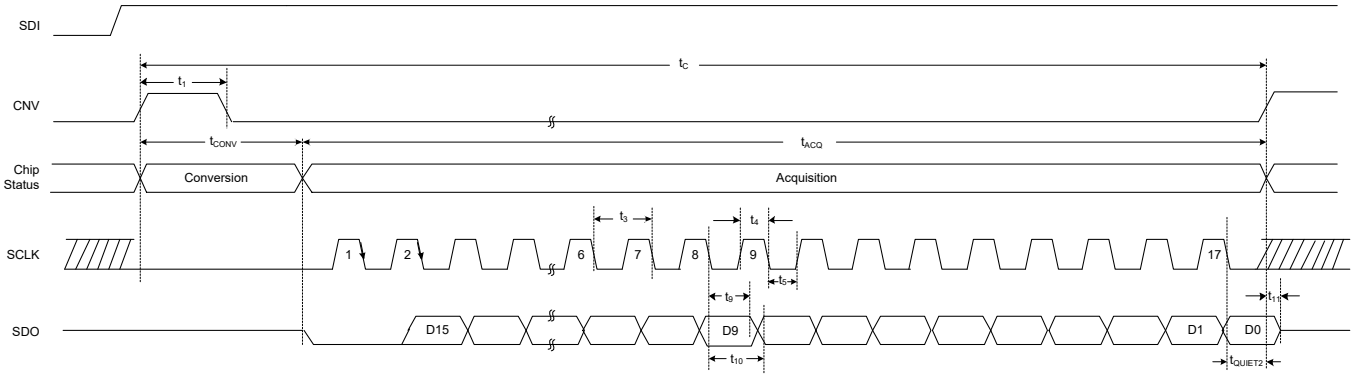


Figure 11. nCS Mode, 3-Wire with Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

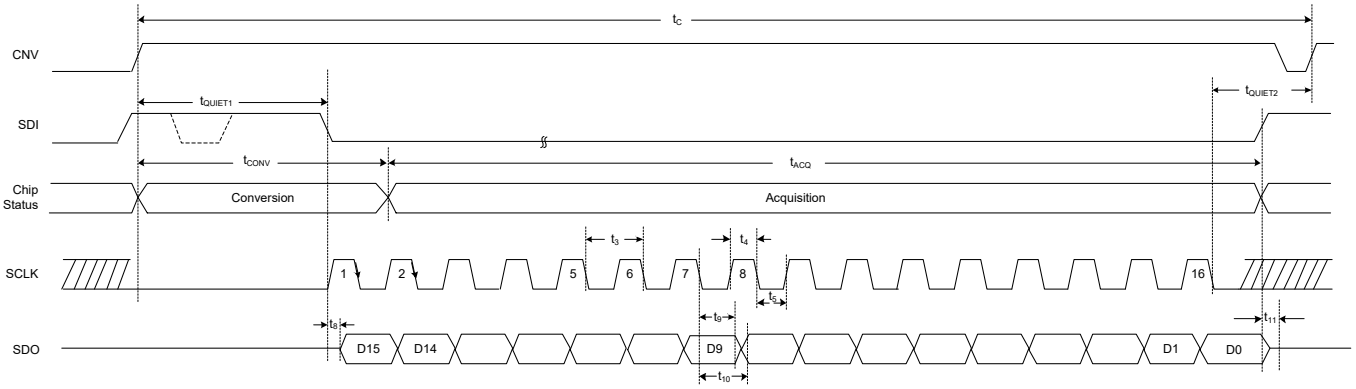


Figure 12. nCS Mode, 4-Wire Turbo Mode Timing Diagram (Status Bits Not Shown)

APPLICATION INFORMATION (continued)

nCS Mode, 4-Wire without Busy Indicator

In this mode, the turbo mode enable bit in configuration register must be cleared. And in this mode, the device shifts out the current frame conversion result, not the previous conversion results.

In this mode, a low to high change edge of CNV triggers a start of a conversion. During the conversion time and readback phase, CNV must be held high.

SDI must be high when the CNV rising edge triggers the conversion. During the conversion time, the device ignores the status of the SDI. SDI can be used for other operating in the system if needed. SDI must be pulled high before the minimum conversion time elapses and keep high for the maximum conversion time. During the conversion time, SCLK must be quiet (stay in a fixed logic), otherwise the logic flipping noise will decrease ADC SNR performance.

In this mode, SDI is a chip select input. Set SDI to low can select the corresponding chip (as shown in Figure 13, chip #N and chip #N+1 are selected by different SDI signals).

After the conversion completes, SDI goes low, the ADC conversion result is shifted out on SDO. The MSB is in the first bit. The following bits are shifted out on the subsequent falling edges of SCLK. The host controller can read the data on both SCLK edges. Reading at the falling edges will get a faster reading throughout rate.

nCS Mode, 4-Wire with Busy Indicator

In this mode, the turbo mode enable bit in configuration register must be cleared. And in this mode, the device shifts out the current frame conversion result, not the previous conversion results.

In this mode, a low to high change edge of CNV triggers a start of a conversion. During the conversion time and readback phase, CNV must be held high.

SDI must be high when the CNV rising edge triggers the conversion. During the conversion time, the device ignores the status of the SDI. SDI can be used for other operating in the system if needed. SDI must be pulled high before the minimum conversion time elapses and keep high for the maximum conversion time. During the conversion time, SCLK must be quiet (stay in a fixed logic), otherwise the logic flipping noise will decrease ADC SNR performance.

With the busy indicator mode enabled, after the conversion completes, SDO pin outputs low (during conversion, SDO is high impedance tri-state output). This transition can be used as an indicating signal to inform host controller. Then the MSB and other following data bits are shifting out on the SCLK falling edges. Refer to Figure 14.

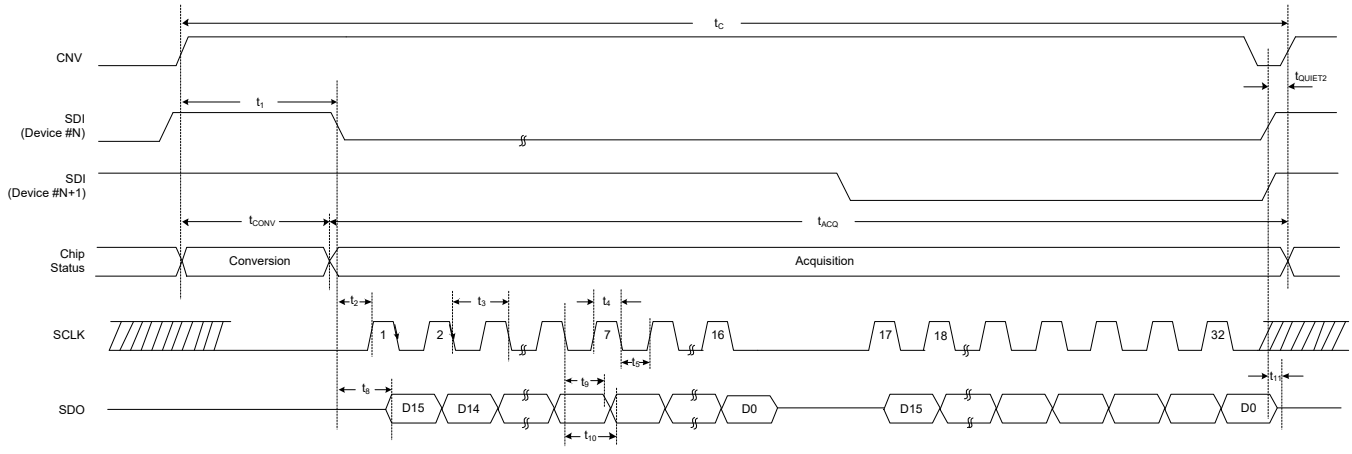


Figure 13. nCS Mode, 4-Wire without Busy Indicator Serial Interface Timing Diagram

APPLICATION INFORMATION (continued)

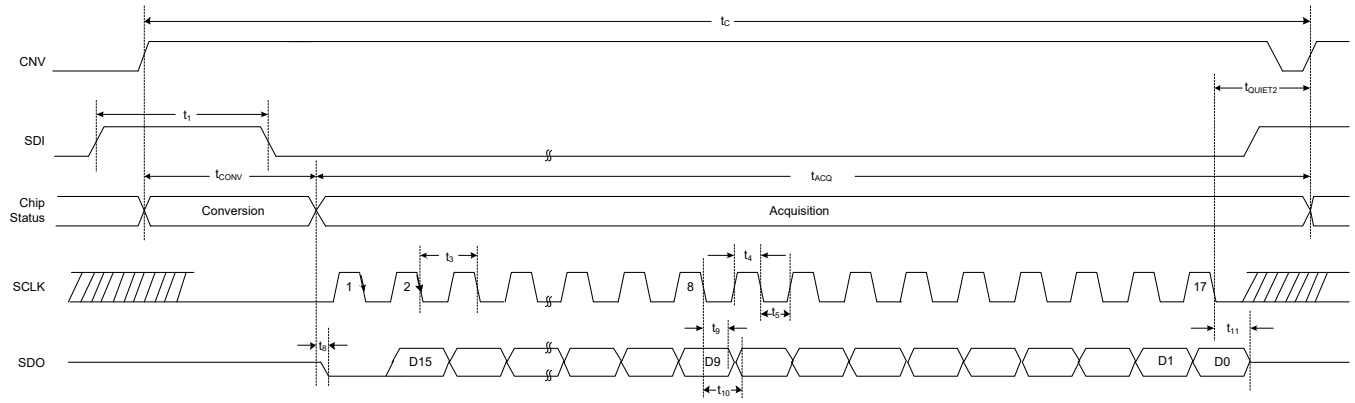


Figure 14. nCS Mode, 4-Wire with Busy Indicator Serial Interface Timing Diagram

Daisy-Chain Mode

A typical daisy-chain connection is shown in Figure 15. In daisy-chain mode, the turbo mode must be disabled.

In Figure 16, a rising edge of CNV initiates a conversion. During the conversion, SDO and SCLK must be quiet (stay in a fixed logic low), otherwise the logic flipping noise will decrease ADC SNR performance. CNV must be held high during the conversion and reading phase.

After conversion is completed, the MSB is output firstly, the following bits are shifted out on the subsequent falling edges of SCLK. The host controller can read the data at both SCLK edges. Reading at the falling edges will get a faster reading throughout rate.

In an X device system, total X × 16 SCLKs are needed to shift all the X ADCs conversion data.

In Figure 17, a writing timing sequence is shown. A 4-wire operation is required in daisy-chain system reading. During the reading process, CNV must be held low.

In an X device system, total (X + 1) × 8 SCLKs are needed to shift all command and data contents to the corresponding devices.

It is not possible to read register contents in daisy-chain mode.

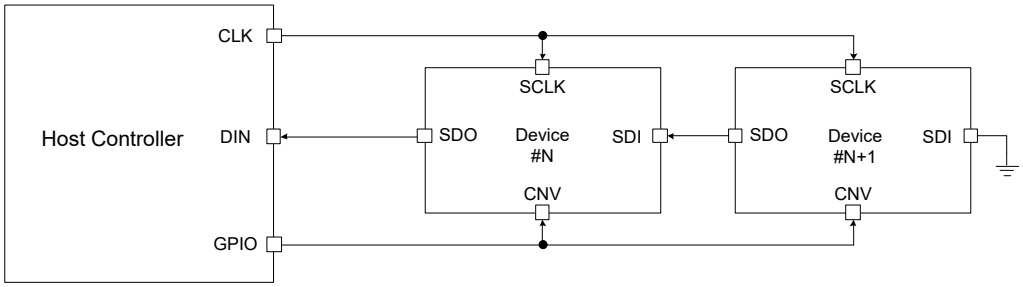


Figure 15. Daisy-Chain Mode Connection Diagram

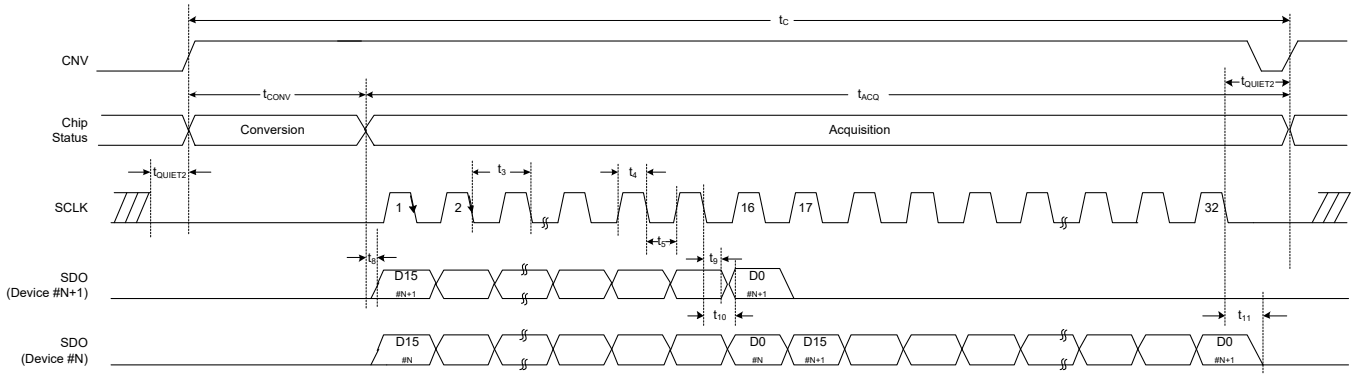


Figure 16. Daisy-Chain Mode Serial Interface Timing Diagram

APPLICATION INFORMATION (continued)

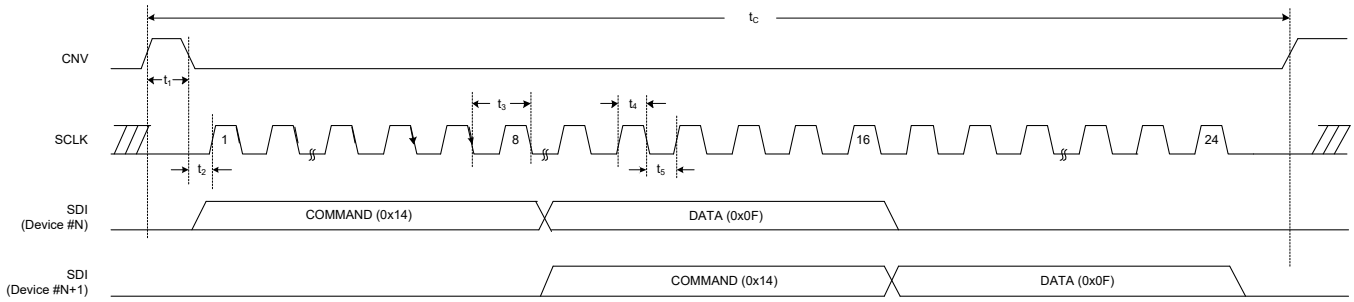


Figure 17. Register Write Timing Diagram, Daisy-Chain Mode

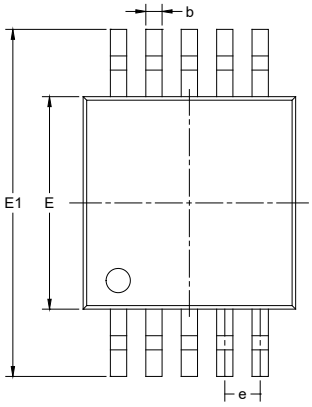
REVISION HISTORY

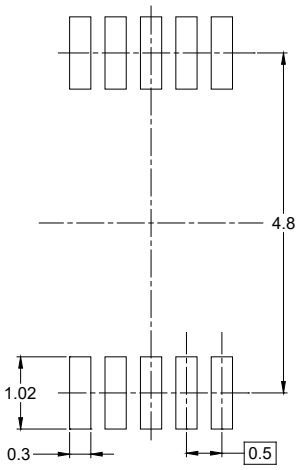
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

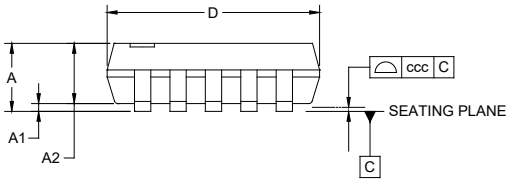
PACKAGE OUTLINE DIMENSIONS

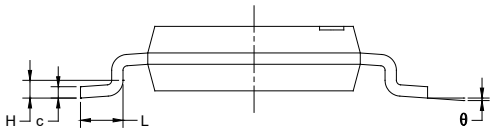
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)



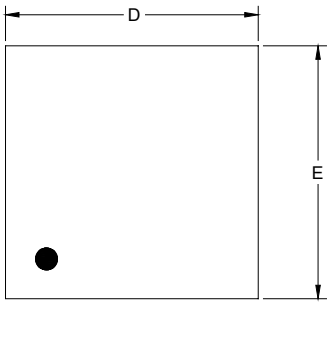


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.150
A2	0.750	-	0.950
b	0.170	-	0.330
c	0.080	-	0.230
D	2.900	-	3.100
E	2.900	-	3.100
E1	4.750	-	5.050
e	0.500 BSC		
H	0.250 TYP		
L	0.400	-	0.800
θ	0°	-	8°
ccc	0.100		

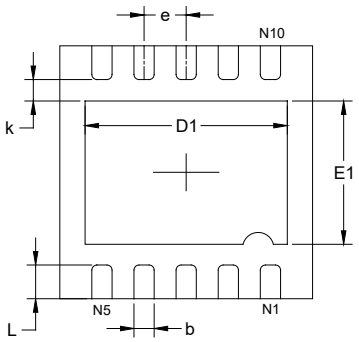
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

PACKAGE OUTLINE DIMENSIONS

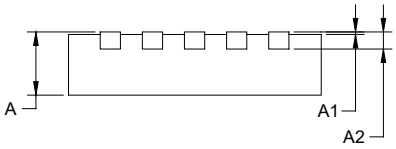
TDFN-3×3-10L



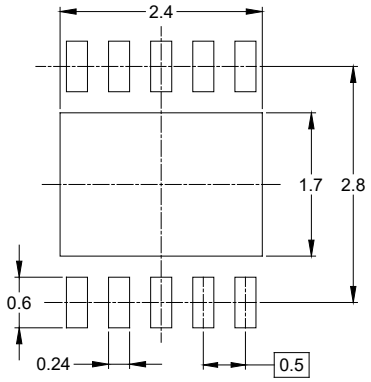
TOP VIEW



BOTTOM VIEW



SIDE VIEW



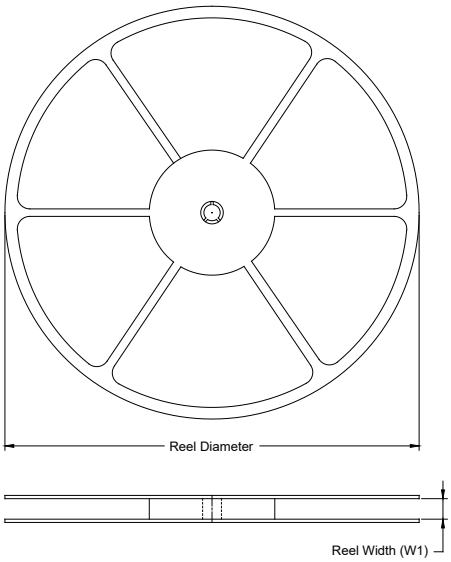
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

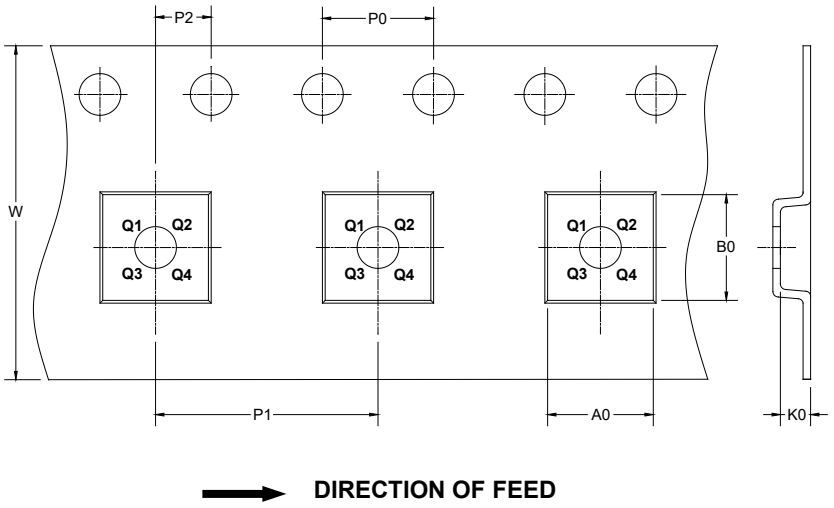
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



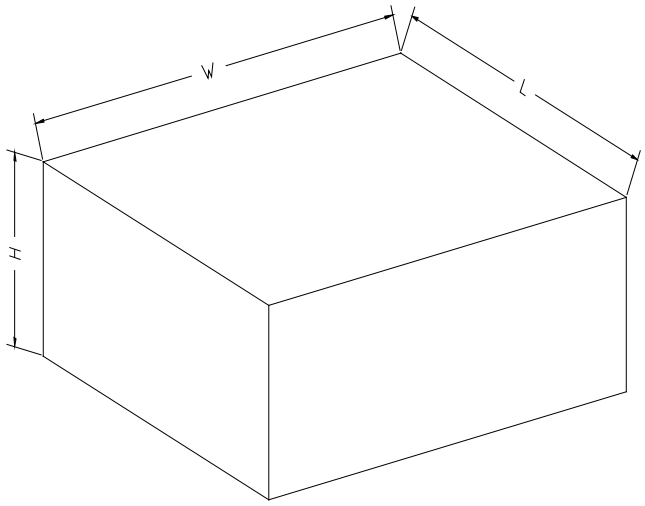
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002