SGM260421
High-Integration PMIC with 4 Bucks, 2 LDOs and Load Bypass Switches

GENERAL DESCRIPTION

The SGM260421 is a highly-integrated multi-channel power management circuit. It supports a variety of microcontrollers and solid-state drive applications. It incorporates four Bucks and two LDOs that deliver several output voltages. Buck1 and two LDOs can be set as a load switch while Buck4 can be set as an LDO. The device has several default configurations which are programmed in the factory. Startup sequencing, turn-on delay, extra delay, turn-off delay, wake-up delay, voltage of each channel, soft-start time, SLEEP or DPSLP state, operating modes, and other settings can all be configured.

SGM260421 supplies 8 configurable GPIOs for system hardware control requirements. These GPIOs can be programmed for a variety of functions, including nIRQ, SYSMON, SYSWARN, EXT_EN, I^2C controlled output, PG of internal rail, SLEEP/PWREN, PWRDIS, EN of internal rail. Otherwise, GPIO2 - GPIO4 can support three-state status for configuring the default output voltage, regulators operation mode, and extra turn-on delay times.

The SGM260421 is available in Green WLCSP-2.69×2.69-36B, FOCSP-3.35×3.1-34B and TBGA-3.35×3.1-34B packages.

APPLICATIONS

Solid-State Drives
FPGA
Microcontroller Applications
Personal Navigation Devices

FEATURES

- **Input Voltage Range: 2.7V to 5.5V**
- **Advanced PMIC:**
  - **Buck1: 1.7V to 2.9V, 20mV/Step, 4A, Configurable Bypass Function**
  - **Buck2: 0.5V to 1.33V, 10mV/Step, 3A**
  - **Buck3: 0.5V to 1.3V, 10mV/Step, 4A**
  - **Buck4: 0.8V to 2.0V, 10mV/Step, 2A, Configurable 400mA LDO**
  - **LDO1: 1V to 2.7V, 50mV/Step, 400mA, Configurable 400mA LSW**
  - **LDO2: 1V to 2.7V, 50mV/Step, 400mA, Configurable 400mA LSW**
  - **ACOT Control for Bucks**
- **Ultra-Low Quiescent Current**
- **Buck1 and LDO1, LDO2 Bypass Mode**
- **Flex Configurable**
  - **Output Voltage**
  - **Soft-Start Time**
  - **Startup Sequence**
  - **Switching Frequency**
  - **Current Limit**
  - **Status Reporting and Controllability via I^2C**
  - **8 Programmable GPIOs**
  - **Seamless Sequencing of External Supplies**
  - **Multiple SLEEP Modes**
- **I^2C Interface up to 3.4MHz**
- **Input OV/UV Protection**
- **Output OV/UV Protection**
- **Thermal Shutdown Protection**

PACKAGE/ORDERING INFORMATION

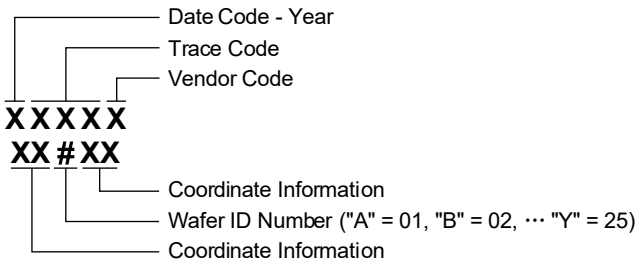
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM260421-001	TBGA-3.35×3.1-34B	-40℃ to +125℃	SGM260421-001XTBAE34G/TR	SGM21R TBAE34 XXXXX	Tape and Reel, 5000
SGM260421-002	WLCSP-2.69×2.69-36B	-40℃ to +125℃	SGM260421-002XG/TR	SGM 24E XXXXX XX#XX	Tape and Reel, 3000
SGM260421-003	FOCSP-3.35×3.1-34B	-40℃ to +125℃	SGM260421-003XG34/TR	24K XXXXX XX#XX	Tape and Reel, 5000
	TBGA-3.35×3.1-34B	-40℃ to +125℃	SGM260421-003XTBAE34G/TR	SGM27Z TBAE34 XXXXX	Tape and Reel, 5000
SGM260421-004	TBGA-3.35×3.1-34B	-40℃ to +125℃	SGM260421-004XTBAE34G/TR	SGM2C4 TBAE34 XXXXX	Tape and Reel, 5000
SGM260421-006	TBGA-3.35×3.1-34B	-40℃ to +125℃	SGM260421-006XTBAE34G/TR	SGM27U TBAE34 XXXXX	Tape and Reel, 5000

Green (RoHS & HSF): SG Micro Corp defines “Green” to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

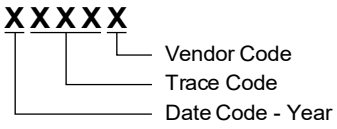
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

FOCSP-3.35×3.1-34B/WLCSP-2.69×2.69-36B



TBGA-3.35×3.1-34B



ABSOLUTE MAXIMUM RATINGS

All I/O and Power pins except PGND12, PGND34, AGND ..... -0.3V to 6V
Grounds: Any PGND referenced to AGND ..... -0.3V to 0.3V
SW_Bx to PGNDx..... -0.3V to 6V
SW_Bx to PGNDx (1ns Transient).....-2V
FB_Bx to AGND..... -0.3V to 6V
LDOx to AGND ..... -0.3V to 6V
Package Thermal Resistance
TBGA-3.35×3.1-34B, θ_{JA}..... 32.4℃/W
TBGA-3.35×3.1-34B, θ_{JB}..... 5.5℃/W
TBGA-3.35×3.1-34B, θ_{JC} ..... 21.5℃/W
WLCSP-2.69×2.69-36B, θ_{JA}..... 28.1℃/W
WLCSP-2.69×2.69-36B, θ_{JB}..... 4.5℃/W
WLCSP-2.69×2.69-36B, θ_{JC}..... 9.6℃/W
FOCSP-3.35×3.1-34B, θ_{JA} ..... 29.1℃/W
FOCSP-3.35×3.1-34B, θ_{JB} ..... 5.2℃/W
FOCSP-3.35×3.1-34B, θ_{JC} ..... 9.2℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

AVIN, VIN_B1, VIN_B2, VIN_B3, VIN_B4 (1) .....2.7V to 5.5V
VIN_LDO1
LDO Mode.....1.62V to 5.5V
LSW Mode .....1.62V to AVIN
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE: 1. The maximum input voltage of the device must be AVIN at all times.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

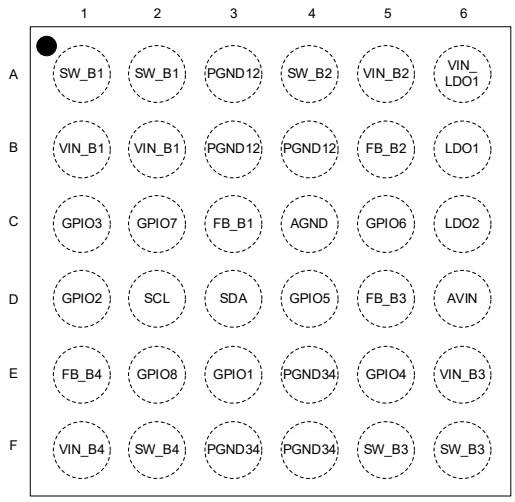
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

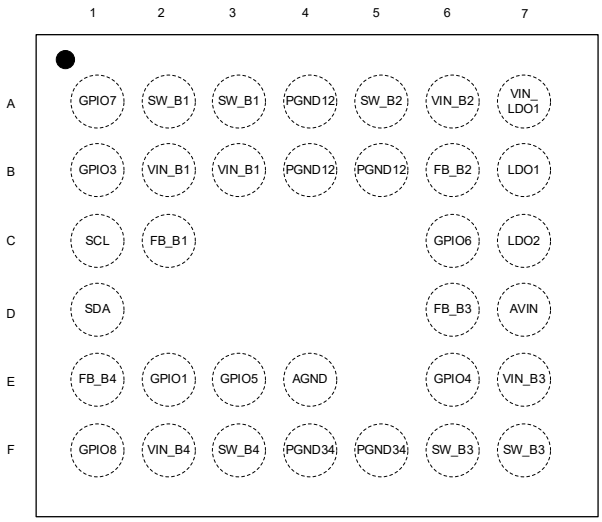
PIN CONFIGURATIONS

(TOP VIEW)



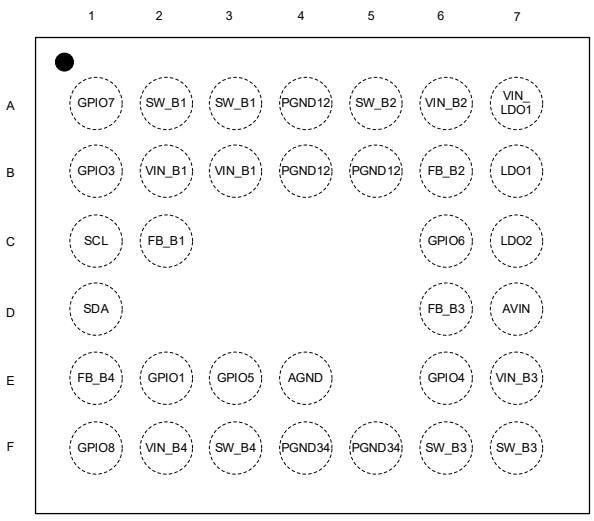
WLCSP-2.69×2.69-36B

(TOP VIEW)



FOCSP-3.35×3.1-34B

(TOP VIEW)



TBGA-3.35×3.1-34B

PIN DESCRIPTION

PIN		NAME	FUNCTION	
WLCSP	FOCSP/TBGA			
A3, B3, B4	A4, B4, B5	PGND12	Power Ground of Buck1 and Buck2.	The PGNDx pins are the dedicated power ground pins for the Buck converters, directly connecting to the low-side FETs of the Buck converters.
E4, F3, F4	F4, F5	PGND34	Power Ground of Buck3 and Buck4.	
C4	E4	AGND	Analog Ground. AGND is the analog ground pin for the analog circuitry and LDOs. It must be tied to the PGNDx pins, and this connection should not carry high currents.	
A1, A2	A2, A3	SW_B1	Switch Pin of Buck1.	SW_Bx are the switch nodes of the Buck converters, directly connected to the corresponding Buck inductor on the top PCB layer.
A4	A5	SW_B2	Switch Pin of Buck2.	
F5, F6	F6, F7	SW_B3	Switch Pin of Buck3.	
F2	F3	SW_B4	Switch Pin of Buck4.	
B1, B2	B2, B3	VIN_B1	VIN Power Input of Buck1.	Each Buck converter requires its VIN_Bx pin to be bypassed directly to the corresponding PGNDx pin on the top PCB layer using a high-quality ceramic capacitor.
A5	A6	VIN_B2	VIN Power Input of Buck2.	
E6	E7	VIN_B3	VIN Power Input of Buck3.	
F1	F2	VIN_B4	VIN Power Input of Buck4.	
C3	C2	FB_B1	Feedback of Buck1.	These are the feedback pins of the Buck regulators, which should be Kelvin-connected to the corresponding Buck output capacitors.
B5	B6	FB_B2	Feedback of Buck2.	
D5	D6	FB_B3	Feedback of Buck3.	
E1	E1	FB_B4	Feedback of Buck4.	
A6	A7	VIN_LDO1	VIN Power Input of LDO1. The dedicated input power pin for LDO1 is designated as VIN_LDO1. This pin must be bypassed directly to AGND on the top PCB layer using a 1μF ceramic capacitor.	
B6	B7	LDO1	Output of LDO1.	These are the LDO output pins. Each LDO output pin must be bypassed directly to AGND using a 1μF ceramic capacitor.
C6	C7	LDO2	Output of LDO2.	
D6	D7	AVIN	Analog Input Supply and Power Input of LDO2. This pin also monitors the VIN for over-voltage or under-voltage. AVIN is the input power pin for LDO2 and supplies power to the analog circuitry. It must be bypassed directly to AGND on the top PCB layer using a 1μF ceramic capacitor.	
D2	C1	SCL	I^2C Clock Input.	Standard I^2C interface pins for digital communication.
D3	D1	SDA	I^2C Data Input and Output.	
E3	E2	GPIO1	Configurable General Purpose I/O (Open-Drain or Push-Pull).	
D1	-	GPIO2		
C1	B1	GPIO3		
E5	E6	GPIO4		
D4	E3	GPIO5		
C5	C6	GPIO6		
C2	A1	GPIO7		
E2	F1	GPIO8		

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital I/O						
GPIOs Leakage Current	I_{LKG_GPIO}	Input = 5V			1	μA
GPIOs Output Low (Open-Drain)	V_{OL}	I_{OL} = 1mA			0.35	V
GPIOs Output High (Push-Pull)	V_{OH}	I_{OH} = 1mA	AVIN - 0.35			V
GPIOs Input Low (GPIO5/6/7/8)	$V_{5-8\_IO\_LOW}$				0.55	V
GPIOs Input High (GPIO5/6/7/8)	$V_{5-8\_IO\_HIGH}$		1.25			V
GPIOs Input Low (GPIO1/2/3/4)	$V_{1-4\_IO\_LOW}$				0.55	V
GPIOs Input Hi-Z (GPIO1/2/3/4)	$V_{1-4\_IO\_FLOAT}$			0.85		V
GPIOs Input High (GPIO1/2/3/4)	$V_{1-4\_IO\_HIGH}$		1.25			V
GPIOs Deglitch Time (1)	t_{IO_DEG}			5		μs
PWRSYSTEM Control						
Supply Voltage Range	V_{IN_Bx}	VIN_B1/VIN_B2 referenced to PGND12, VIN_B3/VIN_B4 referenced to PGND34	2.7		5.5	V
VIN_LDO1 Referenced to AGND	V_{IN_L1}	LDO Mode	1.62		5.5	V
	$V_{IN\_L1\_LSW}$	LSW Mode	1.62		AVIN	
AVIN UVLO Threshold Falling	$V_{AVIN\_UV\_F}$	VIN_LVL = 0	2.4	2.5	2.6	V
		VIN_LVL = 1	3.4	3.5	3.6	
AVIN UVLO Hysteresis	$V_{AVIN\_UV\_HYS}$	VIN_LVL = 0		100		mV
		VIN_LVL = 1		300		
AVIN Deglitch Time UV (1)	$t_{AVIN\_DEG\_UV}$	Falling, enter UV		10		μs
		Rising, exit UV		50		μs
AVIN OV Threshold Rising	$V_{AVIN\_OV\_R}$	VIN_OV_SET = 0	3.8	3.9	4.0	V
		VIN_OV_SET = 1	5.6	5.7	5.8	
AVIN OV Hysteresis	$V_{AVIN\_OV\_HYS}$		150	200	250	mV
AVIN Deglitch Time OV (1)	$t_{AVIN\_DEG\_OV}$	Rising, enter OV		10		μs
		Falling, exit OV		35		μs
AVIN POK_OV Interrupt Threshold Rising (Accuracy is only valid for register default setting, VIN_POK_OV_SET[1:0] = 01)	$V_{AVIN\_POK\_R}$	VIN_POK_OV_SET[1:0] = 00	3.4	3.5	3.6	V
		VIN_POK_OV_SET[1:0] = 01	3.6	3.7	3.8	
		VIN_POK_OV_SET[1:0] = 10	5.17	5.3	5.43	
		VIN_POK_OV_SET[1:0] = 11	5.35	5.5	5.65	
AVIN POK_OV Interrupt Threshold Hysteresis	$V_{AVIN\_POK\_HYS}$		100	200	300	mV
AVIN POK Deglitch Time (1)	$t_{AVIN\_DEG\_POK}$			5		μs

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWRSYSTEM Control						
Operating Supply Current	I_{SD}	All regulators disabled, I^2C is always available		9		μA
	I_Q	All regulators enabled, no load (normal mode)		140		
		All regulators enabled, no load (low-power mode)		115		
System Monitor (SYSMON) Programmable Range - Rising Threshold	V_{SYSMON_R}	In 25mV steps	2.725		3.1	V
AVIN System Monitor (SYSMON) Accuracy	$V_{SYSMON\_R\_ACC}$		-2.5	Set Point	2.5	%
AVIN System Monitor (SYSMON) Hysteresis	V_{SYSMON_HYS}			50		mV
AVIN System Warning (SYSWARN) Programmable Range - Rising Threshold	$V_{SYSWARN\_R}$	In 25mV steps	2.775		3.15	V
AVIN System Warning (SYSWARN) Accuracy	$V_{SYSWARN\_R\_ACC}$	In 25mV steps	-2.5	Set Point	2.5	%
AVIN System Monitor (SYSWARN) Hysteresis	$V_{SYSWARN\_HYS}$			50		mV
Thermal Shutdown Temperature (1)	T_{SD}	Temperature rising		155		℃
Thermal Shutdown Hysteresis (1)	T_{HYS}			30		℃
Thermal Interrupt Threshold (1)	T_{WARN}	Temperature rising, referenced to T_{SD}		T_{SD} - 30		℃
Thermal Interrupt Hysteresis (1)	T_{WARN_HYS}			20		℃
Startup Delay after Initial AVIN	t_{SYS_ON}			1000	1500	μs
Transition Time from SLEEP/DPSLP State to Active State (1)	t_{TRANS_GPIO}	Time from SLEEP/PWREN pin low-to-high transition to time when the first regulator turns on (start to ramp up) with minimum turn-on delay configuration		25		μs
	t_{TRANS_I2C}	Time from I^2C command to time when the first regulator turns on (start to ramp up) with minimum turn-on delay configuration		25		μs
Time to First Power Rail Turn-Off (1)	t_{OFF}	Time from turn-off command to when the first power rail turns off with minimum turn-off delay configuration		10		μs
Output OV/UV Retry Time (1)	t_{HICCUP_OFF}	System retry time in OVUVFLT state		200		ms

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck1						
Operating Voltage Range	V_{IN_B1}		2.7		5.5	V
Output Voltage Range	V_{OUT_B1}	Configurable in 20mV steps	1.7		2.9	V
Maximum Output Current	I_{B1_MAX}		4			A
Supply Current, Standby	I_{VIN_B1}	Normal mode, regulator current only, non-switching		17	27	μA
		Low-power mode, regulator current only, non-switching		14	24	μA
Output Voltage Accuracy	$V_{OUT\_B1\_ACC}$	T_J = +25℃	-1	V_{NOM}	1	%
		T_J = -40℃ to +125℃	-1.5	V_{NOM}	1.5	%
Line Regulation (1)		V_{IN_B1} = 2.7V to 5.5V		0.5		%/V
Load Regulation (1)		I_O = 0A to max rating		0.5		%/A
Power Good UV Threshold	$V_{PG\_B1\_UV}$	V_{OUT_B1} rising, PG becomes high	89.5	93	96.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_B1\_UV}$	V_{OUT_B1} falling, PG becomes low		3.5		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_B1\_OV}$	V_{OUT_B1} rising, PG becomes low	106	110	114	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_B1\_OV}$	V_{OUT_B1} falling, PG becomes high		3.5		$\%V_{NOM}$
OV/UV Deglitch Time (1)	$t_{DEG\_B1\_OV/UV}$	Time from B1 OV or UV to rails shutdown		150		μs
Switching Frequency	f_{SW_B1}	B1_FREQ_SET = 01		2		MHz
Switching Frequency Tolerance	$f_{SW\_B1\_ACC}$		-10		10	%
Soft-Start Period	t_{SS_B1}	B1_SS[1:0] = 00, 10%-90% of V_{OUT}		60		μs
		B1_SS[1:0] = 01, 10%-90% of V_{OUT}		75		
		B1_SS[1:0] = 10, 10%-90% of V_{OUT}		115		
		B1_SS[1:0] = 11, 10%-90% of V_{OUT}		175		
Internal Valley Current Limit (Accuracy is only valid for register default setting, B1_ILIM_SET[1:0] = 10)	I_{LIM_B1}	B1_ILIM_SET[1:0] = 00, T_J = +25℃	1.6	3		A
		B1_ILIM_SET[1:0] = 01, T_J = +25℃	3.0	4		
		B1_ILIM_SET[1:0] = 10, T_J = +25℃	4.3	5		
		B1_ILIM_SET[1:0] = 11, T_J = +25℃	5.3	6		
PMOS On-Resistance	$R_{DS\_ON\_P1}$	V_{IN_B1} = 3.3V		43		mΩ
NMOS On-Resistance	$R_{DS\_ON\_N1}$	V_{IN_B1} = 3.3V		36		mΩ
Output Discharge Resistance (1)	R_{DISCH_B1}	B1_DISCH_SET[1:0] = 00		5		Ω
		B1_DISCH_SET[1:0] = 01		10		
		B1_DISCH_SET[1:0] = 10		20		
		B1_DISCH_SET[1:0] = 11		40		
Buck1 Bypass Mode						
Input Voltage Range for Bypass Mode	$V_{IN\_B1\_LSW}$		2.7	3.3	3.7	V
Internal PMOS Current Shutdown	$I_{LIM\_B1\_LSW}$			5		A
Hiccup Off-Time (1)	$t_{HICCUP\_OFF\_LSW}$			14		ms
Internal PMOS Soft-Start (1)	$t_{SS\_B1\_LSW}$	$V_{IN\_B1\_LSW}$ = 3.3V, C_{OUT} = 44μF		190		μs
Over-Voltage Protection Threshold (1)	$V_{OV\_B1\_LSW}$			3.8		V
OV Deglitch Time (1)	$t_{DEG\_B1\_LSW\_OV}$			20		μs

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck2						
Operating Voltage Range	V_{IN_B2}		2.7		5.5	V
Output Voltage Range	V_{OUT_B2}	Configurable in 10mV steps	0.5		1.33	V
Maximum Output Current	I_{B2_MAX}		3			A
Supply Current, Standby	I_{VIN_B2}	Normal mode, regulator current only, non-switching		17	25	μA
		Low-power mode, regulator current only, non-switching		14	20	μA
Output Voltage Accuracy	$V_{OUT\_B2\_ACC}$	T_J = +25℃	-1	V_{NOM}	1	%
		T_J = -40℃ to +125℃	-1.5	V_{NOM}	1.5	%
Line Regulation (1)		V_{IN_B2} = 2.7V to 5.5V		0.5		%/V
Load Regulation (1)		I_O = 0A to max rating		0.5		%/A
Power Good UV Threshold	$V_{PG\_B2\_UV}$	V_{OUT_B2} rising, PG becomes high	89.5	93	96.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_B2\_UV}$	V_{OUT_B2} falling, PG becomes low		3.5		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_B2\_OV}$	V_{OUT_B2} rising, PG becomes low	106	110	114	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_B2\_OV}$	V_{OUT_B2} falling, PG becomes high		3.5		$\%V_{NOM}$
OV/UV Deglitch Time (1)	$t_{DEG\_B2\_OV/UV}$	Time from B2 OV or UV to rails shutdown		150		μs
Switching Frequency	f_{SW_B2}	B2_FREQ_SET[1:0] = 01		2		MHz
Switching Frequency Tolerance	$f_{SW\_B2\_ACC}$		-10		10	%
Soft-Start Period	t_{SS_B2}	B2_SS[1:0] = 00, 10%-90% of V_{OUT}		30		μs
		B2_SS[1:0] = 01, 10%-90% of V_{OUT}		55		
		B2_SS[1:0] = 10, 10%-90% of V_{OUT}		115		
		B2_SS[1:0] = 11, 10%-90% of V_{OUT}		175		
Internal Valley Current Limit (Accuracy is only valid for register default setting, B2_ILIM_SET[1:0] = 01)	I_{LIM_B2}	B2_ILIM_SET[1:0] = 00, T_J = +25℃	1.1	2		A
		B2_ILIM_SET[1:0] = 01, T_J = +25℃	2.3	3		
		B2_ILIM_SET[1:0] = 10, T_J = +25℃	3.0	4		
		B2_ILIM_SET[1:0] = 11, T_J = +25℃	3.8	5		
PMOS On-Resistance	$R_{DS\_ON\_P2}$	V_{IN_B2} = 3.3V		70		mΩ
NMOS On-Resistance	$R_{DS\_ON\_N2}$	V_{IN_B2} = 3.3V		30		mΩ
Output Discharge Resistance (1)	R_{DISCH_B2}	B2_DISCH_SET[1:0] = 00		5		Ω
		B2_DISCH_SET[1:0] = 01		10		
		B2_DISCH_SET[1:0] = 10		20		
		B2_DISCH_SET[1:0] = 11		40		

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck3						
Operating Voltage Range	V_{IN_B3}		2.7		5.5	V
Output Voltage Range	V_{OUT_B3}	Configurable in 10mV steps	0.5		1.3	V
Maximum Output Current	I_{B3_MAX}		4			A
Supply Current, Standby	I_{VIN_B3}	Normal mode, regulator current only, non-switching		17	25	μA
		Low-power mode, regulator current only, non-switching		14	20	μA
Output Voltage Accuracy	$V_{OUT\_B3\_ACC}$	T_J = +25℃	-1	V_{NOM}	1	%
		T_J = -40℃ to +125℃	-1.5	V_{NOM}	1.5	%
Line Regulation (1)		V_{IN_B3} = 2.7V to 5.5V		0.5		%/V
Load Regulation (1)		I_O = 0A to max rating		0.5		%/A
Power Good UV Threshold	$V_{PG\_B3\_UV}$	V_{OUT_B3} rising, PG becomes high	89.5	93	96.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_B3\_UV}$	V_{OUT_B3} falling, PG becomes low		3.5		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_B3\_OV}$	V_{OUT_B3} rising, PG becomes low	106	110	114	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_B3\_OV}$	V_{OUT_B3} falling, PG becomes high		3.5		$\%V_{NOM}$
OV/UV Deglitch Time (1)	$t_{DEG\_B3\_OV/UV}$	Time from B3 OV or UV to rails shutdown		150		μs
Switching Frequency	f_{SW_B3}	B3_FREQ_SET[1:0] = 01		2		MHz
Switching Frequency Tolerance	$f_{SW\_B3\_ACC}$		-10		10	%
Soft-Start Period	t_{SS_B3}	B3_SS[1:0] = 00, 10%-90% of V_{OUT}		30		μs
		B3_SS[1:0] = 01, 10%-90% of V_{OUT}		55		
		B3_SS[1:0] = 10, 10%-90% of V_{OUT}		115		
		B3_SS[1:0] = 11, 10%-90% of V_{OUT}		175		
Internal Valley Current Limit (Accuracy is only valid for register default setting, B3_ILIM_SET[1:0] = 01)	I_{LIM_B3}	B3_ILIM_SET[1:0] = 00, T_J = +25℃	3.3	4		A
		B3_ILIM_SET[1:0] = 01, T_J = +25℃	4.3	5		
		B3_ILIM_SET[1:0] = 10, T_J = +25℃	5.3	6		
		B3_ILIM_SET[1:0] = 11, T_J = +25℃	5.8	7		
PMOS On-Resistance	$R_{DS\_ON\_P3}$	V_{IN_B3} = 3.3V		56		mΩ
NMOS On-Resistance	$R_{DS\_ON\_N3}$	V_{IN_B3} = 3.3V		24		mΩ
Output Discharge Resistance (1)	R_{DISCH_B3}	B3_DISCH_SET[1:0] = 00		5		Ω
		B3_DISCH_SET[1:0] = 01		10		
		B3_DISCH_SET[1:0] = 10		20		
		B3_DISCH_SET[1:0] = 11		40		

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck4						
Operating Voltage Range	V_{IN_B4}		2.7		5.5	V
Output Voltage Range	V_{OUT_B4}	Configurable in 10mV steps	0.8		2.0	V
Maximum Output Current	I_{B4_MAX}		2			A
Supply Current, Standby	I_{VIN_B4}	Normal mode, regulator current only, non-switching		17	25	μA
		Low-power mode, regulator current only, non-switching		14	20	
Output Voltage Accuracy	$V_{OUT\_B4\_ACC}$	T_J = +25℃	-1	V_{NOM}	1	%
		T_J = -40℃ to +125℃	-1.5	V_{NOM}	1.5	%
Line Regulation (1)		V_{IN_B4} = 2.7V to 5.5V		0.5		%/V
Load Regulation (1)		I_O = 0A to max rating		0.5		%/A
Power Good UV Threshold	$V_{PG\_B4\_UV}$	V_{OUT_B4} rising, PG becomes high	89.5	93	93.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_B4\_UV}$	V_{OUT_B4} falling, PG becomes low		3.5		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_B4\_OV}$	V_{OUT_B4} rising, PG becomes low	106	110	114	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_B4\_OV}$	V_{OUT_B4} falling, PG becomes high		3.5		$\%V_{NOM}$
OV/UV Deglitch Time (1)	$t_{DEG\_B4\_OV/UV}$	Time from B4 OV or UV to rails shutdown		150		μs
Switching Frequency	f_{SW_B4}	B4_FREQ_SET[1:0] = 01		2		MHz
Switching Frequency Tolerance	$f_{SW\_B4\_ACC}$		-10		10	%
Soft-Start Period	t_{SS_B4}	B4_SS[1:0] = 00, 10%-90% of V_{OUT}		30		μs
		B4_SS[1:0] = 01, 10%-90% of V_{OUT}		55		
		B4_SS[1:0] = 10, 10%-90% of V_{OUT}		115		
		B4_SS[1:0] = 11, 10%-90% of V_{OUT}		175		
Internal Valley Current Limit (Accuracy is only valid for register default setting, B4_ILIM_SET[1:0] = 01)	I_{LIM_B4}	B4_ILIM_SET[1:0] = 00, T_J = +25℃	1.0	2		A
		B4_ILIM_SET[1:0] = 01, T_J = +25℃	2.3	3		
		B4_ILIM_SET[1:0] = 10, T_J = +25℃	3.2	4		
		B4_ILIM_SET[1:0] = 11, T_J = +25℃	4.2	5		
PMOS On-Resistance	$R_{DS\_ON\_P4}$	V_{IN_B4} = 3.3V		74		mΩ
NMOS On-Resistance	$R_{DS\_ON\_N4}$	V_{IN_B4} = 3.3V		40		mΩ
Output Discharge Resistance (1)	R_{DISCH_B4}	B4_DISCH_SET[1:0] = 00		5		Ω
		B4_DISCH_SET[1:0] = 01		10		
		B4_DISCH_SET[1:0] = 10		20		
		B4_DISCH_SET[1:0] = 11		40		

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck4 LDO Mode						
Operating Voltage Range	$V_{IN\_B4\_LDO}$		2.7		5.5	V
Output Voltage Range	$V_{OUT\_B4\_LDO}$	Configurable in 10mV steps	0.8		2.0	V
Output Current	$I_{B4\_LDO\_MAX}$	V_{IN_B4} = 2.7V to 5.5V, B4_LDO_ILIM_SET = 1	0.4			A
Output Voltage Accuracy	$V_{OUT\_B4\_LDO\_ACC}$	$V_{IN\_B4\_LDO}$ - $V_{OUT\_B4\_LDO}$ > 0.4V, T_J = +25℃	-1	V_{SET}	1	%
Output Voltage Accuracy	$V_{OUT\_B4\_LDO\_ACC}$	$V_{IN\_B4\_LDO}$ - $V_{OUT\_B4\_LDO}$ > 0.4V, T_J = -40℃ to +125℃	-1.5	V_{SET}	1.5	%
Line Regulation (1)		V_{IN_B4} = 2.7V to 5.5V, $I_{B4\_LDO\_OUT}$ = 1mA		0.5		%/V
Load Regulation (1)		$I_{B4\_LDO\_OUT}$ = 1mA to 400mA, B4_LDO_ILIM_SET = 1,		0.5		%/A
Supply Current	$I_{VIN\_B4\_LDO}$	Regulator enabled no load, normal power mode		20	28	μA
		Regulator enabled no load, low-power mode		7	15	μA
Soft-Start Period	$t_{SS\_B4\_LDO}$	B4_SS_LDO = 0, 10%-90% of V_{OUT}		55		μs
		B4_SS_LDO = 1, 10%-90% of V_{OUT}		100		
Power Good UV Threshold	$V_{PG\_B4\_LDO\_UV}$	$V_{OUT\_B4\_LDO}$ rising, PG becomes high	81.5	85	88.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_B4\_LDO\_UV}$	$V_{OUT\_B4\_LDO}$ falling, PG becomes low		3		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_B4\_LDO\_OV}$	$V_{OUT\_B4\_LDO}$ rising, PG becomes low	111	115	119	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_B4\_\_LDO\_OV}$	$V_{OUT\_B4\_LDO}$ falling, PG becomes high		8		$\%V_{NOM}$
Discharge Resistance (1)	$R_{DISCH\_B4\_LDO}$	Enabled when regulator disabled		4.4		Ω
Output Current Limit (Accuracy is only valid for register default setting, B4_LDO_ILIM_SET = 0)	$I_{LIM\_B4\_LDO}$	B4_LDO_ILIM_SET = 0, T_J = +25℃	300	400		mA
		B4_LDO_ILIM_SET = 1, T_J = +25℃	400	500		

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO1							
Operating Voltage Range	V_{IN_L1}			1.62		5.5	V
Output Voltage Range	V_{OUT_L1}	Configurable in 50mV steps		1		2.7	V
Output Current	I_{OUT_L1}	V_{IN_L1} = 1.62V (2) to 5.5V, L1_ILIM_SET = 1		0.4			A
Output Voltage Accuracy	$V_{OUT\_L1\_ACC}$	V_{IN_L1} - V_{OUT_L1} > 0.4V	T_J = +25℃	-1	V_{NOM}	1	%
			T_J = -40℃ to +125℃	-1.5	V_{NOM}	1.5	%
Line Regulation (1)		V_{IN_L1} - V_{OUT_L1} > 0.4V, V_{IN_L1} = 2.7V to 5.5V, I_{OUT_L1} = 1mA			0.5		%/V
Load Regulation (1)		I_{OUT_L1} = 1mA to 400mA, V_{IN_L1} - V_{OUT_L1} > 0.4V			0.5		%/A
Supply Current	I_{VIN_L1}	Regulator enabled no load, normal power mode			20	28	μA
		Regulator enabled no load, low-power mode			7	15	μA
Soft-Start Period	t_{SS_L1}	L1_SS = 0, 10%-90% of V_{OUT}			55		μs
		L1_SS = 1, 10%-90% of V_{OUT}			100		
Power Good UV Threshold	$V_{PG\_L1\_UV}$	V_{OUT_L1} rising, PG becomes high		81.5	85	88.5	%V_{NOM}
Power Good UV Hysteresis	$V_{PG\_HYS\_L1\_UV}$	V_{OUT_L1} falling, PG becomes low			3		%V_{NOM}
Power Good OV Threshold	$V_{PG\_L1\_OV}$	V_{OUT_L1} rising, PG becomes low		111	115	119	%V_{NOM}
Power Good OV Hysteresis	$V_{PG\_HYS\_L1\_OV}$	V_{OUT_L1} falling, PG becomes high			8		%V_{NOM}
Dropout Voltage	V_{L1_DROP}	I_{OUT_L1} = 200mA, V_{IN_L1} > 2.7V, L1_ILIM_SET = 0				200	mV
		I_{OUT_L1} = 400mA, V_{IN_L1} > 2.7V, L1_ILIM_SET = 1				300	mV
Output Discharge Resistance (1)	R_{DISCH_L1}	L1_DISCH_SET[1:0] = 00			10		Ω
		L1_DISCH_SET[1:0] = 01			20		
		L1_DISCH_SET[1:0] = 10			40		
		L1_DISCH_SET[1:0] = 11			80		
Output Current Limit (Accuracy is only valid for register default setting, L1_ILIM_SET = 1)	I_{LIM_L1}	V_{IN_L1} - V_{OUT_L1} > 0.4V, T_J = +25℃	L1_ILIM_SET = 0	300	400		mA
			L1_ILIM_SET = 1	400	500		
LDO1 Load Switch							
Load Switch Operation Range	$V_{IN\_L1\_LSW}$			1.62		AVIN	V
Load Switch On-Resistance (1)	$R_{DS\_ON\_L1\_LSW}$				200		mΩ
Load Switch Supply Current	$I_{VIN\_L1\_LSW}$	LSW mode, no load			18	28	μA
Soft-Start Period (1)	$t_{SS\_L1\_LSW}$	V_{IN_L1} = 3.3V, C_{OUT} = 1μF			190		μs
Output Current Limit (Accuracy is only valid for register default setting, L1_ILIM_SET = 1)	$I_{LIM\_L1\_LSW}$	L1_ILIM_SET = 0, T_J = +25℃		300	400		mA
		L1_ILIM_SET = 1, T_J = +25℃		400	500		
Over-Voltage Protection Threshold (1)	$V_{OV\_L1\_LSW}$				3.8		V
OV Deglitch Time (1)	$t_{DEG\_L1\_LSW\_OV}$				20		μs

NOTES:

1. Guaranteed by design and laboratory test, not tested in production.
2. LDO1 does not have the ability to output with full load at V_{IN_L1} = 1.62V.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO2							
Operating Voltage Range	V_{IN_L2}			2.7		5.5	V
Output Voltage Range	V_{OUT_L2}	Configurable in 50mV steps		1		2.7	V
Output Current	I_{OUT_L2}	AVIN = 2.7V to 5.5V, L2_ILIM_SET = 1		0.4			A
Output Voltage Accuracy	$V_{OUT\_L2\_ACC}$	AVIN - V_{OUT_L2} > 0.4V	T_J = +25℃	-1	V_{SET}	1	%
			T_J = -40℃ to +125℃	-1.5	V_{SET}	1.5	%
Line Regulation (1)		AVIN - V_{OUT_L2} > 0.4V, AVIN = 2.7V to 5.5V, I_{OUT_L2} = 1mA			0.5		%/V
Load Regulation (1)		I_{OUT_L2} = 1mA to 400mA, AVIN - V_{OUT_L2} > 0.4V			0.5		%/A
Supply Current	I_{VIN_L2}	Regulator enabled no load, normal power mode			20	28	μA
		Regulator enabled no load, low-power mode			7	15	μA
Soft-Start Period	t_{SS_L2}	L2_SS = 0, 10%-90% of V_{OUT}			55		μs
		L2_SS = 1, 10%-90% of V_{OUT}			100		
Power Good UV Threshold	$V_{PG\_L2\_UV}$	V_{OUT_L2} rising, PG becomes high		81.5	85	88.5	$\%V_{NOM}$
Power Good UV Hysteresis	$V_{PG\_HYS\_L2\_UV}$	V_{OUT_L2} falling, PG becomes low			3		$\%V_{NOM}$
Power Good OV Threshold	$V_{PG\_L2\_OV}$	V_{OUT_L2} rising, PG becomes low		111	115	119	$\%V_{NOM}$
Power Good OV Hysteresis	$V_{PG\_HYS\_L2\_OV}$	V_{OUT_L2} falling, PG becomes high			8		$\%V_{NOM}$
Dropout Voltage	V_{L2_DROP}	I_{OUT_L2} = 200mA, AVIN > 2.7V, L2_ILIM_SET = 0				200	mV
		I_{OUT_L2} = 400mA, AVIN > 2.7V, L2_ILIM_SET = 1				300	
Output Discharge Resistance (1)	R_{DISCH_L2}	L2_DISCH_SET[1:0] = 00			10		Ω
		L2_DISCH_SET[1:0] = 01			20		
		L2_DISCH_SET[1:0] = 10			40		
		L2_DISCH_SET[1:0] = 11			80		
Output Current Limit (Accuracy is only valid for register default setting, L2_ILIM_SET = 1)	I_{LIM_L2}	AVIN - V_{OUT_L2} > 0.4V, T_J = +25℃	L2_ILIM_SET = 0	280	400		mA
			L2_ILIM_SET = 1	400	500		
LDO2 Load Switch							
Load Switch Operation Range	$V_{IN\_L2\_LSW}$			2.7		5.5	V
PMOS On-Resistance (1)	$R_{DS\_ON\_L2\_LSW}$				200		mΩ
Load Switch Supply Current	$I_{VIN\_L2\_LSW}$	LSW mode, no load			18	28	μA
Soft-Start Period (1)	$t_{SS\_L2\_LSW}$	AVIN = 3.3V, C_{OUT} = 1μF			190		μs
Output Current Limit (Accuracy is only valid for register default setting, L2_ILIM_SET = 1)	$I_{LIM\_L2\_LSW}$	L2_ILIM_SET = 0, T_J = +25℃		280	400		mA
		L2_ILIM_SET = 1, T_J = +25℃		400	500		
Over-Voltage Protection Threshold (1)	$V_{OV\_L2\_LSW}$				3.8		V
OV Deglitch Time (1)	$t_{DEG\_L2\_LSW\_OV}$				20		μs

NOTE: 1. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Interface						
SCL/SDA Input Low	V_{IL_I2C}	AVIN = 3.3V			0.55	V
SCL/SDA Input High	V_{IH_I2C}	AVIN = 3.3V	1.25			V
SDA Leakage Current	V_{LKG_SDA}	V_{SDA} = 5V			1	μA
SDA Output Low	V_{OL_SDA}	I_{OL_SDA} = 5mA			0.35	V
SCL Clock Frequency	f_{SCL}				3400	kHz
SCL Low Period	t_{LOW}		160			μs
SCL High Period	t_{HIGH}		60			μs
SDA Data Setup Time	t_{SU_DAT}		20			ns
SDA Data Hold Time	t_{HD_DAT}		0			ns
Start Setup Time	t_{SU_STA}	For start condition	160			ns
Stop Setup Time	t_{SU_STO}	For stop condition	160			ns
Capacitance on SCL/SDA Pin	C_S				10	pF
SDA/SCL Rise Time	t_R	Device requirement			40	ns
SDA/SCL Fall Time	t_F	Device requirement			40	ns

I²C TIMING DIAGRAM

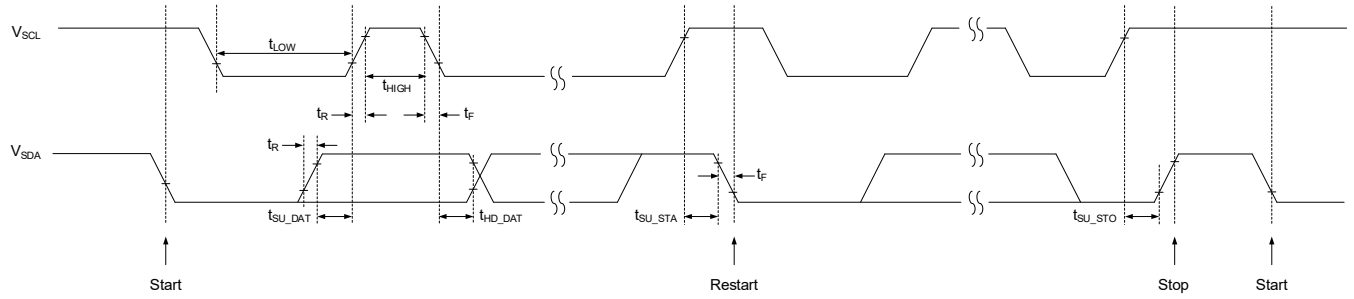
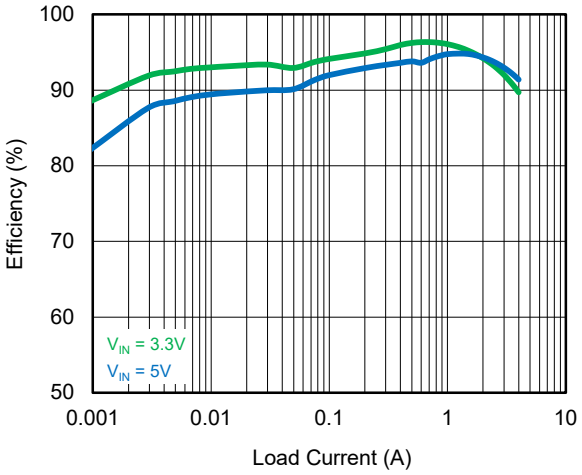


Figure 1. I²C Timing Diagram

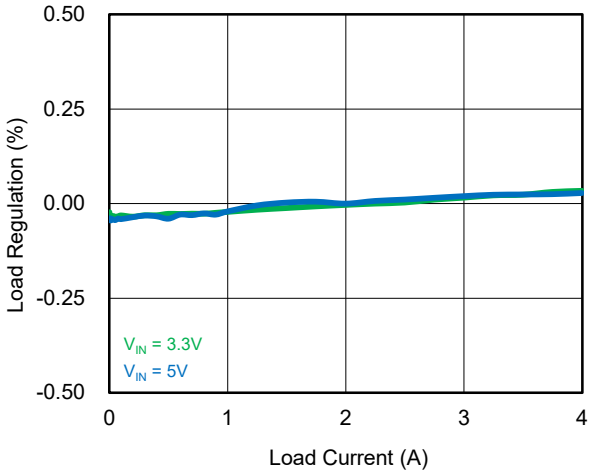
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = 3.3V, f = 2MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

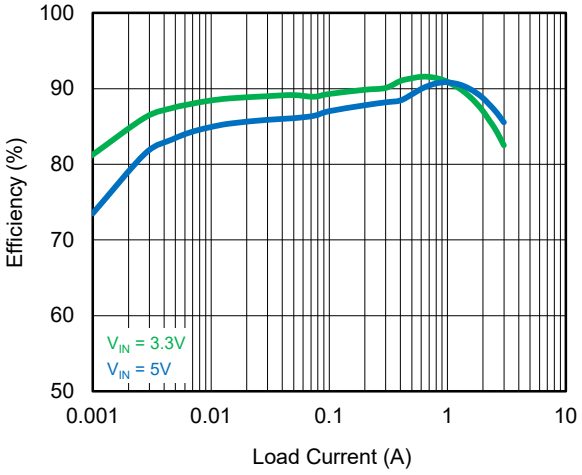
Efficiency vs. Load Current (V_{OUT_B1} = 2.5V)



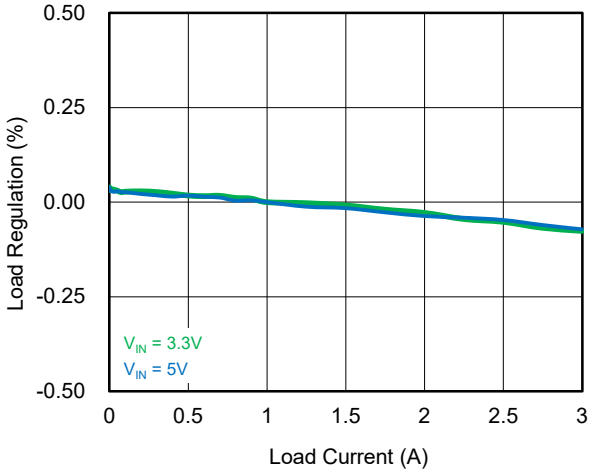
Load Regulation (V_{OUT_B1} = 2.5V)



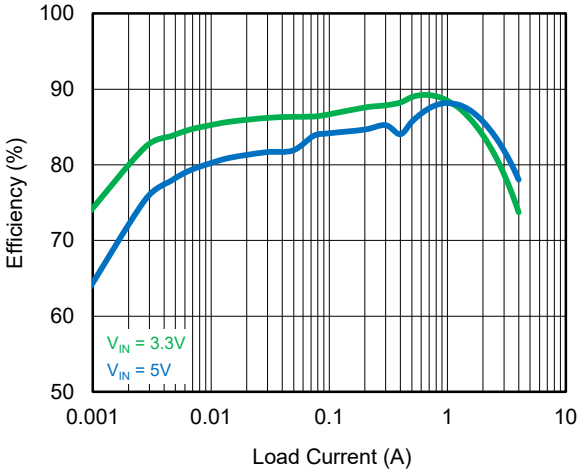
Efficiency vs. Load Current (V_{OUT_B2} = 1.2V)



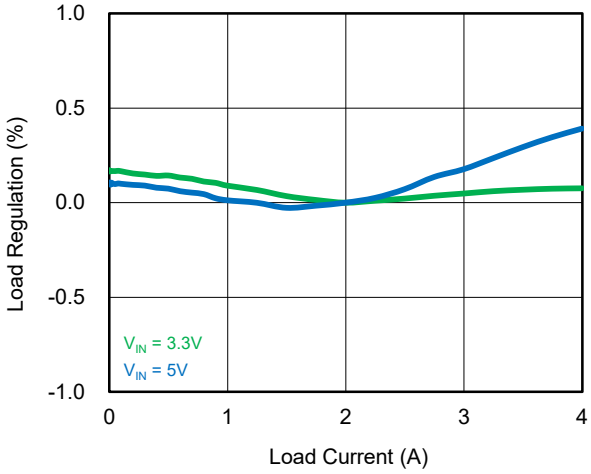
Load Regulation (V_{OUT_B2} = 1.2V)



Efficiency vs. Load Current (V_{OUT_B3} = 0.75V)



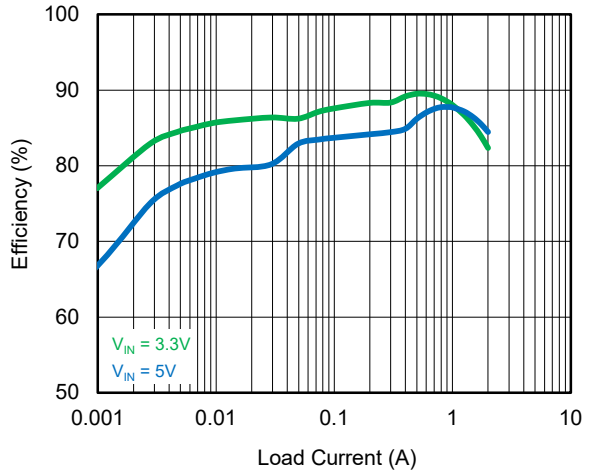
Load Regulation (V_{OUT_B3} = 0.75V)



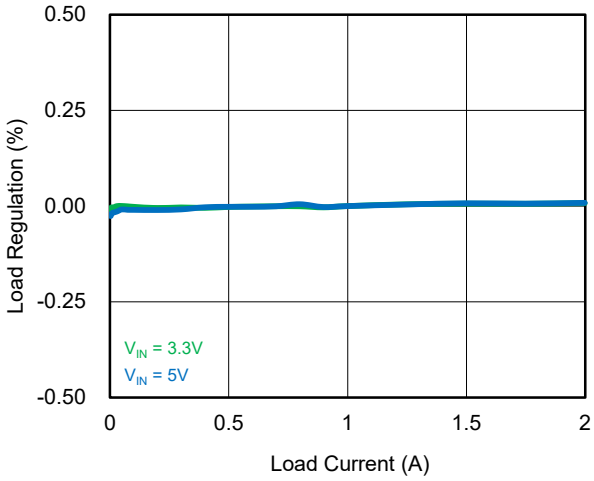
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 3.3V, f = 2MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

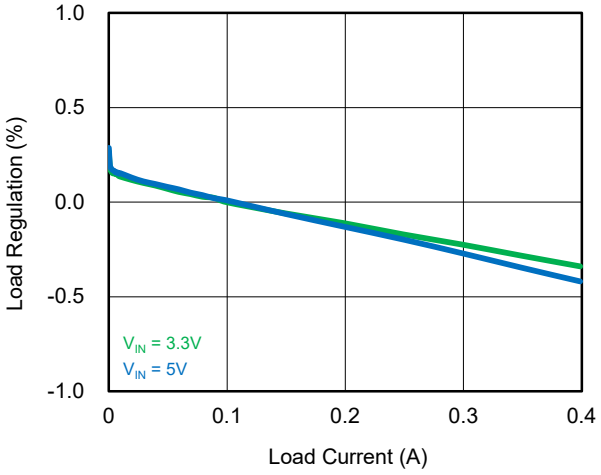
Efficiency vs. Load Current (V_{OUT_B4} = 0.9V)



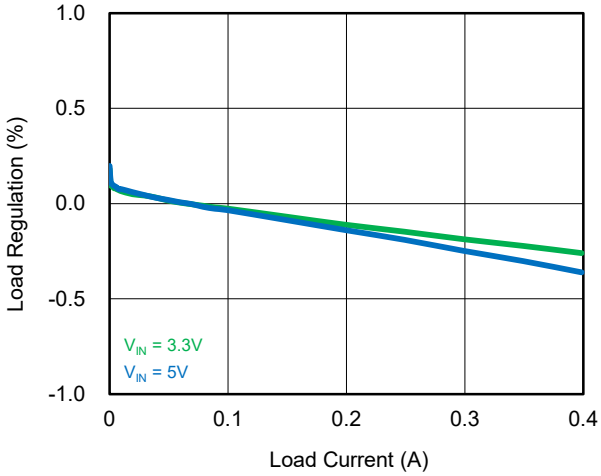
Load Regulation (V_{OUT_B4} = 0.9V)



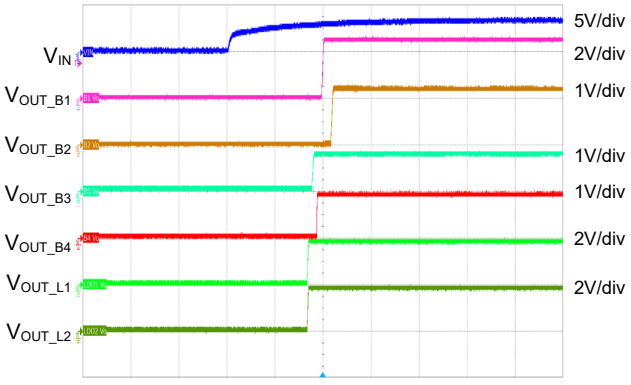
Load Regulation (V_{OUT_L1} = 1.8V)



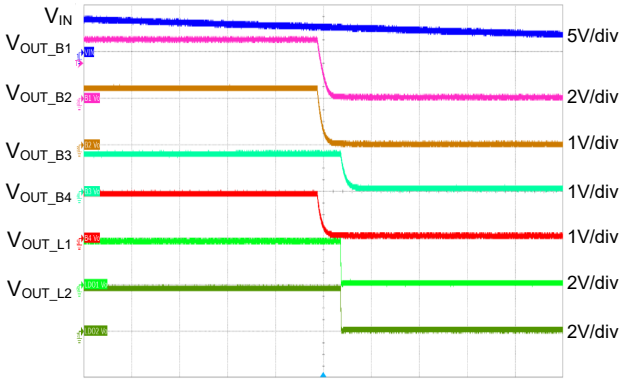
Load Regulation (V_{OUT_L2} = 1.8V)



CMI 001 Power-Up Sequence (GPIO3 = Float)



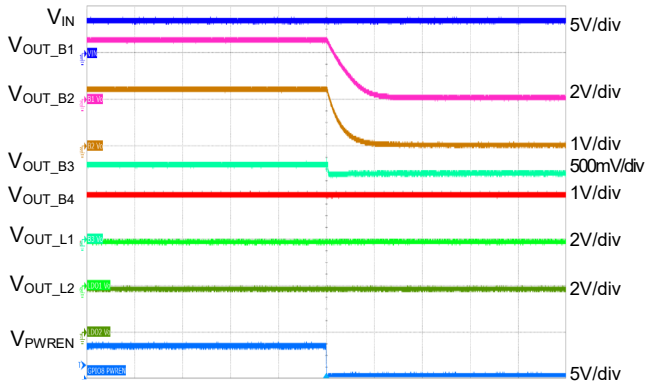
CMI 001 Power-Down Sequence (GPIO3 = Float)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

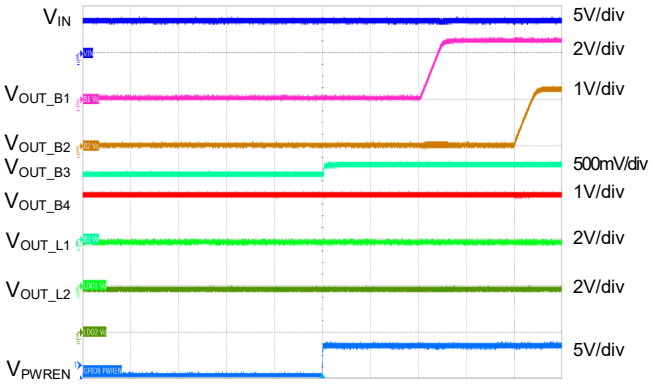
T_J = +25℃, V_{IN} = 3.3V, f = 2MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

Enter DPSLP



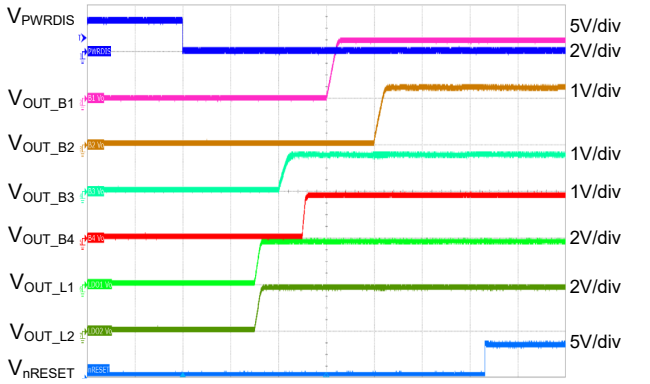
Time (500μs/div)

Exit DPSLP



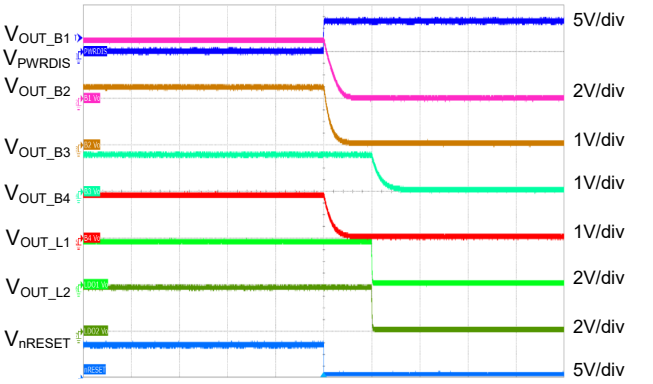
Time (500μs/div)

PWRDIS Power On



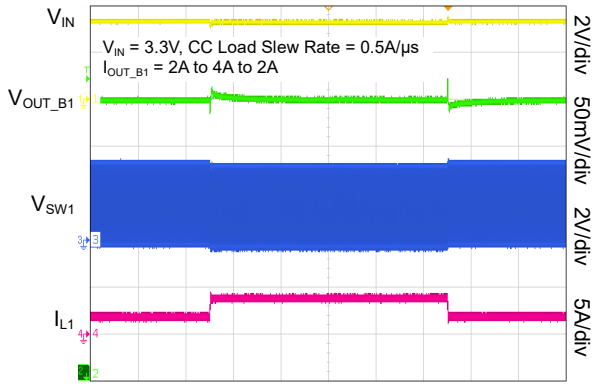
Time (1ms/div)

PWRDIS Power Off



Time (1ms/div)

Load Transient (V_{OUT_B1} = 2.5V)



Time (200μs/div)

Load Transient (V_{OUT_B2} = 1.2V)

Time (200μs/div)

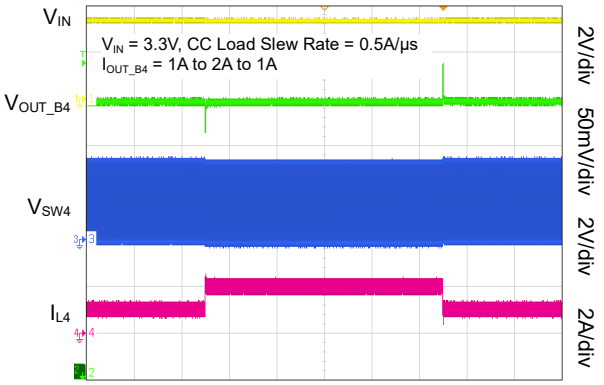
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 3.3V, f = 2MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

Load Transient (V_{OUT_B3} = 0.75V)

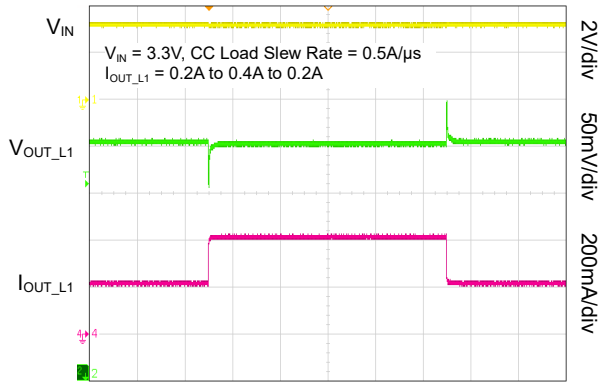
Time (200μs/div)

Load Transient (V_{OUT_B4} = 0.9V)



Time (200μs/div)

Load Transient (V_{OUT_L1} = 1.8V)



Time (200μs/div)

Load Transient (V_{OUT_L2} = 1.8V)

Time (200μs/div)

TYPICAL APPLICATION CIRCUIT

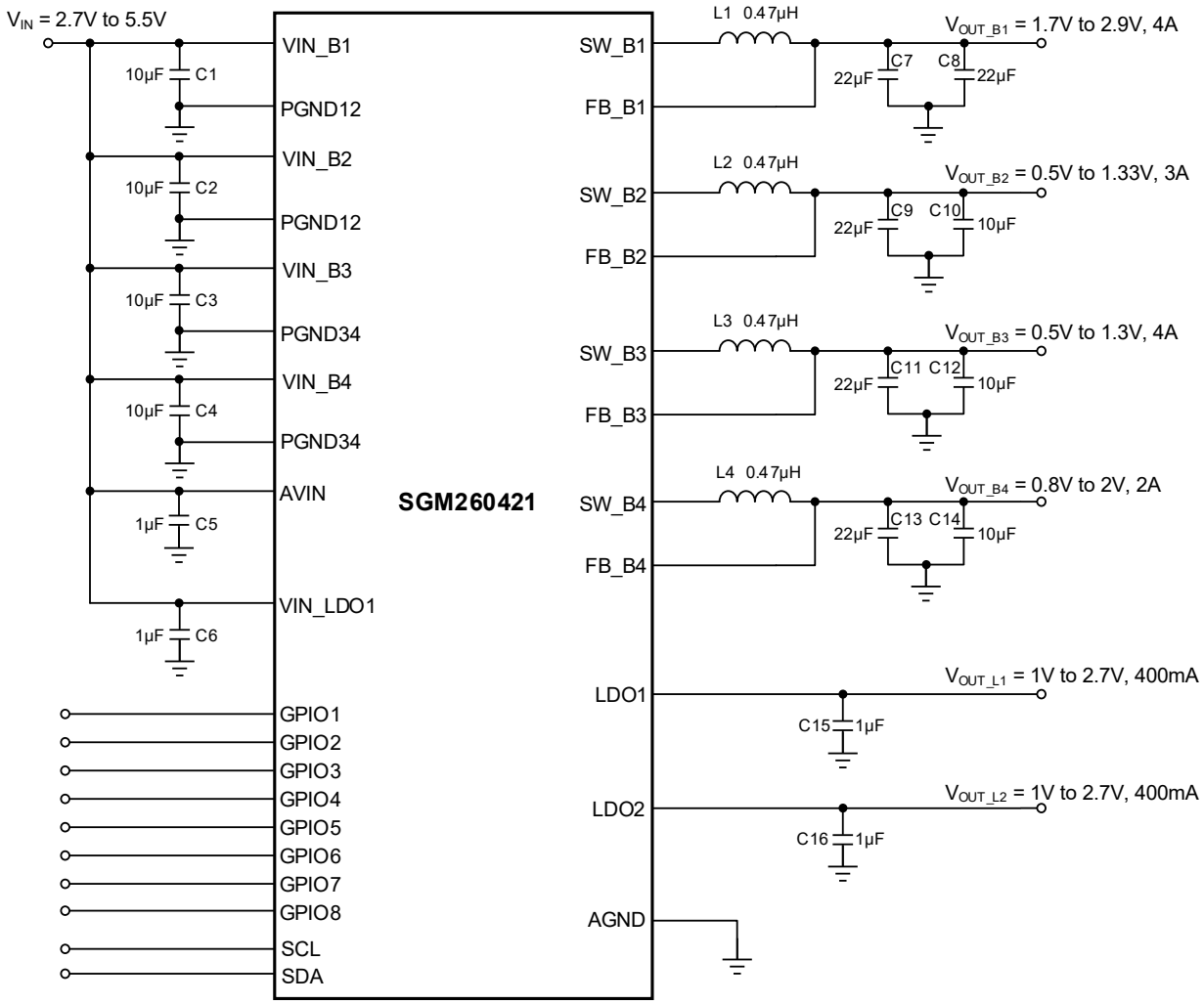


Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

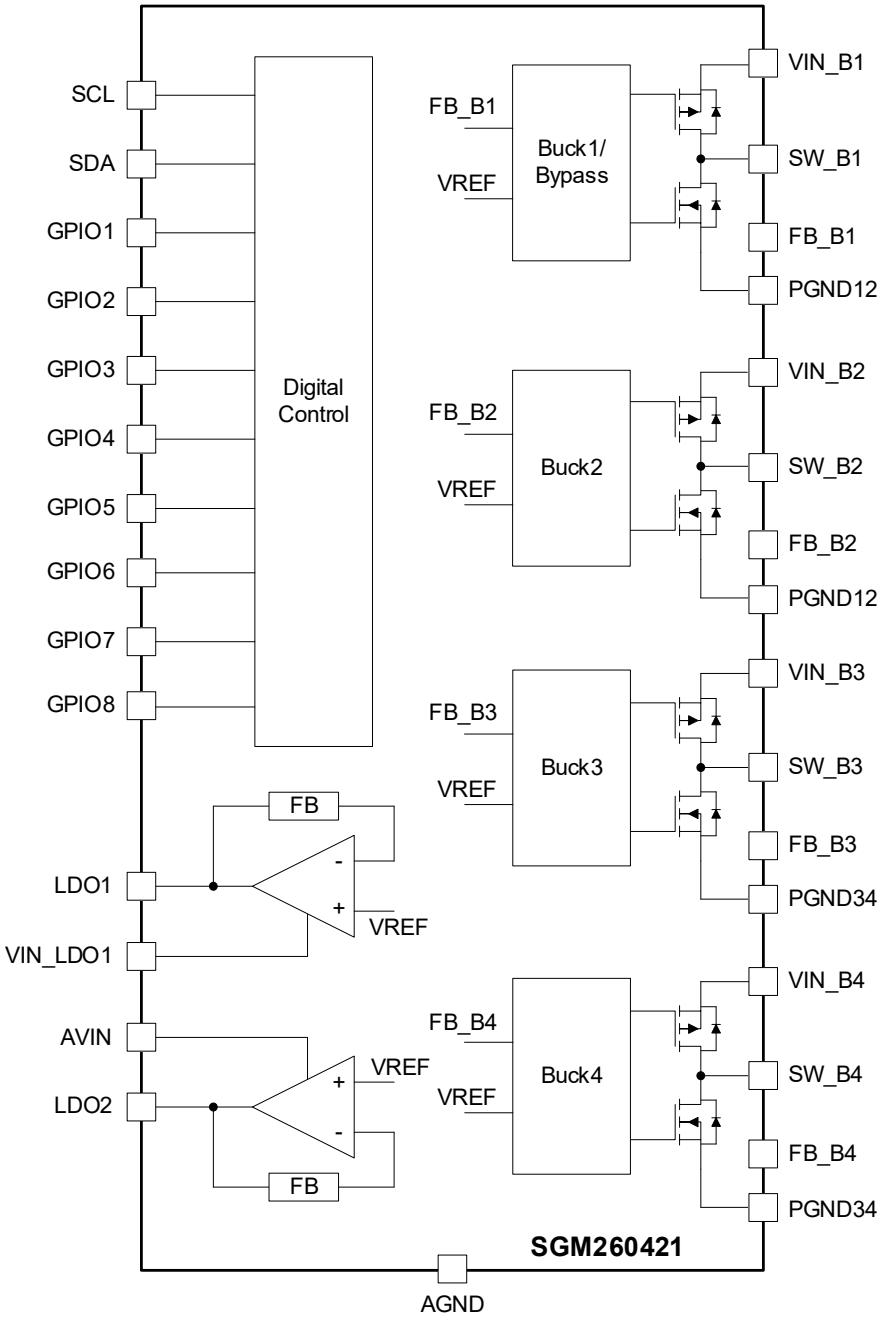


Figure 3. Block Diagram

DETAILED DESCRIPTION: SYSTEM CONTROL

General

The SGM260421 represents an integrated power management IC engineered for next-generation solid-state drive controllers. This system-on-chip solution is equipped with four high efficiency Buck converters and two LDOs, and has been specifically optimized for mission-critical storage controllers and industrial automation processors. This device achieves space-saving and cost-effective power delivery through advanced integration. SGM260421 contains a master controller governing critical operations: startup sequencing, turn-on delay, extra delay, turn-off delay, wake-up delay, voltage of each channel, soft-start time, SLEEP or DPSLP state, and fault conditions.

System parameters can be dynamically adjusted through I^2C interface, without physical hardware modifications. A built-in bypass switch for Buck1 enhances sequencing flexibility in 3.3V power architectures.

The master controller continuously tracks all output channels, transmitting status information through I^2C protocol communication and hardware-level status signals. User can configure fault thresholds and response mechanisms via I^2C interface, including selective fault masking capabilities.

Factory-defined parameters for SGM260421 are established through Code Matrix Index (CMI). The device supports extensive customization for different GPIO configurations as well as voltage and current limit for each channel, etc. It is specifically defined for each SGM260421 CMI part number.

I^2C Serial Interface

Standard I^2C interface is used to program SGM260421 parameters and get status reports. It operates as a slave device, and can be configured by factory to one of four 7-bit slave addresses. The base address incorporates an extension bit which defining the operation is read or write.

The I^2C controller does not have a timeout feature. However, whenever it detects a new start signal, it will immediately stop and reset the current data processing, even if a valid data packet is being transmitted.

I^2C is 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The SDA pin operates in open-drain configuration and requires an external pull-up resistor.

Table 1. SGM260421 I^2C Addresses

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25	0100101	0x4A	0x4B
0x27	0100111	0x4E	0x4F
0x67	1100111	0xCE	0xCF
0x6B	1101011	0xD6	0xD7

I^2C Registers

The SGM260421 integrates internal configuration registers that store critical operational parameters, including output voltage setting, switching frequency, startup sequencing, fault detection thresholds, fault mask configurations, etc. These registers provide the core programmability of the device. Two register categories are implemented.

Basic Volatile

These registers are R/W (read/write) and R (read only). After power-up, user can modify R/W registers to adjust IC functions, such as masking faults. R registers display IC status, including faults. All changes are lost on power cycle. Default values are fixed and cannot be altered by the factory or user.

Basic Non-Volatile

These registers are R/W and R types. Once the IC is powered up, user can change the R/W registers to adjust functions like output voltage, startup delay, and current limit thresholds. These modifications are lost when power is cycled. The default values can be set at the factory to optimize the IC for specific applications. Please contact SGMICRO for custom options and minimum order quantities. When updating only certain bits within a register, be careful not to alter the other bits, as doing so may cause unexpected device behavior.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

State Machine

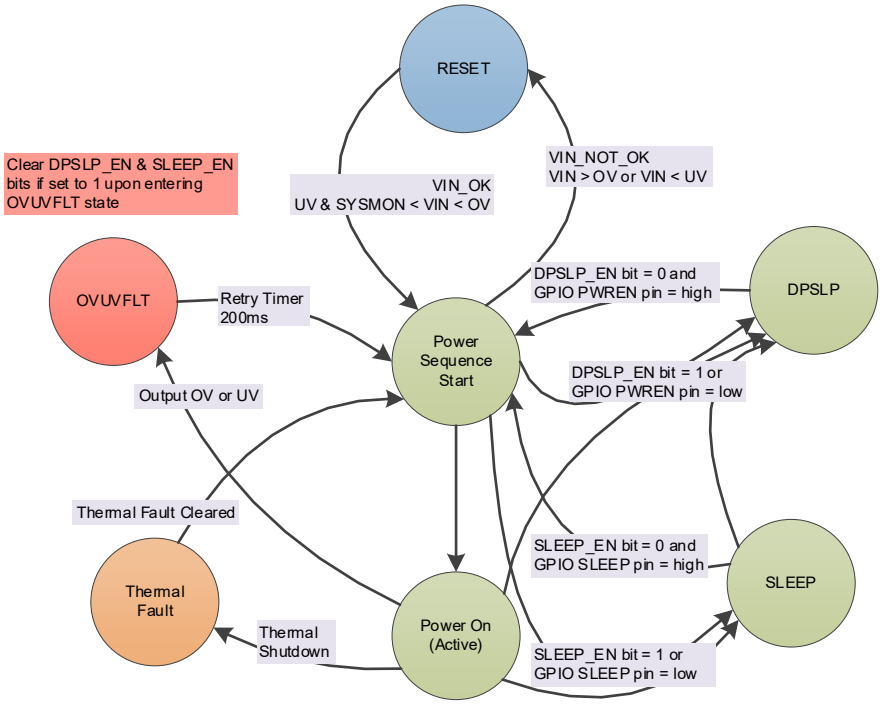


Figure 4. State Machine

RESET State

During the RESET state, the SGM260421 monitors AVIN until it stabilizes within the acceptable range specified by VIN_UV, SYSMON and VIN_OV. In this state, all regulators remain off and the outputs are maintained at a low level. When the input voltage drops below the VIN_UV threshold or exceed the VIN_OV limit, the IC will revert to the RESET state regardless of its current operating state.

Power Sequence Start State

During the power sequence start state, the system is in a transitional phase as the regulators begin their activation. During this period, outputs are activated and start their ramp-up. As soon as the regulators stabilize and enter regulation, the IC promptly shifts to the active, SLEEP or DPSLP state.

Power On (Active) State

The active state represents normal operation, where the input voltage remains within the acceptable range, all outputs are enabled, and no faults are detected.

SLEEP State

The SLEEP state represents a configurable low-power state. In SLEEP state, each output of SGM260421 can be configured to remain on/off. Buck2 and Buck3 can be configured to regulate at their respective DVS_VSET voltages. When transiting into/out of SLEEP mode, the outputs follow their programmed sequencing delay time for turning on/off. When SGM260421 transitions into SLEEP mode, it disables some internal circuits to activate a low-power mode (LPM), thereby reducing the VIN supply current for power saving.

The IC supports entry into SLEEP state through two methods: setting the SLEEP_EN bit in the I^2C register, or pulling low GPIO input.

1. When a GPIOx configured for the SLEEP function transitions from high voltage level to low voltage level, the IC enters the SLEEP state.
2. Apart from external hardware-based SLEEP state control, the IC is also capable of entering the SLEEP state via the I^2C interface, when the SLEEP_EN bit is set to 1, the PMIC switches to the SLEEP state.

Exit from SLEEP state occurs when both the I^2C SLEEP_EN bit and GPIO are de-asserted. In the absence of a GPIO configured to manage SLEEP state, only the SLEEP_EN bit dictates access (entry and exit) to this state.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

DPSLP State

The DPSLP state is designed for even lower power consumption than the SLEEP mode. Each output can be individually set to be on/off in DPSLP mode, with setting that may differ from those in the SLEEP state. Buck2 and Buck3 can also be configured to regulate at their respective DVS_VSET voltages. When transitioning into/out of DPSLP mode, the outputs follow their programmed sequencing delay time for turning on/off. When SGM260421 transitions into DPSLP mode, it also disables some internal circuits to activate LPM, thereby reducing the VIN supply current for power saving.

The IC supports entry into DPSLP state through two methods: setting the DPSLP_EN bit in the I^2C register, or pulling low GPIO input.

1. When a GPIOx configured for the PWREN function transitions from high voltage level to low voltage level, the IC enters the DPSLP State.
2. Apart from external hardware-based DPSLP state control, the IC is also capable of entering the DPSLP state via the I^2C interface; when the DPSLP_EN bit is set to 1, the PMIC switches to the DPSLP state.

Exit from DPSLP state occurs when both the I^2C DPSLP_EN bit and GPIO are de-asserted. In the absence of a GPIO configured to manage DPSLP state, only the DPSLP_EN bit dictates access (entry and exit) to this state.

THERMAL State

If the IC temperature rises above +155℃, it enters the THERMAL state, turning off all regulators and asserting nRESET for protection. The PMIC exits this state and reverts to startup sequence only when the die temperature drops below +125℃.

OVUVFLT State

When the output voltage of any regulator goes above the over-voltage (OV) threshold or below the under-voltage (UV) threshold after soft-start, the IC enters OVUVFLT state. All regulators turn off, and the nRESET is pulled low. The system tries to restart after a 200ms delay. If the OV/UV condition remains, the IC returns to OVUVFLT state, repeating this cycle until the fault is removed or input power is disconnected. While over-current conditions do not directly trigger OVUVFLT state, sustained over-current causing UV conditions will lead to PMIC enter OVUVFLT state.

Sequencing

The SGM260421 delivers advanced sequencing control for multi-rail power systems. Each of its six outputs has five basic programmable parameters: turn-on delay, turn-off delay, wake-up delay, soft-start time, and output voltage. All parameters are programmed through dedicated configuration registers, enabling application specific optimization without hardware changes.

Turn-On Delay

Defined as the duration between SYS_OK (indicating OTP register initialization and GPIO status detection are complete) and the start of output activation, the turn-on delay for each output is programmed using its I^2C ON_DLY bit. It can be changed after IC powers up, these delays are volatile and revert to factory settings when power is recycled. In addition to the turn-on delay, each channel can also add an extra delay based on the status of GPIO3 during startup. This means that the actual startup delay is composed of a turn-on delay and an extra delay.

Turn-Off Delay

The turn-off delay is measured as the time between the assertion of SLEEP/DPSLP mode and the start of output turn-off, and it also applies when the PMIC is disabled via PWRDIS or VIN shutdown. The delay of each output is programmed using its I^2C OFF_DLY bit. These delays can be changed after power on, but are volatile, returning to factory defaults upon power recycling.

Wake-Up Delay

The enable delay time for a regulator exiting SLEEP or DPSLP mode is set by this wake-up delay timer. It is measured from the rising edge of the SLEEP/DPSLP signal until the regulator turns on.

Table 2. The Delay Time Contributions to the Sequence

Sequence	ON_DLY	Extra_ DLY	OFF_DLY	WAKE_ UP_DLY
Power-Up	Yes	Yes	-	-
Power-Off	-	-	Yes	-
Shutdown PMIC by PWRDIS = H	-	-	Yes	-
Startup PMIC by PWRDIS = L	Yes	Yes	-	-
Enter SLEEP/DPSLP	-	-	Yes	-
Exit SLEEP/DPSLP	-	-	-	Yes

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

Soft-Start Time

Defined as the time it takes an output ramp from 10% to 90% of its target voltage, the soft-start time for each output is programmed using dedicated I^2C soft-start bits. These settings can be adjusted after power-up but are volatile, resetting to factory values when power is cycled.

Output Voltage

Output voltages for Bucks are programmed via respective I^2C bits (Bx_VSETx). During active mode, Buck2 regulates to B2_VSET0/1 as determined by GPIO2 configuration, and in SLEEP/DPSLP state, it can be set to B2_DVS_VSET through either the I^2C interface or a GPIO input. Likewise, Buck3 regulates to B3_VSET0/1/2 in active mode (based on GPIO1/3 settings) and supports programming to B3_DVS_VSET0/1/2 in SLEEP/DPSLP state via I^2C or GPIO input.

The Bx_VSETx voltage of each output can be modified via I^2C after the IC powers up, but such settings are volatile and reset to factory defaults upon power recycling. All Bucks and LDOs output voltages are also adjustable on-the-fly by updating their I^2C registers with new values.

Dynamic Voltage Scaling

Dynamic voltage scaling (DVS) for Buck2 and Buck3 is available. DVS enables systems to save power by rapidly adjusting micro-processor performance in response to load change.

The IC is configurable to transition into DVS upon entering SLEEP or DPSLP mode.

With B2/3_DVS_AT_SLEEP bit = 1, any condition that puts the IC into SLEEP state puts the Buck2/3 into DVS mode. With B2/3_DVS_AT_DPSLP bit = 1, any condition that puts the IC into DPSLP state also puts the Buck2/3 into DVS mode.

Similar to any power supply, changing an output voltage too quickly can demand a current beyond the current limit threshold. It is critical for users to verify that voltage step, slew rate, and load current parameters avoid creating an instantaneous load current that results in current limit condition.

SYSMON, SYSWARN and POK_OV

SGM260421 monitoring the input voltage (AVIN) to ensure compliance with system-level operational limits, the outputs disabled until AVIN exceeds the SYSMON rising threshold. This threshold is programmable between 2.725V and 3.1V, with a step of 25mV. Additionally, if AVIN falls below the SYSMON falling threshold, outputs persist in normal operation as long as AVIN stays above UVLO falling threshold.

SYSWARN is a warning signal, it triggers when the AVIN voltage falls below its monitored SYSWARN falling threshold. The SYSWARN rising threshold is configurable between 2.775V and 3.15V, with a step of 25mV.

A GPIO pin can be assigned to the SYSMON/SYSWARN output signals, both of which are real-time. Figure 5 shows the details (note: VIN_LVL bit = 0).

POK_OV is a warning indicator that alerts when the AVIN voltage exceeds the voltage it monitors. Additionally, the system can track the power good status of AVIN (the input source) using the two signals, SYSWARN and POK_OV.

Offering real-time reactions, the indicator bits for SYSMON, SYSWARN, and POK_OV reflect AVIN status dynamically. The POK_OV bit set to 1 means AVIN exceeds its monitoring voltage, so keep this bit at 0 to ensure AVIN stays in the correct operational range. Conversely, SYSMON and SYSWARN bits become 0 when AVIN is below their configured thresholds, maintain them at 1 for normal operation.

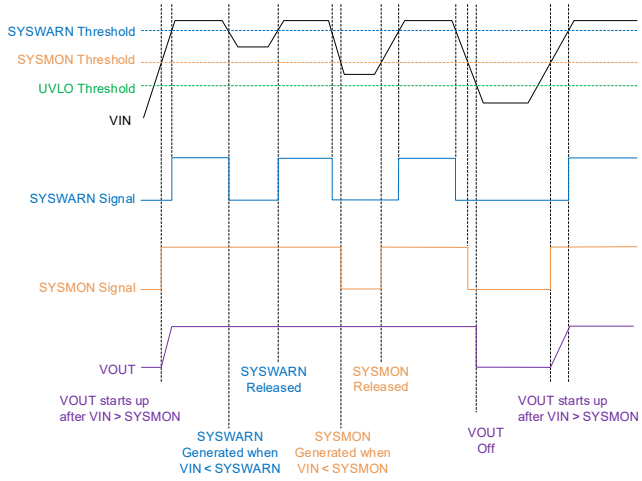


Figure 5. SYSMON and SYSWARN Signals

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

AVIN UVLO and AVIN OV

The input voltage at the AVIN pin is monitored by the SGM260421 for UVLO conditions. Upon the voltage dropping below the UVLO threshold, the IC is in the RESET state, with all outputs disabled and nRESET asserted low. The UVLO falling threshold can be set to either 2.5V or 3.5V via the factory-programmable VIN_LVL bit.

Operation of the PMIC begins when the AVIN voltage is over the SYSMON threshold. SYSWARN and POK_OV can be used to monitor the AVIN. A fault status is generated and sent through the nIRQ signal to alert the system if AVIN falls below SYSWARN (even below SYSMON) or exceeds POK_OV, though the PMIC remains operational in warning status. The PMIC is forced to shut down only if AVIN further getting worse to below the UVLO falling threshold or above the OV rising threshold.

Output Under/Over-Voltage

SGM260421 monitors output voltages for UV/OV conditions. When an output entering a UV/OV fault condition, the IC enters the OVUVFLT state (turning off all outputs for 200ms), then moves to the power start sequence state to restart using the programmed power-up sequence. Trigger current limit may also cause a shutdown if their voltage drops below the UV threshold.

The Lx_OVP_EN bit controls the LDO output over-voltage (OV) function. With Lx_OVP_EN set to 0, the IC is prevented from entering the OVUVFLT state when LDO OV fault occurs. Under this condition, the LDO output voltage is discharged when it exceeds 115% of the reference voltage and stops discharging once it falls below 107% if EN_DISCHG_Lx_OVP being set to 1.

UV threshold:

For Bucks, the output voltage drops below 89.5% of the reference.

For LDOs, the output voltage drops below 82% of the reference.

OV threshold:

For Bucks, the output voltage exceeds 110% of the reference.

For LDOs, the output voltage exceeds 115% of the reference.

Output Current Limit

Buck converters provide over-current limit protection by detecting the low-side MOSFET current (inductor valley current). If the valley current is above the configured current limit, the low-side MOSFET is kept on to pull the inductor current down. Once the valley current is lower than the current limit, the control loop changes from the over-current (OC) loop to the normal loop. Four over-current levels are applied to each Buck converter in the SGM260421, refer to register tables for more details.

For LDOs, over-current thresholds are determined by the Output Current Limit setting of each LDO. When the output current reaches this threshold, the LDO limits its output current.

Thermal Warning and Thermal Shutdown

The SGM260421 continuously monitors its internal die temperature. It issues a warning via the nIRQ signal when the temperature exceeds the thermal interrupt threshold (typically +125℃) and generates a fault report when it rises above the thermal shutdown temperature (typically +155℃). A temperature fault transitions the state machine into the thermal fault state and turn off all outputs.

Status and Flag

The AVIN status, OT, nRESET, and nIRQ monitored in the TOP_STATUS_REG, along with the outputs' POK status monitored in the RAIL_STATUS_REG, are all real-time signals. These signals are designed as level-triggered.

Output UV, OV, and current limit events are recorded by the flags in the RAIL_FLAG_REGx, which are designed as edge-triggered signals. A fault triggers the related bit to latch the fault status even the fault is removed. Read the bit to clear when the fault condition is removed.

The TOP_STATUS_REG, RAIL_STATUS_REG, and RAIL_FLAG_REGx form the fault code system, which records what happen in the present. When there is a problem with the power system of an SSD application, reading these register values will help users quickly understand what has happened.

GPIO CONFIGURATION

General Description

SGM260421 has 8 configurable GPIOs. Four of these (GPIO1/2/3/4) are designed for 3-state inputs (high, float, low), whereas the others support only 2-state inputs. GPIO1 can be set as nRESET or Buck3 voltage select function. With the exception of GPIO1, all GPIOs can be configured to implement various functions, including nIRQ, SYSMON, SYSWARN, EXT_EN, I^2C controlled output, PG of internal rail, SLEEP/PWREN, PWRDIS, EN of internal rail. In addition to above features, GPIO2/3/4/6 can also be configured for additional functions, including an operation mode, a default output voltage, and an extra power-up delay time selector.

nRESET

The nRESET signal monitors the input voltage and regulator output validity to trigger a reset when either the input voltage or regulator outputs are abnormal. The nRESET output signal is typically connected to both the input voltage and the power good (PG) signals of enabled regulators to ensure proper operation. Only GPIO1 can be set as nRESET. Below events can assert nRESET low:

- Input Voltage Power Bad: Input OV or UV
- Thermal Shutdown
- PMIC Disabled by PWRDIS
- Enabled Rails' Output Power Bad: Output OV or UV

After the power-up sequence, the input voltage and regulator outputs being power good (PG) is indicated by nRESET = H, while power bad (PBAD) is indicated by nRESET = L.

The nRESET_MASK_REG provides the function of masking any output PBAD, VIN_OV, and OT events. By setting the corresponding bits to 1, nRESET is configured to ignore PBAD events on masked rails. Any PBAD event on an unmasked rail will cause nRESET to assert low. In addition, the power good delay time, measured from the rising edge of Buck3 PG to that of nRESET, can be programmed in the nRST_DLY bits.

The nRESET signal is isolated from disabled regulators: even if a PG signal of regulator is unmasked, the disabled regulator cannot affect nRESET. This isolation avoids nRESET triggering when the regulator is shut down by user command. In SLEEP/DPSLP status, nRESET remains asserted high, even with some rails are turned off.

nIRQ

GPIO2~8 can be configured to nIRQ ouput. Integrated into the fault code system, the nIRQ system records all faults in dedicated internal registers and selects which faults to export through nIRQ_MASK_REG.

The SGM260421 contains several faults protection that can assert nIRQ:

- Input POK_OV
- Input OV
- Input Voltage Drops below SYSMON
- Input Voltage Drops below SYSWARN
- Output OV/UV
- Thermal Warning
- Thermal Shutdown

The nIRQ system contains two registers, nIRQ_FLAG_REG (REG0x05) and nIRQ_MASK_REG (REG0x06), where nIRQ_FLAG_REG records fault flags, which is latched bits that remain asserted until read via I^2C and the fault is removed.

The nIRQ_MASK_REG controls whether the fault flags in the nIRQ_FLAG_REG are blocked or allowed to affect the nIRQ output (active-low). If a fault is recorded but masked by the nIRQ system, the nIRQ output ignores the recorded fault, if the fault is recorded and unmasked, the GPIO configured as nIRQ asserts a low-level signal. The nIRQ only de-asserts after two events: the fault condition is no longer present, and the corresponding fault bit in the nIRQ_FLAG_REG is read via I^2C.

SYSMON

GPIO2~8 can be configured to output active-low SYSMON signals for host system monitoring. It gets low when AVIN < SYSMON falling threshold, and it gets high when AVIN > SYSMON rising threshold. It is a real-time signal.

SYSWARN

GPIO2~8 can be configured to output active-low SYSWARN signals for host system monitoring. It gets low when AVIN < SYSWARN falling threshold, and it gets high when AVIN > SYSWARN rising threshold. It is a real-time signal.

GPIO CONFIGURATION (continued)

EXT_EN

GPIO2~8 can be configured to EXT_EN. The EXT_EN is a GPIO output function for enabling external power supplies, facilitating their integration into the system-level startup sequence. The EXT_EN output is activated by one of the internal PG signals, SYSMON and GPIOs, which can be programmed to have a delay time via the EXT_EN_ON_DLY/EXT_EN_OFF_DLY bit.

The EXT_EN signal asserts low when the SGM260421 initiates a power-down sequence due to protection events (e.g., VIN OV, OT, PWRDIS = H, or output rails experiencing OV/UV faults). Additionally, the EXT_EN can be configured to enable or disable in SLEEP/DPSLP mode via an I^2C register.

I^2C Controlled Output

GPIO2~8 can be configured as I^2C-controlled outputs, where a register bit defines the output state as either high or low.

PG of Internal Rails

GPIO2~8 can be configured as the PG of the internal rail. The internal PG (power good) bit of a regulator can be connected to a GPIO. This PG function indicates that the regulator output voltage is maintained within regulation.

SLEEP/PWREN

GPIO2~8 can be configured as SLEEP/PWREN inputs. These digital input signals determine whether the IC operates in power on mode or SLEEP/DPSLP mode. For details, refer to the SLEEP/DPSLP state section.

The SLEEP/DPSLP state is entered by pulling SLEEP/PWREN low, during which Buck2 and Buck3 can be configured to remain turn on, DVS mode or shutdown. Buck1/4 and the LDOs can be configured to remain turn-on or shutdown.

PWRDIS

GPIO2~8 can be configured as PWRDIS. Upon the PWRDIS signal going high, the PMIC enter the power-off sequence.

EN of Internal Rail

GPIO2~8 can be configured as EN of internal rail. Which allowing user to control the internal rail on/off. For system-level integration, the PG signal of external rail may be connected to these GPIOs to incorporate external power supplies into the startup sequence.

GPIO1

GPIO1 can be configured as nRESET signal or Buck3 voltage select. If GPIO1 is configured to Buck3 voltage select function, once AVIN is valid, the GPIO1 status is checked and latched immediately. Please see Table 3 for the description of GPIO1 additional configurable function.

Table 3. GPIO1 Additional Configurable Function

GPIO1 Status	High	Float	Low
Buck3 Output	VSET0	VSET1	VSET2
Buck3 Output in SLEEP/DPSLP	DVS_VSET0	DVS_VSET1	DVS_VSET2

GPIO2

GPIO2 has an additional configurable function, Buck1/Buck2 operation mode and voltage select. If GPIO2 is configured to this function, once AVIN is valid, the GPIO2 status is checked and latched immediately. When GPIO2 is not set as Buck1/Buck2 operation mode and voltage select at factory. Buck1 works in Buck mode and output voltage is set by B1_VSET0, and Buck2 output voltage is set by B2_VSET0. Please see Table 4 for the description of GPIO2 additional configurable function.

Table 4. GPIO2 Additional Configurable Function

GPIO2 Status	High	Float	Low
Buck1 Output	LSW	VSET0	VSET1
Buck2 Output	VSET0	VSET0	VSET1

GPIO CONFIGURATION (continued)

GPIO3

GPIO3 has an additional configurable function, B3 voltage select and all the rails extra power-up delay time and Buck1/Buck2 wake-up delay. If GPIO3 is configured to this function, once AVIN is valid, the GPIO3 status is checked and latched immediately. Please see Table 5 for the description of GPIO3 additional configurable function. The extra delay time in Table 5 is the default CMI 001 configuration. This extra delay time doesn't affect wake-up delay time. For other delay time configuration, please contact SGMICRO.

If both GPIO1 and GPIO3 are configured to Buck3 voltage select function, Buck3 voltage is determined by GPIO1 status, and GPIO3 only selects the extra delay time of Buck3. Otherwise, if neither GPIO1 nor GPIO3 is configured to Buck3 voltage select function at factory, Buck3 voltage is determined by B3_VSET0 or B3_DVS_VSET0. Besides, extra power-up delay time and wake-up delay follow the set of the float column in Table 5, when GPIO3 is not configured as this function.

Table 5. GPIO3 Additional Configurable Function

GPIO3 Status		High	Float	Low
Buck3 Output		VSET0	VSET1	VSET2
Buck3 Output in SLEEP/DPSLP		DVS_VSET0	DVS_VSET1	DVS_VSET2
Buck1 Wake-Up Delay		2ms	1ms	1ms
Buck2 Wake-Up Delay		1ms	2ms	2ms
Extra Power-Up Delay Time	Buck1	+1ms	+0ms	+0ms
	Buck2	+0ms	+1ms	+1ms
	Buck3	+0ms	+0ms	+0ms
	Buck4	+0ms	+0ms	+0ms
	L1	+0ms	+0ms	+0ms
	L2	+0ms	+0ms	+0ms

GPIO4

GPIO4 has an additional configurable function, B4/L1 operation mode and voltage select. If GPIO4 is configured to this function, once AVIN is valid, the GPIO4 status is checked and latched immediately. Please see Table 6 for the description of GPIO4 additional configurable function. When GPIO4 is not set as B4/L1 operation mode and voltage select at factory, the output voltage is set by the VSET0 register, and the Buck or LDO operation is set by B4_MODE register at factory. Likewise，LDO1 V_{OUT} is set by VSET0, LDO1 mode is set by L1_MODE bit at factory.

Table 6. GPIO4 Additional Configurable Function

GPIO4 Status	High	Float	Low
Buck4 Output	Buck: VSET0	B4_MODE_AT_GPIO4_F = 0 Buck: VSET2	Buck: VSET1
		B4_MODE_AT_GPIO4_F = 1 LDO: VSET2	
LDO1 Output	VSET0	L1_MODE_AT_GPIO4_F = 0 LDO: VSET0	L1_MODE_AT_GPIO4_L = 0 LDO: VSET1
		L1_MODE_AT_GPIO4_F = 1 LSW	L1_MODE_AT_GPIO4_L = 1 LSW

GPIO6

GPIO6 has an additional configurable function, L2 operation mode. If GPIO6 is configured to this function, once AVIN is valid, the GPIO6 status is checked and latched immediately. Please see Table 7 for the description of GPIO6 additional configurable function. When GPIO6 is not set as L2 operation mode select at factory, the LDO or LSW operation is set by L2_MODE bit at factory.

Table 7. GPIO6 Additional Configurable Function

GPIO6 Status	High	Low
LDO2 Output	VSET	LSW

STEP-DOWN DC/DC CONVERTERS

General Description

The SGM260421 integrates four Buck converters. All Bucks are ACOT mode controlled. These Buck converters feature internal compensation, requiring only three small external components (C_{IN}, C_{OUT}, and L) for operation.

Each Buck converter has its own dedicated input pin and power ground pin. To ensure optimal performance, each converter requires a dedicated input capacitor placed strategically to minimize power routing loops. Although the Buck converters have separate input pins, all inputs must be tied to the same voltage potential.

The SGM260421 Buck regulators offer extensive configurability and can be easily adjusted via I^2C, eliminating the need for PCB modifications when hardware requirements change. The following I^2C controlled functions are available:

- Real-Time Monitoring of Power Good, Over-Voltage (OV), Under-Voltage and Current Limit
- Selective Fault Masking
- Dynamic Output Voltage Adjustment
- On/Off Control
- Soft-Start Ramp Configuration
- Power Save Mode
- Over-Current Thresholds Adjustment

Operating Mode

Buck1/2/3/4 use adaptive constant on time (ACOT) control. By default, all Buck converters operate in fixed-frequency PWM mode under medium to heavy loads. At light loads, it automatically transitions to a proprietary power-saving mode that reduces conduction losses by preventing negative inductor current. All the Bucks can switch to FPWM mode, PSM mode or LPM mode through I^2C interface.

Buck1 can be configured as a bypass switch for systems with a 3.3V bus. And Buck4 can be configured to LDO mode.

Buck LPM

To optimize efficiency under extremely light loads, each regulator features a low-power mode (LPM). Enabled by setting the EN_LPM bit to 1, LPM significantly reduces power loss in this condition. After entering SLEEP/DPSLP mode, the system automatically enters LPM mode. LPM only supports extremely light load applications. It is only recommended to use LPM mode in SSD applications.

Enable/Disable Control

During normal operation, each Buck converter can be enabled or disabled via the I^2C interface by writing to the Bx_EN bit. Each Buck converter includes a load discharge function that rapidly pulls the output voltage to ground when the converter is disabled. The Bucks discharge resistor is adjustable via I^2C.

Soft-Start

Each Buck regulator feature built-in soft-start ramps to control the output voltage rise, reducing input inrush current and ensuring a smooth, monotonic startup regardless of load conditions. This mechanism is activated after the regulator is enabled and recovered from short-circuit or other fault. The soft-start duration can be adjusted via the Bx_SS bit.

Dynamic Voltage Scaling

Buck2 and Buck3 support dynamic voltage scaling (DVS). When the SGM260421 enters SLEEP or DPSLP modes, these Bucks (if kept active) can automatically switch their output voltage to the pre-configured DVS_VSET level. The slew rate of this transition between VSET and DVS_VSET is programmed via the I^2C bits Bx_DVS_SET.

Separately, the output voltage of Buck1 and Buck4 can be updated dynamically through their I^2C VSET registers, with the transition likewise being slew rate controlled.

Over-Current and Short-Circuit Protection

Each Buck converter includes over-current and short-circuit protections. Over-current protection is implemented using cycle-by-cycle current limit. The valley current threshold are set by the Bx_ILIM_SET bits.

Buck regulate the maximum valley current of the low-side FET by preventing the high-side FET from turning on until the low-side FET current falls below the valley current limit.

If an output enters current limit, its voltage may drop below the UV threshold which shuts down all outputs and enter the OVUVFLT state. If V_{OUT} is short to GND, the current is likewise limited. This action typically induces an immediate UV condition, prompting the IC to enter the OVUVFLT state.

STEP-DOWN DC/DC CONVERTERS (continued)

Buck1 Bypass Switch

Buck1 can be configured as a bypass switch for systems with a 3.3V bus. In bypass mode, the Buck1 PMOS functions as a switch, while the NMOS remains disabled. The bypass switch activates the 3.3V rail with the programmed delay.

In bypass mode, neither a short to ground nor an overload at VOUT will trigger an under-voltage (UV) fault. This is because the switch shuts down rapidly to protect the PMIC, leaving insufficient time for the UV condition to be registered.

Note that in this mode, the over-voltage protection (OV) threshold is set to 3.8V with a 20μs deglitch time. If OV occurs, SGM260421 shuts down all outputs, enters OVUVFLT state, retries after 200ms.

Buck4 LDO Operation

Buck4 integrates a 400mA LDO. The operating mode (Buck or LDO) is selectable via GPIO4 or B4_MODE = 1 at factory (when GPIO4 is not set as B4/L1 operation mode and voltage select). When configured for LDO operation by floating GPIO4, the output voltage is set by the VSET2 register. When configured for LDO operation by B4_MODE = 1 (fixed at factory, change this bit via I^2C has no reaction), the output voltage is set by the VSET0 register. The external inductor must be removed in LDO mode operation.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. 10μF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. The input voltage ripple is calculated using the following Equation:

$$V_{RIPPLE} = I_{OUT} \times \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times C_{IN}}$$

Consider the capacitor's DC bias effects and maximum ripple current rating when using sizes smaller than 0805, as DC bias significantly impacts actual capacitance. The input capacitor is typically X5R, X7R, or a similar dielectric. Proper placement is critical. Each input capacitor of Bucks must be positioned as close to the IC as possible. The traces from V_{IN_Bx} to the capacitor and from the capacitor to PGNDx should be as short and wide as possible.

Inductor Selection

The Buck converters use ACOT control with a proprietary internal compensation scheme that simplifies external component selection and optimizes transient performance across the full operating range. The SGM260421 is designed for 0.47μH inductors. Select an inductor with low DC resistance and a DC rating at least 30% higher than the maximum output current to prevent saturation. The inductor ripple current is calculated using the following equation:

$$\Delta I_L = I_{OUT} \times \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times V_{OUT}}{f_{SW} \times L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The SGM260421 is optimized for compact, low-ESR ceramic output capacitors. Ensure the output ripple voltage remains below 1% of the output voltage. The equation below defines the relationship between output voltage ripple and output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

Where ΔI_L is the inductor ripple current, f_{SW} is the switching frequency, and C_{OUT} is the effective output capacitance, considering DC bias effects. When using capacitors smaller than 0805, ensure they meet the required ripple current rating and account for capacitance reduction due to DC bias. The actual capacitance can vary significantly based on voltage conditions. Typically, X5R, X7R, or similar dielectric capacitors are recommended for the output stage.

LDO CONVERTERS

General Description

The SGM260421 integrates two 400mA low dropout (LDO) regulators, optimized for minimal dropout voltage. They can also operate in load switch mode. Each LDO requires only two small external capacitors (C_{IN} and C_{OUT}) for proper function. The default output voltages are factory-set but can be adjusted via the I^2C interface for advanced power management needs.

LDO1 is powered through its own dedicated pin, VIN_LDO1, allowing it to operate from an input voltage source independent of those for the Buck converters and LDO2. In contrast, LDO2 is powered directly from the AVIN pin.

Enable/Disable Control

During normal operation, each LDO can be enabled or disabled through the I^2C interface by setting the Lx_EN bit or through GPIO. Each LDO includes a load discharge function that rapidly pulls the output voltage to ground when the LDO is disabled.

Soft-Start

Each LDO includes a soft-start circuit that controls the output voltage ramp, reducing input inrush current and ensuring monotonic start-up. This function is active whenever the LDO is enabled and after recovery from a short-circuit or other fault conditions. The soft-start time of each LDO is adjustable via I^2C.

Over-Current and Short-Circuit Protections

Each LDO features over-current detection and short-circuit protection. Upon reaching the current limit, the IC keeps the over-current threshold level until the over-current condition is removed.

During overload or short-circuit conditions, the LDO limits the output current, causing the output voltage to drop. Once current limiting causes the output voltage to drop and trigger an under-voltage (UV) condition, the IC shuts down all power supplies and enters the OVUVFLT state. Then it will automatically restart after a 200ms delay, following the default power-up sequence.

Low-Power Mode

LDO1 and LDO2 feature a low-power mode (LPM) that minimizes their standby current. Note that in LPM, certain protections such as over-voltage (OV) and current limit (ILIM) are disabled. After entering SLEEP/DPSLP mode, the system automatically enters LPM mode. LPM only supports extremely light load applications. It is only recommended to use LPM mode in SSD applications.

Input Capacitor Selection

Each LDO requires a high-quality, low-ESR ceramic capacitor. A 1μF capacitor is typically sufficient, but a larger value can be used without restriction. The input capacitor should have an X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high-quality, low-ESR ceramic output capacitor, a 1μF is a typical choice. The capacitor should have an X5R, X7R, or similar dielectric.

Load Switch Mode

LDO1 and LDO2 can be configured as a PMOS load switch (LSW mode). In this mode, the LDO1 operates with an input voltage ranging from 1.62V to AVIN. The load switch current limit (LSW) is set to either 0.4A or 0.5A via the LDOx_ILIM_SET I^2C bit.

Over-voltage protection in LSW mode has a 3.8V threshold with 20μs deglitch. If an OV (if Lx_OVP_EN = 1) or UV condition is detected, the SGM260421 shuts down all outputs, enters the OVUVFLT state, and initiates an auto-retry after 200ms.

I²C COMPATIBLE INTERFACE

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM260421 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM260421 operates as a slave device that address (adjustable) is 0x25. It has fifty 8-bit registers, numbered from 0x00 to 0x52.

Physical Layer

The standard I²C interface of SGM260421 supports standard mode, fast mode, fast mode plus and high-speed mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the high-speed mode is up to 3.4Mbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown Figure 6. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

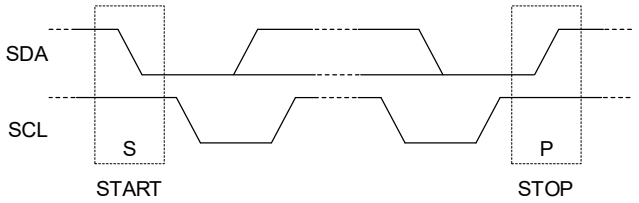


Figure 6. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 7.

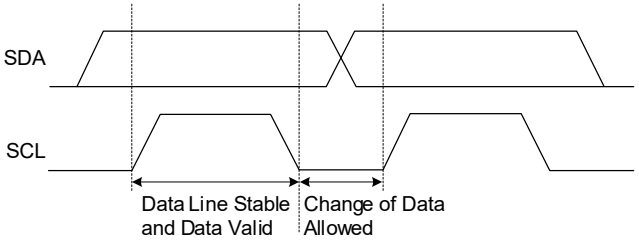


Figure 7. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 8 shows the byte transfer process with I²C interface.

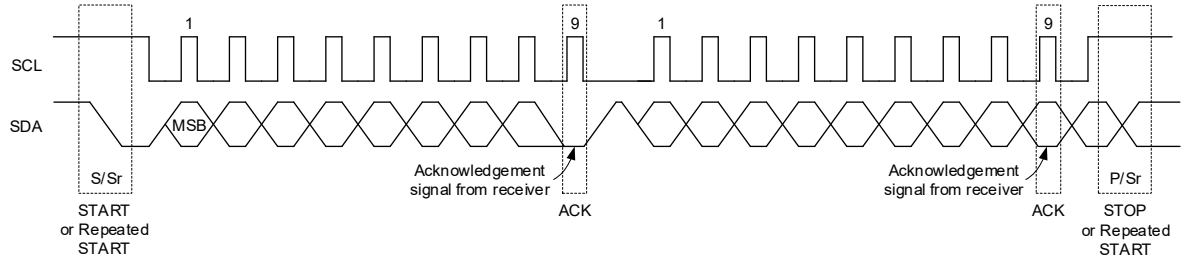


Figure 8. Byte Transfer Process

I²C COMPATIBLE INTERFACE (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 9.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 10 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 11), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

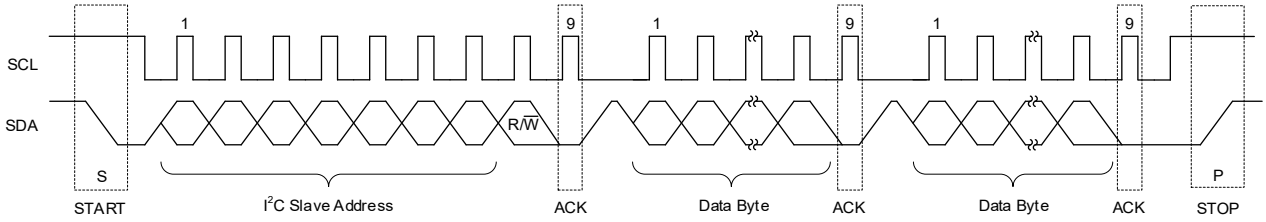


Figure 9. Data Transfer Transaction

I²C COMPATIBLE INTERFACE (continued)

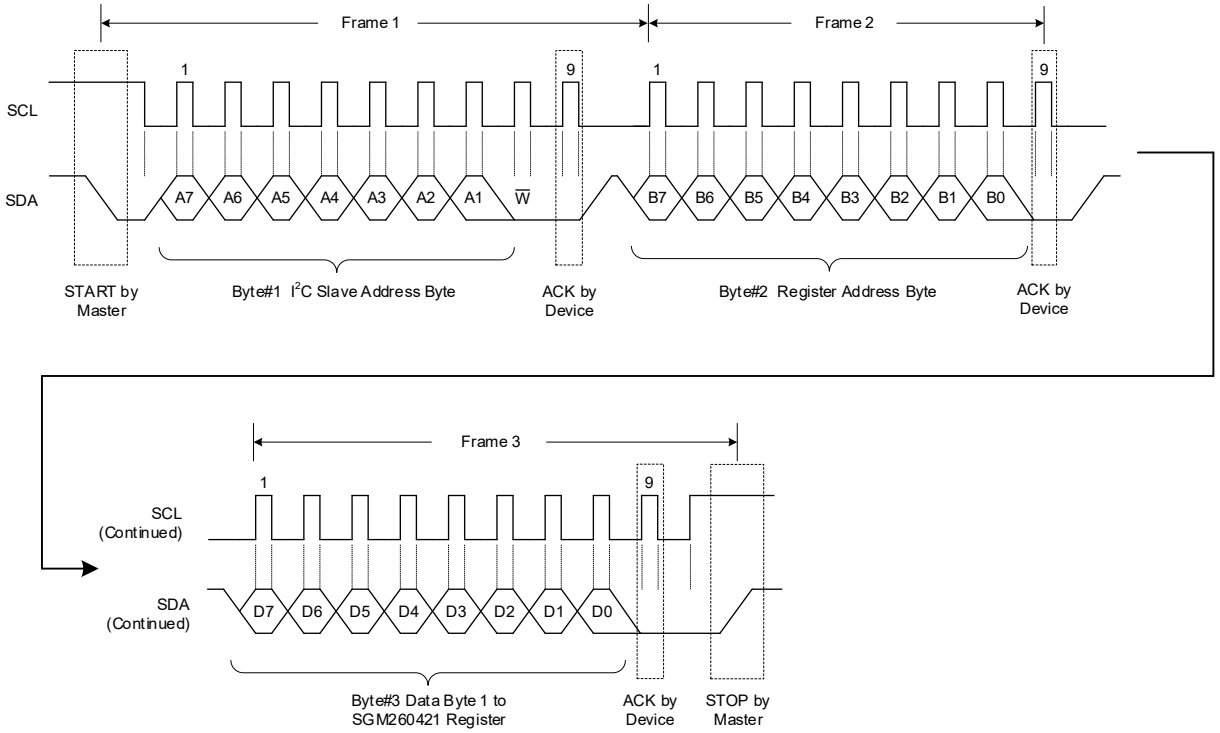


Figure 10. A Single Write Transaction

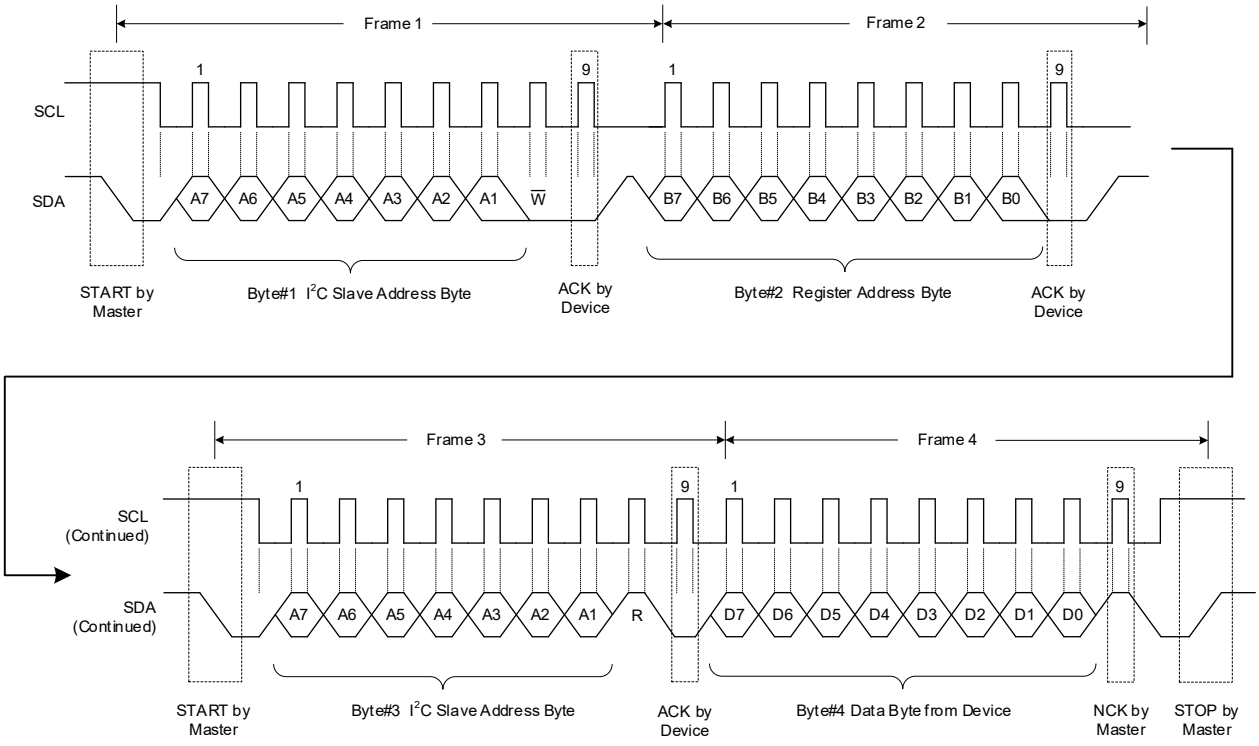


Figure 11. A Single Read Transaction

I²C COMPATIBLE INTERFACE (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM260421 for REG0x00 through REG0x52 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

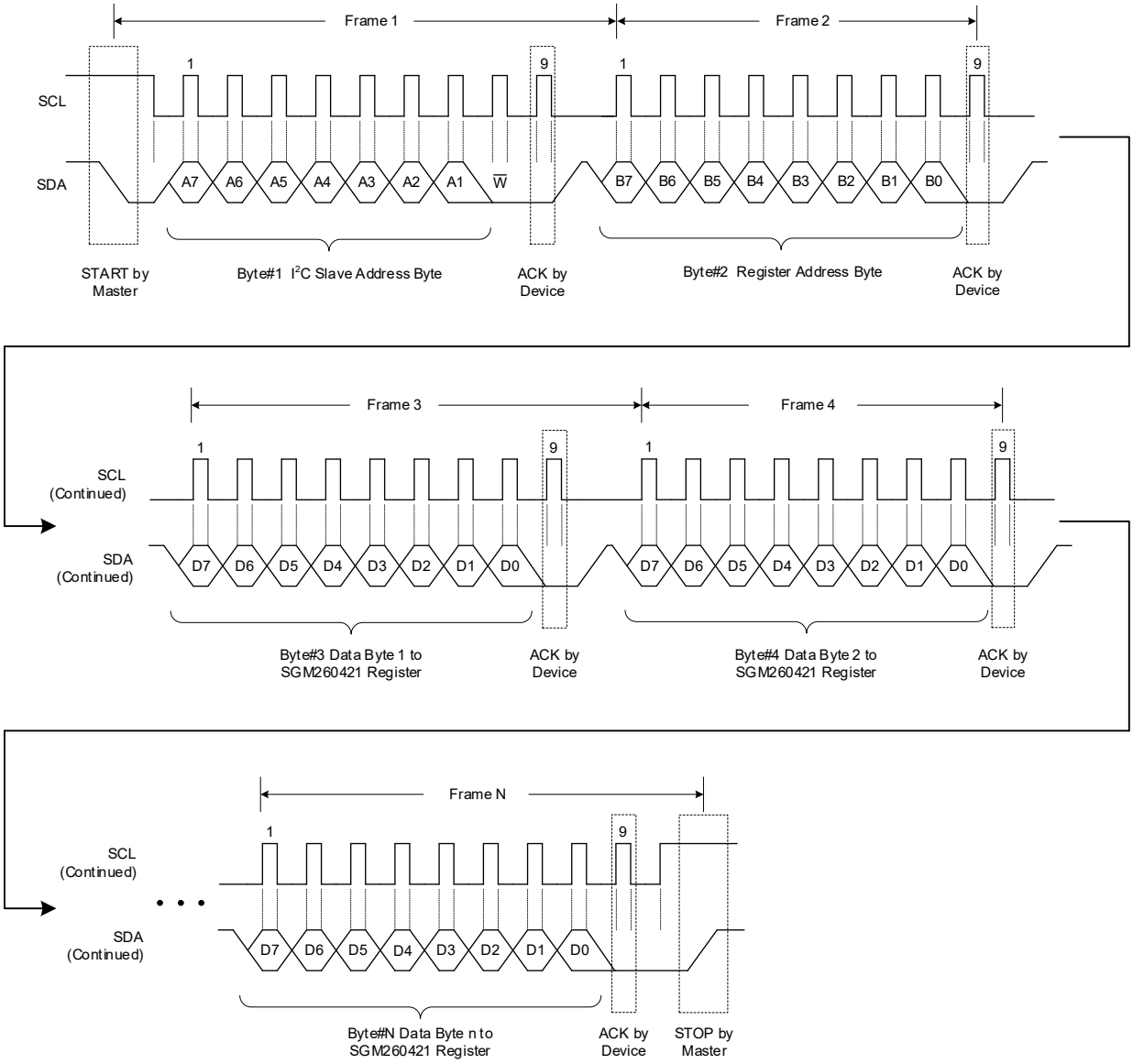


Figure 12. A Multi-Write Transaction

I²C COMPATIBLE INTERFACE (continued)

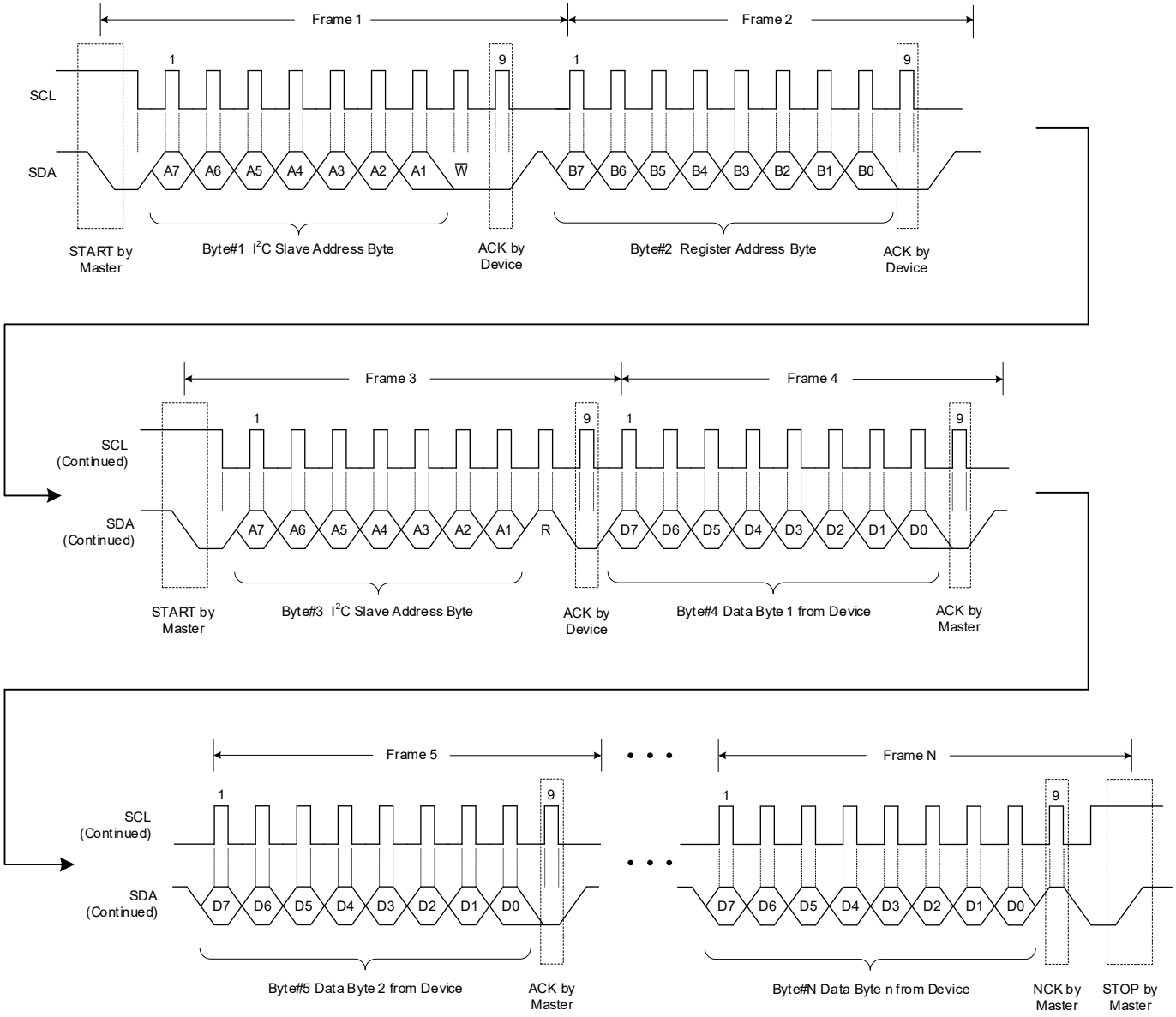


Figure 13. A Multi-Read Transaction

CMI OPTIONS

This section provides the basic default configuration settings for each available SGM260421 CMI option. IC functionality in this section supersedes functionality in the main datasheet. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 001: SGM260421-001

The following tables describe the SGM260421-001 IC default settings.

Table 8. Voltage and Currents

Rail	Output Voltage (V)			SLEEP Mode	DPSLP Mode	Current Limit (A)	f_{SW} (MHz)
Buck1	GPIO2 Status	High	LSW mode	On	Off	5	2
		Float	2.5				
		Low	2.5				
Buck2	GPIO2 Status	High	1.2	On	Off	4	2
		Float	1.2				
		Low	1.2				
Buck3	GPIO1 Status	High	0.8	On	DVS 0.7V	5	2
		Float	0.75		DVS 0.65V		
		Low	0.75		DVS 0.65V		
Buck4	GPIO4 Status	High	0.9	Off	On	3	2
		Float	0.9				
		Low	0.9				
LDO1	GPIO4 Status	High	1.8	On	On	0.5	N/A
		Float	LSW mode				
		Low	LSW mode				
LDO2	GPIO6 Status	High	1.8	On	On	0.5	N/A
		Low	LSW mode				

Table 9. Startup and Sequencing

Rail	On Delay (ms)	Extra Delay (ms)			Wake-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms)
Buck1	2	GPIO3 Status	High	1	2	175	0
			Float	0	1		
			Low	0	1		
Buck2	2		High	0	1	175	0
			Float	1	2		
			Low	1	2		
Buck3	1		High	0	0	175	1
			Float	0			
			Low	0			
Buck4	1.5		High	0	0	55	0
			Float	0			
			Low	0			
LDO1	0.5		High	0	0	100	1
			Float	0			
			Low	0			
LDO2	0.5		High	0	0	100	1
			Float	0			
			Low	0			

CMI OPTIONS (continued)

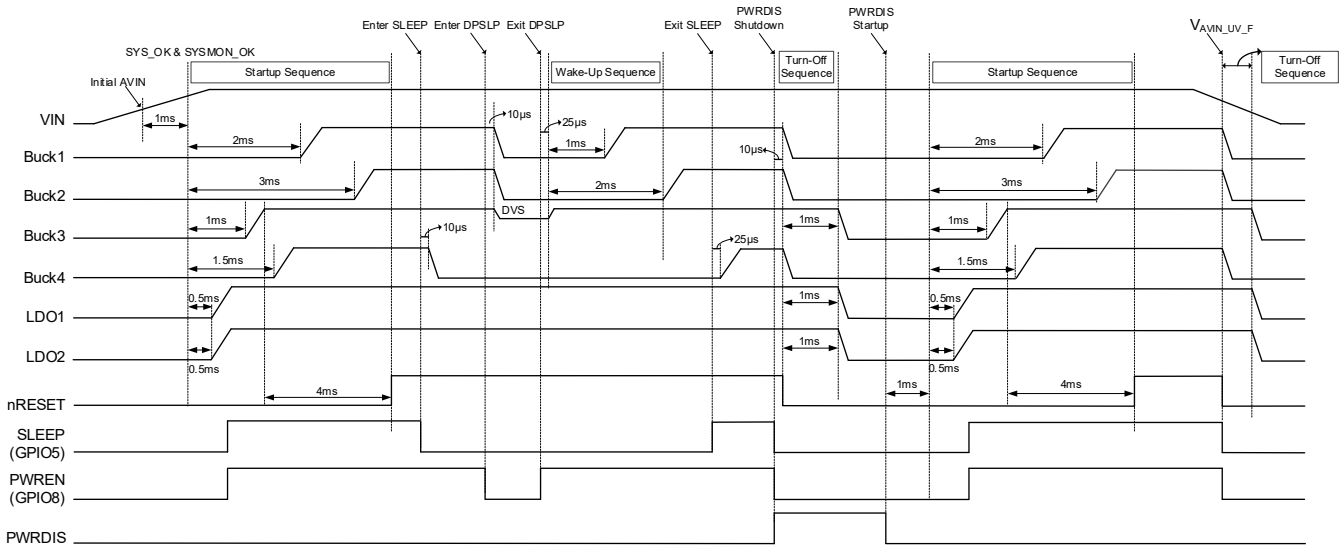


Figure 14. CMI 001 Sequence at GPIO3 = Float

I²C Address

The SGM260421-001 7-bit I²C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 - B3 Voltage Select

Refer to GPIO configuration section.

GPIO2 - B1/B2 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO3 - Extra Power-Up Delay Time and Wake-Up Delay Select

Refer to GPIO configuration section.

GPIO4 - B4/L1 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO5 - SLEEP

When SLEEP is H, the IC is in active mode. When SLEEP is L, the IC is in SLEEP mode.

GPIO6 - L2 Operation Mode Select

Refer to GPIO configuration section.

GPIO7 - No Function

GPIO8 - PWREN

When PWREN is H, the IC is in active mode. When PWREN is L, the IC is in DPSLP mode.

CMI OPTIONS (continued)

CMI 002: SGM260421-002

The following tables describe the SGM260421-002 IC default settings.

Table 10. Voltage and Currents

Rail	Output Voltage (V)			SLEEP Mode	DPSLP Mode	Current Limit (A)	f_{SW} (MHz)
Buck1	GPIO2 Status	High	LSW mode	Off	Off	5	2
		Float	2.5				
		Low	2.5				
Buck2	GPIO2 Status	High	0.91	On	DVS 0.68V	3	2
		Float	0.91				
		Low	1.2				
Buck3	GPIO3 Status	High	0.76	On	DVS 0.68V	5	2
		Float	0.76				
		Low	0.76				
Buck4	GPIO4 Status	High	1.1	Off	Off	3	2
		Float	1.2				
		Low	1.2				
LDO1	GPIO4 Status	High	1.8	On	On	0.5	N/A
		Float	1.8				
		Low	2.5				
LDO2	GPIO6 Status	High	1.8	On	On	0.5	N/A
		Low	LSW mode				

Table 11. Startup and Sequencing

Rail	On Delay (ms)	Extra Delay (ms)			Wake-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms)
Buck1	3	GPIO3 Status	High	0.25	0.75	175	0
			Float	0.25	0		
			Low	0.25	2		
Buck2	0.5		High	0.25	0	175	0
			Float	0.25			
			Low	0.25			
Buck3	0		High	0.75	0	175	0
			Float	0.75			
			Low	0			
Buck4	1.5		High	1.5	0.5	175	0
			Float	2.25			
			Low	0			
LDO1	2		High	0	0	100	0
			Float	0			
			Low	0			
LDO2	2		High	0	0	100	0
			Float	0			
			Low	0			

CMI OPTIONS (continued)

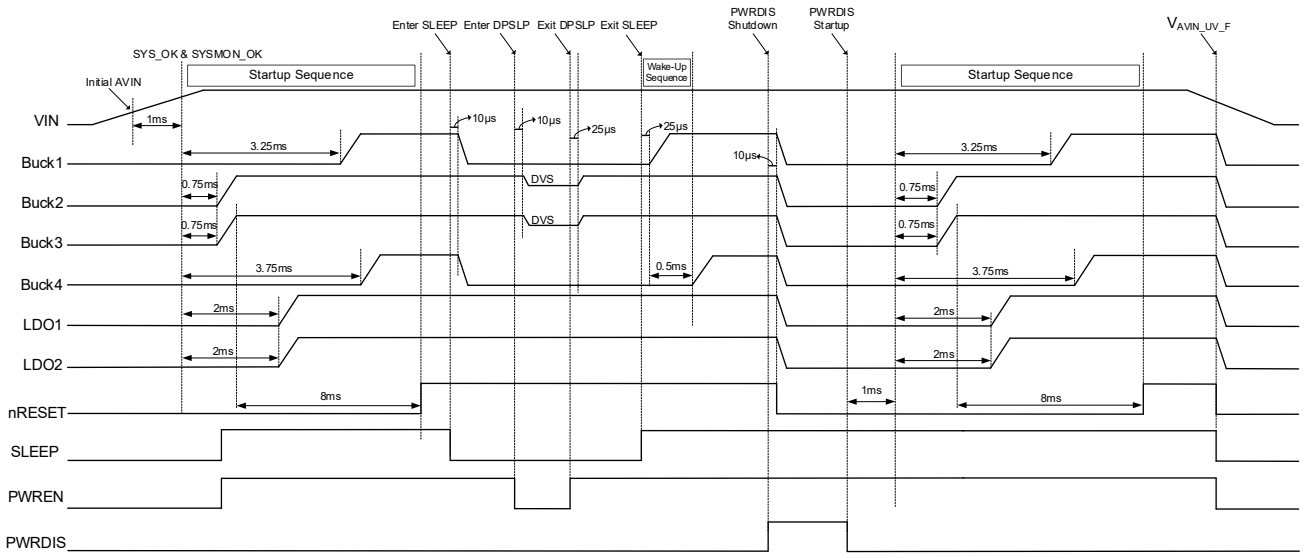


Figure 15. CMI 002 Sequence at GPIO3 = Float

I²C Address

The SGM260421-002 7-bit I²C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 - nRESET

GPIO1 is configured as an open-drain nRESET. nRESET goes high 8ms after Buck3 goes into regulation.

GPIO2 - B1/B2 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO3 - B3 Voltage, Extra Power-Up Delay Time and Wake-Up Delay Select

Refer to GPIO configuration section.

GPIO4 - B4/L1 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO5 - No Function

GPIO6 - L2 Operation Mode Select

Refer to GPIO configuration section.

GPIO7 - No Function

GPIO8 - No Function

CMI OPTIONS (continued)

CMI 003: SGM260421-003

The following tables describe the SGM260421-003 IC default settings.

Table 12. Voltage and Currents

Rail	Output Voltage (V)			SLEEP Mode	DPSLP Mode	Current Limit (A)	f_{SW} (MHz)
Buck1	GPIO2 Status	High	LSW mode	On	Off	5	2
		Float	2.5				
		Low	2.5				
Buck2	GPIO2 Status	High	1.2	On	Off	4	2
		Float	1.2				
		Low	1.2				
Buck3	GPIO1 Status	High	0.8	On	DVS 0.7V	5	2
		Float	0.75		DVS 0.65V		
		Low	0.75		DVS 0.65V		
Buck4	GPIO4 Status	High	0.9	Off	Off	3	2
		Float	0.9				
		Low	0.9				
LDO1	GPIO4 Status	High	1.8	On	On	0.5	N/A
		Float	LSW mode				
		Low	LSW mode				
LDO2	GPIO6 Status	High	1.8	On	On	0.5	N/A
		Low	LSW mode				

Table 13. Startup and Sequencing

Rail	On Delay (ms)	Extra Delay (ms)			Wake-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms)
Buck1	2	GPIO3 Status	High	1	2	175	0
			Float	0	1		
			Low	0	1		
Buck2	2		High	0	1	175	0
			Float	1	2		
			Low	1	2		
Buck3	1		High	0	0	175	1
			Float	0			
			Low	0			
Buck4	1.5		High	0	0	55	0
			Float	0			
			Low	0			
LDO1	0.5		High	0	0	100	1
			Float	0			
			Low	0			
LDO2	0.5		High	0	0	100	1
			Float	0			
			Low	0			

CMI OPTIONS (continued)

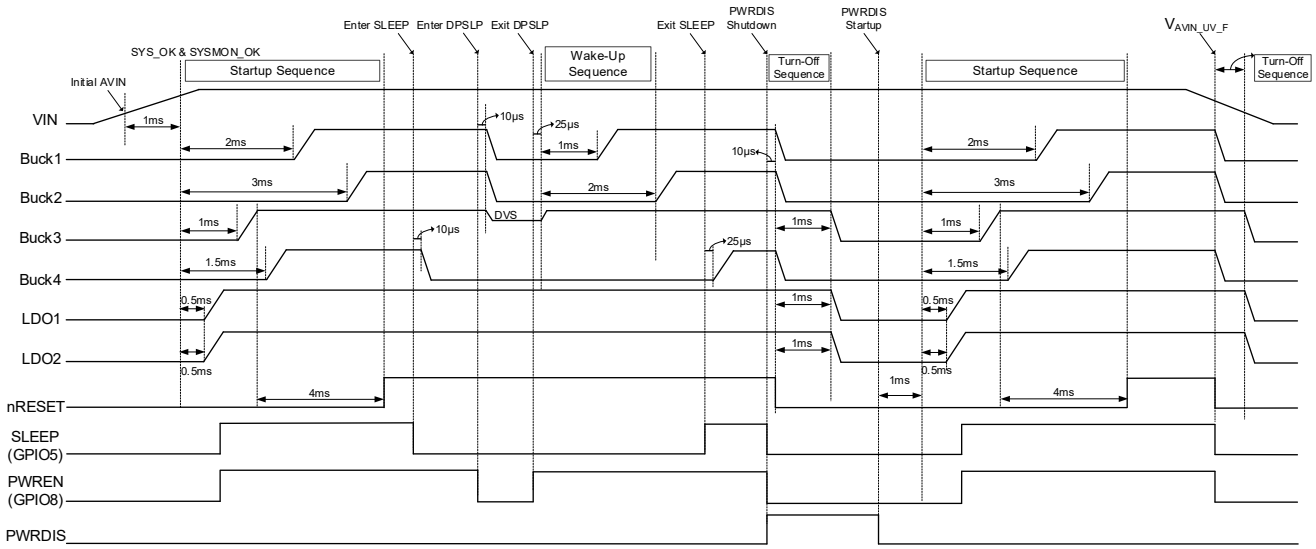


Figure 16. CMI 003 Sequence at GPIO3 = Float

I²C Address

The SGM260421-003 7-bit I²C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 - B3 Voltage Select

Refer to GPIO configuration section.

GPIO2 - B1/B2 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO3 - Extra Power-Up Delay Time and Wake-Up Delay Select

Refer to GPIO configuration section.

GPIO4 - B4/L1 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO5 - SLEEP

When SLEEP is H, the IC is in Active Mode. When SLEEP is L, the IC is in SLEEP mode.

GPIO6 - L2 Operation Mode Select

Refer to GPIO configuration section.

GPIO7 - No Function

GPIO8 - PWREN

When PWREN is H, the IC is in Active Mode. When PWREN is L, the IC is in DPSLP mode.

CMI OPTIONS (continued)

CMI 004: SGM260421-004

The following tables describe the SGM260421-004 IC default settings.

Table 14. Voltage and Currents

Rail	Output Voltage (V)			SLEEP Mode	DPSLP Mode	Current Limit (A)	f_{SW} (MHz)
Buck1	GPIO2 Status	High	LSW mode	On	On	5	2
		Float	2.5				
		Low	2.5				
Buck2	GPIO2 Status	High	0.91	On	On	3	2
		Float	0.91				
		Low	0.91				
Buck3	GPIO3 Status	High	0.78	On	On	5	2
		Float	0.78				
		Low	0.78				
Buck4	GPIO4 Status	High	1.2	On	On	3	2
		Float	1.2				
		Low	1.2				
LDO1	GPIO4 Status	High	1.8	On	On	0.5	N/A
		Float	1.8				
		Low	LSW mode				
LDO2	GPIO6 Status	High	1.8	On	On	0.5	N/A
		Low	LSW mode				

Table 15. Startup and Sequencing

Rail	On Delay (ms)	Extra Delay (ms)			Wake-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms)
Buck1	3	GPIO3 Status	High	0.25	0.75	175	0
			Float	0	0		
			Low	0.25	2		
Buck2	0.5		High	0.25	0	175	0
			Float	0	0		
			Low	0.25	0		
Buck3	0		High	0.75	0	175	0
			Float	0.5			
			Low	0			
Buck4	1.5		High	1.5	0.5	175	0
			Float	2			
			Low	0			
LDO1	2		High	0	0	100	0
			Float	0			
			Low	0			
LDO2	2		High	0	0	100	0
			Float	0			
			Low	0			

CMI OPTIONS (continued)

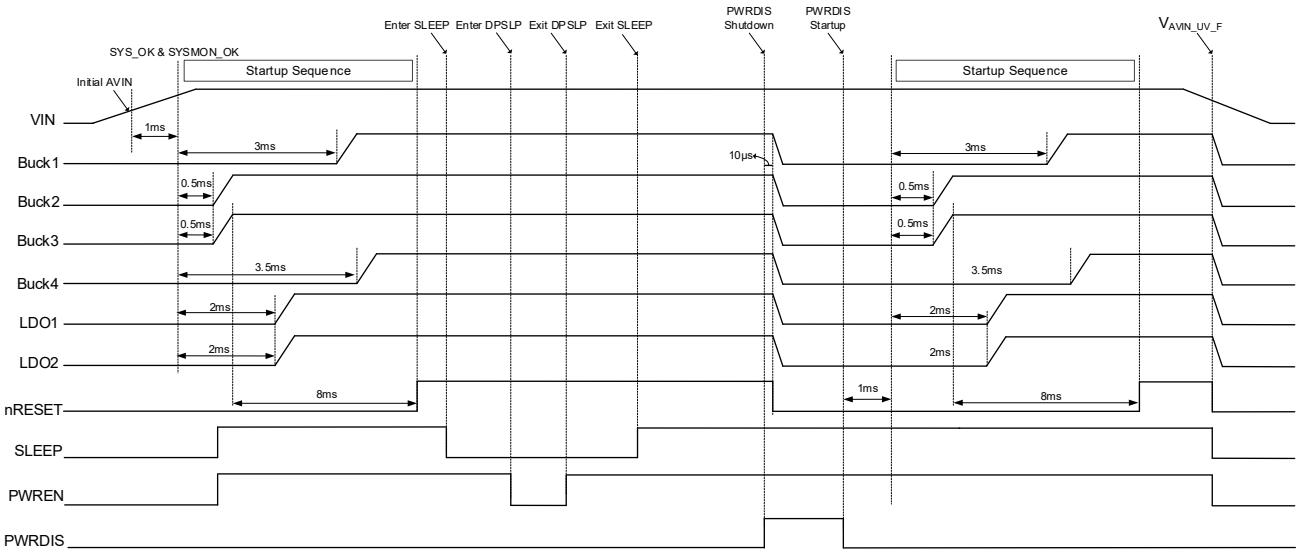


Figure 17. CMI 004 Sequence at GPIO3 = Float

I²C Address

The SGM260421-004 7-bit I²C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 - nRESET

GPIO1 is configured as an open-drain nRESET. nRESET goes high 8ms after Buck3 goes into regulation.

GPIO2 - B1/B2 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO3 - B3 Voltage, Extra Power-Up Delay Time and Wake-Up Delay Select

Refer to GPIO configuration section.

GPIO4 - B4/L1 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO5 - No Function

GPIO6 - L2 Operation Mode Select

Refer to GPIO configuration section.

GPIO7 - No Function

GPIO8 - No Function

CMI OPTIONS (continued)

CMI 006: SGM260421-006

The following tables describe the SGM260421-006 IC default settings.

Table 16. Voltage and Currents

Rail	Output Voltage (V)			SLEEP Mode	DPSLP Mode	Current Limit (A)	f_{SW} (MHz)
Buck1	GPIO2 Status	High	LSW Mode	On	On	5	2
		Float	2.5				
		Low	2.9				
Buck2	GPIO2 Status	High	1.2	On	On	4	2
		Float	1.2				
		Low	1.2				
Buck3	GPIO3 Status	High	0.75	On	On	5	2
		Float	0.75				
		Low	0.75				
Buck4	N/A	N/A	0.9	On	On	3	2
		N/A					
		N/A					
LDO1	N/A	N/A	1.8	On	On	0.5	N/A
		N/A					
		N/A					
LDO2	N/A	N/A	1.8	On	On	0.5	N/A
		N/A					

Table 17. Startup and Sequencing

Rail	On Delay (ms)	Extra Delay (ms)			Wake-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms)
Buck1	2.5	GPIO3 Status	High	1	0	175	0
			Float	0	0		
			Low	0.5	0		
Buck2	3		High	0	0	175	0
			Float	0	0		
			Low	0	0		
Buck3	0.5		High	0	0	175	1
			Float	0			
			Low	0			
Buck4	2		High	0	0	175	0
			Float	0			
			Low	0			
LDO1	1		High	0	0	100	1
			Float	0			
			Low	0			
LDO2	1.5		High	0	0	100	1
			Float	0			
			Low	0			

CMI OPTIONS (continued)

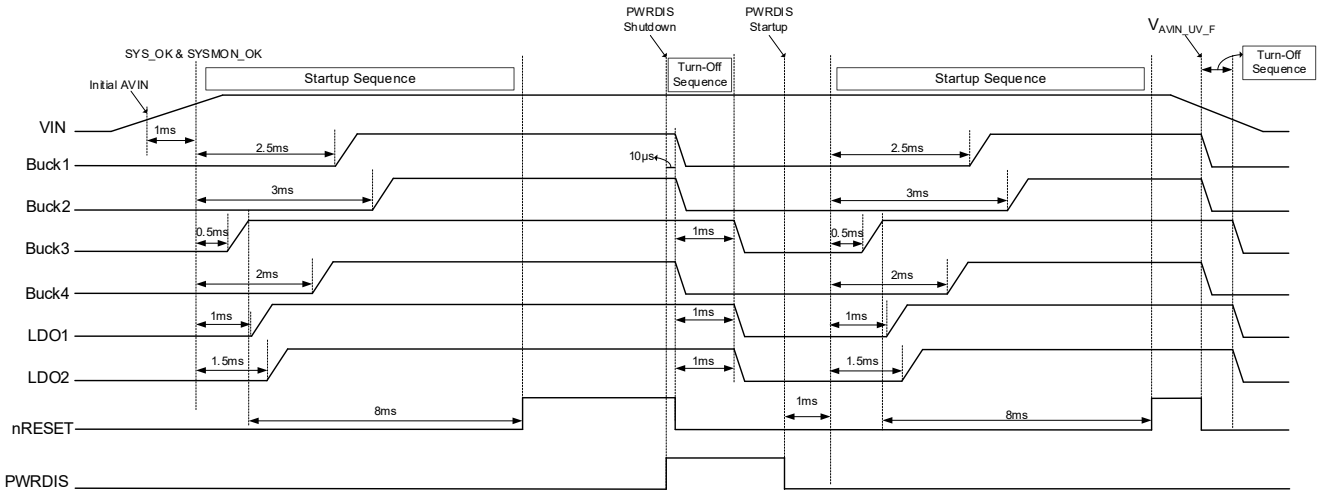


Figure 18. CMI 006 Sequence at GPIO3 = Float, GPIO8 = High

I²C Address

The SGM260421-006 7-bit I²C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 - nRESET

GPIO1 is configured as an open-drain nRESET. nRESET goes high 8ms after Buck3 goes into regulation.

GPIO2 - B1/B2 Operation Mode and Voltage Select

Refer to GPIO configuration section.

GPIO3 - B3 Voltage, Extra Power-Up Delay Time and Wake-Up Delay Select

Refer to GPIO configuration section.

GPIO4 - No Function

GPIO5 - I²C Controlled Output

Refer to GPIO configuration section.

GPIO6 - nIRQ

Refer to GPIO configuration section.

GPIO7 - PG of Internal Rail (Buck4)

Refer to GPIO configuration section.

GPIO8 - EN of Internal Rail (Buck4)

Refer to GPIO configuration section.

REGISTER MAPS

Register Types

The register types of SGM260421 are as follows.

Basic Volatile

Customer R/W (Read and Write) and R (Read only).

The register values can be modified to change the device function. However, if the power is recycled, the changes are lost. The default values of register are fixed and cannot be altered.

Basic Non-Volatile

The register values can be modified to change the device function. Although changes are lost upon power is recycled, the default values can be pre-set at the factory to tailor the device for specific applications. For more demands, please consult with sales.

The following table shows the SGM260421 register map. It shows the register default value of SGM260421-001 CMI.

ADDR (HEX)	REGISTER NAME	DEFAULT VALUE (HEX)	TYPE
0x00	TOP_STATUS_REG	00	R
0x01	RAIL_STATUS_REG	00	R
0x02	RAIL_FLAG_REG0	00	R
0x03	RAIL_FLAG_REG1	00	R
0x04	RAIL_FLAG_REG2	00	R
0x05	nIRQ_FLAG_REG	00	R
0x06	nIRQ_MASK_REG	00	R/W
0x07	nRESET_MASK_REG	00	R/W
0x08	GPIO1_REG	3B	R/W
0x09	GPIO2_REG	52	R/W
0x0A	GPIO3_REG	50	R/W
0x0B	GPIO4_REG	53	R/W
0x0C	GPIO5_REG	30	R/W
0x0D	GPIO6_REG	53	R/W
0x0E	GPIO7_REG	49	R/W
0x0F	GPIO8_REG	3A	R/W
0x10	INTERNAL_RAIL_EN_REG0	00	R/W
0x11	INTERNAL_RAIL_EN_REG1	00	R/W
0x12	INTERNAL_RAIL_EN_REG2	00	R/W
0x13	INTERNAL_RAIL_PG_REG0	00	R/W
0x14	INTERNAL_RAIL_PG_REG1	00	R/W
0x15	INTERNAL_RAIL_PG_REG2	00	R/W
0x16	EXTRA_DLY_REG0	40	R/W
0x17	EXTRA_DLY_REG1	00	R/W
0x18	EXTRA_DLY_REG2	44	R/W
0x19	EXTRA_DLY_REG3	00	R/W
0x1A	EXTRA_DLY_REG4	00	R/W
0x1B	EXTRA_DLY_REG5	00	R/W
0x1C	EXTRA_DLY_REG6	00	R/W
0x1D	EXTRA_DLY_REG7	00	R/W
0x1E	EXTRA_DLY_REG8	00	R/W

REGISTER MAPS (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT VALUE (HEX)	TYPE
0x1F	EXT_EN_REG0	00	R/W
0x20	EXT_EN_REG1	14	R/W
0x21	Reserved	FF	R/W
0x22	VIN_VTH_REG0	00	R/W
0x23	VIN_VTH_REG1	40	R/W
0x24	ADDRESS_REG	00	R
0x25	MANUFACTURE_ID_REG	42	R
0x26	DEVICE_ID_REG	49	R
0x27	CMI_NUMBER_REG	01	R
0x28	B1_CFG_REG0	6B	R/W
0x29	B1_CFG_REG1	90	R/W
0x2A	B1_VSET0_REG	68	R/W
0x2B	B1_VSET1_REG	E8	R/W
0x2C	B2_CFG_REG0	6B	R/W
0x2D	B2_CFG_REG1	8A	R/W
0x2E	B2_VSET0_REG	46	R/W
0x2F	B2_VSET1_REG	46	R/W
0x30	B2_DVS_VSET_REG	46	R/W
0x31	B3_CFG_REG0	5B	R/W
0x32	B3_CFG_REG1	90	R/W
0x33	B3_VSET0_REG	9E	R/W
0x34	B3_VSET1_REG	19	R/W
0x35	B3_VSET2_REG	19	R/W
0x36	B3_DVS_VSET0_REG	94	R/W
0x37	B3_DVS_VSET1_REG	0F	R/W
0x38	B3_DVS_VSET2_REG	0F	R/W
0x39	B4_CFG_REG0	59	R/W
0x3A	B4_CFG_REG1	80	R/W
0x3B	B4_VSET0_REG	8A	R/W
0x3C	B4_VSET1_REG	0A	R/W
0x3D	B4_VSET2_REG	8A	R/W
0x3E	LDO_CFG_REG0	D8	R/W
0x3F	LDO_CFG_REG1	03	R/W
0x40	L1_VSET0_REG	90	R/W
0x41	L1_VSET1_REG	10	R/W
0x42	L2_VSET_REG	90	R/W
0x43	EN_CTRL_REG	FD	R/W
0x44	DISCH_CTRL_REG0	FD	R/W
0x45	DISCH_CTRL_REG1	45	R/W
0x46	DISCH_CTRL_REG2	55	R/W
0x47	LPM_CTRL_REG	02	R/W
0x48	SLEEP_CTRL_REG	EC	R/W
0x49	DPSLP_CTRL_REG	3C	R/W

REGISTER MAPS (continued)

ADDR (HEX)	REGISTER NAME	DEFAULT VALUE (HEX)	TYPE
0x4A	B1_TIME_REG	40	R/W
0x4B	B2_TIME_REG	40	R/W
0x4C	B3_TIME_REG	29	R/W
0x4D	B4_TIME_REG	31	R/W
0x4E	L1_TIME_REG	18	R/W
0x4F	L2_TIME_REG	18	R/W
0x50	WAKEUP_DLY_GPIO3_REG0	B0	R/W
0x51	WAKEUP_DLY_GPIO3_REG1	94	R/W
0x52	PWRDIS_REG	00	R/W

REGISTER MAPS (continued)

REG0x00: TOP_STATUS_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SYSMON	0	R	Real Time Status 0 = V_{IN} < V_{SYSMON} (default) 1 = V_{IN} > V_{SYSMON}
D[6]	SYSWARN	0	R	Real Time Status 0 = V_{IN} < $V_{SYSWARN}$ (default) 1 = V_{IN} > $V_{SYSWARN}$
D[5]	POK_OV	0	R	Real Time Status 0 = V_{IN} < V_{POK_OV} (default) 1 = V_{IN} > V_{POK_OV}
D[4]	VIN_OV	0	R	Real Time Status 0 = V_{IN} < V_{IN_OV} (default) 1 = V_{IN} > V_{IN_OV}
D[3]	OT_WARN	0	R	Real Time Status 0 = Die temperature < OT_WARN (default) 1 = Die temperature > OT_WARN
D[2]	OT	0	R	Real Time Status 0 = Die temperature < OT (default) 1 = Die temperature > OT
D[1]	nRESET	0	R	Real Time Status 0 = Indicates PMIC power not good (default) 1 = Indicates PMIC power good
D[0]	nIRQ	0	R	Real Time Status 0 = Indicates PMIC has fault (default) 1 = Indicates PMIC has no fault

REG0x01: RAIL_STATUS_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Buck1_PG	0	R	Real Time Status 0 = Buck1 power not good (default) 1 = Buck1 power good
D[6]	Buck2_PG	0	R	Real Time Status 0 = Buck2 power not good (default) 1 = Buck2 power good
D[5]	Buck3_PG	0	R	Real Time Status 0 = Buck3 power not good (default) 1 = Buck3 power good
D[4]	Buck4_PG	0	R	Real Time Status 0 = Buck4 power not good (default) 1 = Buck4 power good
D[3]	LDO1_PG	0	R	Real Time Status 0 = LDO1 power not good (default) 1 = LDO1 power good
D[2]	LDO2_PG	0	R	Real Time Status 0 = LDO2 power not good (default) 1 = LDO2 power good
D[1:0]	Reserved	00	R	Reserved

REGISTER MAPS (continued)

REG0x02: RAIL_FLAG_REG0

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Buck1_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck1 triggers UV
D[6]	Buck2_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck2 triggers UV
D[5]	Buck3_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck3 triggers UV
D[4]	Buck4_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck4 triggers UV
D[3]	LDO1_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO1 triggers UV
D[2]	LDO2_UV	0	R	Flag bit, UV fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO2 triggers UV
D[1:0]	Reserved	00	R	Reserved

REG0x03: RAIL_FLAG_REG1

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Buck1_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck1 triggers OV
D[6]	Buck2_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck2 triggers OV
D[5]	Buck3_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck3 triggers OV
D[4]	Buck4_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck4 triggers OV
D[3]	LDO1_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO1 triggers OV
D[2]	LDO2_OV	0	R	Flag bit, OV fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO2 triggers OV
D[1:0]	Reserved	00	R	Reserved

REGISTER MAPS (continued)

REG0x04: RAIL_FLAG_REG2

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Buck1_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck1 triggers ILIM
D[6]	Buck2_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck2 triggers ILIM
D[5]	Buck3_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck3 triggers ILIM
D[4]	Buck4_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = Buck4 triggers ILIM
D[3]	LDO1_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO1 triggers ILIM
D[2]	LDO2_ILIM	0	R	Flag bit, ILIM fault removed and read this bit to clear it. 0 = Normal (default) 1 = LDO2 triggers ILIM
D[1:0]	Reserved	00	R	Reserved

REG0x05: nIRQ_FLAG_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SYSMON_FLAG	0	R	0 = No interrupt event occurs. 1 = Indicates the interrupt flag of the event. Interrupt event removed and read this bit to clear it.
D[6]	SYSWARN_FLAG	0	R	
D[5]	POK_OV_FLAG	0	R	
D[4]	VIN_OV_FLAG	0	R	
D[3]	OT_WARN_FLAG	0	R	
D[2]	OT_FLAG	0	R	
D[1]	OUTPUT_OVUV_FLAG	0	R	
D[0]	Reserved	0	R	

REG0x06: nIRQ_MASK_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SYSMON_FLAG_MASK	0	R/W	Only mask the interrupt flag events to the nIRQ inputs. But the flag bits still work well to indicate the interrupt events. 0 = Unmask the interrupt flag of the event. If the event flag is set 1, nIRQ will assert low. 1 = Mask the interrupt flag of the event. If the event flag is set 1, nIRQ will not assert low.
D[6]	SYSWARN_FLAG_MASK	0	R/W	
D[5]	POK_OV_FLAG_MASK	0	R/W	
D[4]	VIN_OV_FLAG_MASK	0	R/W	
D[3]	OT_WARN_FLAG_MASK	0	R/W	
D[2]	OT_FLAG_MASK	0	R/W	
D[1]	OUTPUT_OVUV_FLAG_MASK	0	R/W	
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x07: nRESET_MASK_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Buck1_PBAD_RESET_MASK	0	R/W	Mask the protection function which will make nRESET signal active. 0 = Not mask, the event will assert nRESET low. 1 = Mask the event, the event will not assert nRESET low. Note: Only the rails power bad event, like output OV or UV events can assert nRESET low. Disabling the rails through I^2C or GPIO won't affect nRESET signal. nRESET keeps high when entering SLEEP or DPSLP mode.
D[6]	Buck2_PBAD_RESET_MASK	0	R/W	
D[5]	Buck3_PBAD_RESET_MASK	0	R/W	
D[4]	Buck4_PBAD_RESET_MASK	0	R/W	
D[3]	LDO1_PBAD_RESET_MASK	0	R/W	
D[2]	LDO2_PBAD_RESET_MASK	0	R/W	
D[1]	VIN_OV_RESET_MASK	0	R/W	
D[0]	OT_RESET_MASK	0	R/W	

REG0x08: GPIO1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO1_PUSHPULL_EN	0	R/W	0 = GPIO1 open-drain output (default) 1 = GPIO1 push-pull output. This bit is only effective when GPIO1 is configured to output function.
D[6:4]	nRST_DLY	011	R/W	The delay time from the PG signal of Buck3 rail in the power-up sequence to nRESET signal. 000 = 0.5ms 001 = 1ms 010 = 2ms 011 = 4ms (default) 100 = 8ms 101 = 16ms 110 = 32ms 111 = 64ms
D[3]	GPIO1_FUNC_CONFIG	1	R/W	0 = nRESET 1 = Buck3 output voltage select (default) If GPIO1 is configured as Buck3 voltage select function, and GPIO3 is also configured as Buck3 voltage and extra delay time select function, Buck3 voltage is decided by GPIO1 status.
D[2:0]	Reserved	011	R/W	Reserved

REGISTER MAPS (continued)

REG0x09: GPIO2_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO2_PUSHPULL_EN	0	R/W	0 = GPIO2 open-drain output (default) 1 = GPIO2 push-pull output. This bit is only effective when GPIO2 is configured to output function.
D[6:3]	GPIO2_FUNC_CONFIG	1010	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) 1010 = B1/B2 operation mode and voltage select (input) (default) Above 1010 are not used.
D[2]	GPIO2_I2C_CTRL	0	R/W	If the GPIO2 is configured to I^2C controlled output, this bit can control the GPIO2 output voltage level. 0 = Low level (default) 1 = High level
D[1:0]	Reserved	10	R/W	Reserved

REG0x0A: GPIO3_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO3_PUSHPULL_EN	0	R/W	0 = GPIO3 open-drain output (default) 1 = GPIO3 push-pull output. This bit is only effective when GPIO3 is configured to output function.
D[6:3]	GPIO3_FUNC_CONFIG	1010	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) 1010 = B3 voltage and all the rails' extra delay time select. (input) (default) Above 1010 are not used.
D[2]	GPIO3_I2C_CTRL	0	R/W	If the GPIO3 is configured to I^2C controlled output, this bit can control the GPIO3 output voltage level. 0 = Low level (default) 1 = High level
D[1:0]	Reserved	00	R/W	Reserved

REGISTER MAPS (continued)

REG0x0B: GPIO4_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO4_PUSHPULL_EN	0	R/W	0 = GPIO4 open-drain output (default) 1 = GPIO4 push-pull output. This bit is only effective when GPIO4 is configured to output function.
D[6:3]	GPIO4_FUNC_CONFIG	1010	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) 1010 = B4/L1 operation mode and voltage select. (input) (default) Above 1010 are not used.
D[2]	GPIO4_I2C_CTRL	0	R/W	If the GPIO4 is configured to I^2C controlled output, this bit can control the GPIO4 output voltage level. 0 = Low level (default) 1 = High level
D[1]	L1_MODE_AT_GPIO4_F	1	R/W	0 = L1 is LDO mode when GPIO4 float. 1 = L1 is LSW mode when GPIO4 float (default) This bit is effective when GPIO4 configured to B4/L1 operation mode and voltage select function.
D[0]	L1_MODE_AT_GPIO4_L	1	R/W	0 = L1 is LDO mode when GPIO4 low. 1 = L1 is LSW mode when GPIO4 low (default) This bit is effective when GPIO4 configured to B4/L1 operation mode and voltage select function.

REG0x0C: GPIO5_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO5_PUSHPULL_EN	0	R/W	0 = GPIO5 open-drain output (default) 1 = GPIO5 push-pull output. This bit is only effective when GPIO5 is configured to output function.
D[6:3]	GPIO5_FUNC_CONFIG	0110	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) (default) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) Above 1001 are not used.
D[2]	GPIO5_I2C_CTRL	0	R/W	If the GPIO5 is configured to I^2C controlled output, this bit can control the GPIO5 output voltage level. 0 = Low level (default) 1 = High level
D[1]	B4_MODE_AT_GPIO4_F	0	R/W	0 = B4 is Buck mode when GPIO4 float. (default) 1 = B4 is LDO mode when GPIO4 float This bit is effective when GPIO4 configured to B4/L1 operation mode and voltage select function.
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x0D: GPIO6_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO6_PUSHPULL_EN	0	R/W	0 = GPIO6 open-drain output (default) 1 = GPIO6 push-pull output. This bit is only effective when GPIO6 is configured to output function.
D[6:3]	GPIO6_FUNC_CONFIG	1010	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) 1010 = L2 operation mode select. (input) (default) Above 1010 are not used.
D[2]	GPIO6_I2C_CTRL	0	R/W	If the GPIO6 is configured to I^2C controlled output, this bit can control the GPIO6 output voltage level. 0 = Low level (default) 1 = High level
D[1:0]	Reserved	11	R/W	Reserved

REG0x0E: GPIO7_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_PUSHPULL_EN	0	R/W	0 = GPIO7 open-drain output (default) 1 = GPIO7 push-pull output. This bit is only effective when GPIO7 is configured to output function.
D[6:3]	GPIO7_FUNC_CONFIG	1001	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) (default) Above 1001 are not used.
D[2]	GPIO7_I2C_CTRL	0	R/W	If the GPIO7 is configured to I^2C controlled output, this bit can control the GPIO7 output voltage level. 0 = Low level (default) 1 = High level
D[1:0]	Reserved	01	R/W	Reserved

REGISTER MAPS (continued)

REG0x0F: GPIO8_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO8_PUSHPULL_EN	0	R/W	0 = GPIO8 open-drain output (default) 1 = GPIO8 push-pull output. This bit is only effective when GPIO8 is configured to output function.
D[6:3]	GPIO8_FUNC_CONFIG	0111	R/W	0000 = nIRQ (output) 0001 = SYSMON (output) 0010 = SYSWARN (output) 0011 = EXT_EN (output) 0100 = I^2C controlled output (output) 0101 = PG of Internal rail (output) 0110 = SLEEP (input) 0111 = PWREN (input) (default) 1000 = PWRDIS (input) 1001 = EN of internal rail (input) Above 1001 are not used.
D[2]	GPIO8_I2C_CTRL	0	R/W	If the GPIO8 is configured to I^2C controlled output, this bit can control the GPIO8 output voltage level. 0 = Low level (default) 1 = High level
D[1:0]	Reserved	10	R/W	Reserved

REG0x10: INTERNAL_RAIL_EN_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_EN_CONFIG	0	R/W	0 = B1 has no GPIO as EN control. (default) 1 = B1 has a GPIO as EN control.
D[6:4]	B1_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B1_EN_CONFIG = 1.
D[3]	B2_EN_CONFIG	0	R/W	0 = B2 has no GPIO as EN control (default) 1 = B2 has a GPIO as EN control
D[2:0]	B2_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B2_EN_CONFIG = 1.

REGISTER MAPS (continued)

REG0x11: INTERNAL_RAIL_EN_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_EN_CONFIG	0	R/W	0 = B3 has no GPIO as EN control (default) 1 = B3 has a GPIO as EN control
D[6:4]	B3_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B3_EN_CONFIG = 1.
D[3]	B4_EN_CONFIG	0	R/W	0 = B4 has no GPIO as EN control (default) 1 = B4 has a GPIO as EN control
D[2:0]	B4_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B4_EN_CONFIG = 1.

REG0x12: INTERNAL_RAIL_EN_REG2

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	L1_EN_CONFIG	0	R/W	0 = LDO1 has no GPIO as EN control (default) 1 = LDO1 has a GPIO as EN control
D[6:4]	L1_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when L1_EN_CONFIG = 1.
D[3]	L2_EN_CONFIG	0	R/W	0 = LDO2 has no GPIO as EN control (default) 1 = LDO2 has a GPIO as EN control
D[2:0]	L2_EN_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when L2_EN_CONFIG = 1.

REGISTER MAPS (continued)

REG0x13: INTERNAL_RAIL_PG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_PG_CONFIG	0	R/W	0 = B1 has no GPIO as PG output (default) 1 = B1 has a GPIO as PG output
D[6:4]	B1_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B1_PG_CONFIG = 1.
D[3]	B2_PG_CONFIG	0	R/W	0 = B2 has no GPIO as PG output (default) 1 = B2 has a GPIO as PG output
D[2:0]	B2_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B2_PG_CONFIG = 1.

REG0x14: INTERNAL_RAIL_PG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_PG_CONFIG	0	R/W	0 = B3 has no GPIO as PG output (default) 1 = B3 has a GPIO as PG output
D[6:4]	B3_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B3_PG_CONFIG = 1.
D[3]	B4_PG_CONFIG	0	R/W	0 = B4 has no GPIO as PG output (default) 1 = B4 has a GPIO as PG output
D[2:0]	B4_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when B4_PG_CONFIG = 1.

REGISTER MAPS (continued)

REG0x15: INTERNAL_RAIL_PG_REG2

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	L1_PG_CONFIG	0	R/W	0 = L1 has no GPIO as PG output (default) 1 = L1 has a GPIO as PG output
D[6:4]	L1_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when L1_PG_CONFIG = 1.
D[3]	L2_PG_CONFIG	0	R/W	0 = L2 has no GPIO as PG output (default) 1 = L2 has a GPIO as PG output
D[2:0]	L2_PG_SEL	000	R/W	000 = GPIO2 (default) 001 = GPIO3 010 = GPIO4 011 = GPIO5 100 = GPIO6 101 = GPIO7 110 = GPIO8 Above 110 are not used. These bits only effective when L2_PG_CONFIG = 1.

REG0x16: EXTRA_DLY_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B1_EXTRA_DLY_GPIO3_H	0100	R/W	Buck1 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x16[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B1_EXTRA_DLY_GPIO3_F	0000	R/W	Buck1 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x16[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x17: EXTRA_DLY_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B1_EXTRA_DLY_GPIO3_L	0000	R/W	Buck1 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x17[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B2_EXTRA_DLY_GPIO3_H	0000	R/W	Buck2 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x17[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REGISTER MAPS (continued)

REG0x18: EXTRA_DLY_REG2

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B2_EXTRA_DLY_GPIO3_F	0100	R/W	Buck2 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x18[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B2_EXTRA_DLY_GPIO3_L	0100	R/W	Buck2 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x18[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x19: EXTRA_DLY_REG3

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B3_EXTRA_DLY_GPIO3_H	0000	R/W	Buck3 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x19[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B3_EXTRA_DLY_GPIO3_F	0000	R/W	Buck3 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x19[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x1A: EXTRA_DLY_REG4

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B3_EXTRA_DLY_GPIO3_L	0000	R/W	Buck3 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1A[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B4_EXTRA_DLY_GPIO3_H	0000	R/W	Buck4 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1A[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x1B: EXTRA_DLY_REG5

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B4_EXTRA_DLY_GPIO3_F	0000	R/W	Buck4 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1B[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	B4_EXTRA_DLY_GPIO3_L	0000	R/W	Buck4 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1B[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REGISTER MAPS (continued)

REG0x1C: EXTRA_DLY_REG6

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	L1_EXTRA_DLY_GPIO3_H	0000	R/W	LDO1 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1C[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	L1_EXTRA_DLY_GPIO3_F	0000	R/W	LDO1 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1C[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x1D: EXTRA_DLY_REG7

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	L1_EXTRA_DLY_GPIO3_L	0000	R/W	LDO1 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1D[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	L2_EXTRA_DLY_GPIO3_H	0000	R/W	LDO2 extra delay time when GPIO3 is high. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1D[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REG0x1E: EXTRA_DLY_REG8

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	L2_EXTRA_DLY_GPIO3_F	0000	R/W	LDO2 extra delay time when GPIO3 is float. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1E[7:4]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.
D[3:0]	L2_EXTRA_DLY_GPIO3_L	0000	R/W	LDO2 extra delay time when GPIO3 is low. Offset = 0ms Step = 0.25ms Delay time = DEC(0x1E[3:0]) × 0.25ms These bits are effective when GPIO3 as extra delay time select function.

REGISTER MAPS (continued)

REG0x1F: EXT_EN_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	EXT_EN_INPUT_TRIGGER	0000	R/W	0000 = VIN SYSMON rising threshold (default) 0001 = Buck1 PG 0010 = Buck2 PG 0011 = Buck3 PG 0100 = Buck4 PG 0101 = LDO1 PG 0110 = LDO2 PG 0111 = GPIO2 1000 = GPIO3 1001 = GPIO4 1010 = GPIO5 1011 = GPIO6 1100 = GPIO7 1101 = GPIO8 Program the EXT_EN startup sequence input trigger if a GPIO is configured to EXT_EN function. Above 1101 are not used.
D[3:0]	EXT_EN_ON_DLY	0000	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x1F[3:0]) × 0.5ms Set EXT_EN delay time from the input trigger to EXT_EN become high.

REG0x20: EXT_EN_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	EXT_EN_OFF_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set EXT_EN turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[4:2]	EXT_EN_WAKEUP_DLY	101	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms (default) 110 = 4ms 111 = 8ms Set EXT_EN wake-up delay time when exiting SLEEP or DPSLP mode.
D[1]	EXT_EN_ON_SLEEP	0	R/W	0 = Pull EXT_EN low to shutdown external rail when IC enters sleep mode. (default) 1 = EXT_EN keeps high when IC enters SLEEP mode.
D[0]	EXT_EN_ON_DPSLP	0	R/W	0 = Pull EXT_EN low to shutdown external rail when IC enters DPSLP mode. (default) 1 = EXT_EN keeps high when IC enters DPSLP mode.

REG0x21: Reserved

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	1111 1111	R/W	Reserved

REGISTER MAPS (continued)

REG0x22: VIN_VTH_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	SYSMON_VTH	0000	R/W	V_{TH} of the SYSMON Selection Offset = 2725mV Step = 25mV Max = 3100mV SYSMON threshold = 2725mV + DEC(0x22[7:4]) × 25mV
D[3:0]	SYSWARN_VTH	0000	R/W	V_{TH} of the SYSWARN Selection Offset = 2775mV Step = 25mV Max = 3150mV SYSWARN threshold = 2775mV + DEC(0x22[3:0]) × 25mV

REG0x23: VIN_VTH_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	VIN_POK_OV_SET	01	R/W	V_{TH} of the VIN POK_OV Selection 00 = 3.5V 01 = 3.7V (default) 10 = 5.3V 11 = 5.5V
D[5]	VIN_OV_SET	0	R/W	V_{TH} of the VIN_OV Selection 0 = 3.9V (default) 1 = 5.7V
D[4]	VIN_LVL	0	R/W	VIN UVLO Falling Threshold 0 = 2.5V (default) 1 = 3.5V
D[3:2]	Reserved	00	R/W	Reserved
D[1]	POWER_I2C_OFF	0	R/W	0 = PMIC work normally (default) 1 = PMIC shutdown
D[0]	Reserved	0	R/W	Reserved

REG0x24: ADDRESS_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	ADDRESS	00	R	00 = 010 0101 (0x25h) address (default) 01 = 010 0111 (0x27h) address 10 = 110 0111 (0x67h) address 11 = 110 1011 (0x6Bh) address
D[5:0]	Reserved	00 0000	R	Reserved

REG0x25: MANUFACTURE_ID_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	MANUFACTURE ID	0100 0010	R	0x42 for SGMICRO

REG0x26: DEVICE_ID_REG

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE ID	0100 1001	R	0x49 for SGM260421

REGISTER MAPS (continued)

REG0x27: CMI_NUMBER_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CMI_NUMBER	0000 0001	R	OTP Configure Version Code

REG0x28: B1_CFG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	B1_FREQ_SET	01	R/W	Set Buck1 Frequency 00 = 1.5MHz 01 = 2MHz (default) 10 = 2.5MHz 11 = 3MHz
D[5:4]	B1_ILIM_SET	10	R/W	Set Buck1 Valley Current Limit 00 = 3A 01 = 4A 10 = 5A (default) 11 = 6A
D[3:2]	B1_DVS_SET	10	R/W	Set Buck1 DVS Slew Rate 00 = 2.5mV/μs 01 = 5mV/μs 10 = 10mV/μs (default) 11 = 20mV/μs
D[1:0]	B1_SS	11	R/W	Set Buck1 Soft-Start Time 00 = 60μs 01 = 75μs 10 = 115μs 11 = 175μs (default)

REG0x29: B1_CFG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5]	B1_MODE	0	R/W	Set Buck1 mode at factory when GPIO2 is not set as B1/B2 operation mode and voltage select. 0 = Buck mode (default) 1 = Bypass mode
D[4:2]	B1_WAKEUP_DLY_GPIO3_F	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set Buck1 wake-up delay time when exiting SLEEP or DPSLP mode. These bits also set Buck1 wake-up delay time if there is no GPIO3 selecting wake-up delay function.
D[1]	B1_FPWM	0	R/W	0 = PSM (default) 1 = Forced PWM mode This bit is high priority. If both FPWM bit = 1 and LPM bit = 1, the DC/DC enters forced PWM mode.
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x2A: B1_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	01	R/W	Reserved
D[5:0]	B1_VSET0	101000	R/W	Buck1 Output Voltage: Offset = 1.7V Step = 20mV Max = 2.9V 111100 ~111111: 2.9V Output voltage = 1.7V + DEC(0x2A[5:0]) × 20mV

REG0x2B: B1_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	11	R/W	Reserved
D[5:0]	B1_VSET1	101000	R/W	Buck1 Output Voltage: Offset = 1.7V Step = 20mV Max = 2.9V 111100 ~111111: 2.9V Output voltage = 1.7V + DEC(0x2B[5:0]) × 20mV

REG0x2C: B2_CFG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	B2_FREQ_SET	01	R/W	Set Buck2 Frequency 00 = 1.5MHz 01 = 2MHz (default) 10 = 2.5MHz 11 = 3MHz
D[5:4]	B2_ILIM_SET	10	R/W	Set Buck2 Valley Current limit 00 = 2A 01 = 3A 10 = 4A (default) 11 = 5A
D[3:2]	B2_DVS_SET	10	R/W	Set Buck2 DVS Slew Rate 00 = 2.5mV/μs 01 = 5mV/μs 10 = 10mV/μs (default) 11 = 20mV/μs
D[1:0]	B2_SS	11	R/W	Set Buck2 Soft-Start Time 00 = 30μs 01 = 55μs 10 = 115μs 11 = 175μs (default)

REGISTER MAPS (continued)

REG0x2D: B2_CFG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5]	B2_DVS_AT_SLEEP	0	R/W	0 = Buck2 output voltage stays unchanged when PMIC enters SLEEP mode. (default) 1 = Buck2 enters DVS mode adjusting to another output voltage when entering SLEEP mode.
D[4]	B2_DVS_AT_DPSLP	0	R/W	0 = Buck2 output voltage stays unchanged when PMIC enters DPSLP mode. (default) 1 = Buck2 enters DVS mode adjusting to another output voltage when entering DPSLP mode.
D[3:1]	B2_WAKEUP_DLY_GPIO3_F	101	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms (default) 110 = 4ms 111 = 8ms Set Buck2 wake-up delay time when exiting SLEEP or DPSLP mode. These bits also set Buck2 wake-up delay time if there is no GPIO3 selecting wake-up delay function.
D[0]	B2_FPWM	0	R/W	0 = PSM (default) 1 = Forced PWM mode This bit is high priority. If both FPWM bit = 1 and LPM bit = 1, the DC/DC enters forced PWM mode.

REG0x2E: B2_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B2_VSET0	100 0110	R/W	Buck2 Output Voltage: Offset = 0.5V Step = 10mV Max = 1.33V 1001101: 1.27V 1001110: 1.31V 1001111: 1.32V 1010000: 1.33V Output voltage = 0.5V + DEC(0x2E[6:0]) × 10mV (only applicable to less than 1.27V)

REG0x2F: B2_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B2_VSET1	1000 110	R/W	Buck2 Output Voltage: Offset = 0.5V Step = 10mV Max = 1.33V 1001101: 1.27V 1001110: 1.31V 1001111: 1.32V 1010000: 1.33V Output voltage = 0.5V + DEC(0x2F[6:0]) × 10mV (only applicable to less than 1.27V)

REGISTER MAPS (continued)

REG0x30: B2_DVS_VSET_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B2_DVS_VSET	100 0110	R/W	Buck2 Output Voltage in SLEEP/DPSLP: Offset = 0.5V Step = 10mV Max = 1.33V 100 1101: 1.27V 100 1110: 1.31V 100 1111: 1.32V 101 0000: 1.33V Output voltage = 0.5V + DEC(0x30[6:0]) × 10mV (only applicable to less than 1.27V)

REG0x31: B3_CFG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	B3_FREQ_SET	01	R/W	Set Buck3 Frequency 00 = 1.5MHz 01 = 2MHz (default) 10 = 2.5MHz 11 = 3MHz
D[5:4]	B3_ILIM_SET	01	R/W	Set Buck3 Valley Current Limit 00 = 4A 01 = 5A (default) 10 = 6A 11 = 7A
D[3:2]	B3_DVS_SET	10	R/W	Set Buck3 DVS Slew Rate 00 = 5mV/μs 01 = 10mV/μs 10 = 15mV/μs (default) 11 = 20mV/μs
D[1:0]	B3_SS	11	R/W	Set Buck3 Soft-Start Time 00 = 30μs 01 = 55μs 10 = 115μs 11 = 175μs (default)

REGISTER MAPS (continued)

REG0x32: B3_CFG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5]	B3_DVS_AT_SLEEP	0	R/W	0 = Buck3 output voltage stays unchanged when PMIC enters SLEEP mode. (default) 1 = Buck3 enters DVS mode adjusting to another output voltage when entering SLEEP mode.
D[4]	B3_DVS_AT_DPSLP	1	R/W	0 = Buck3 output voltage stays unchanged when PMIC enters DPSLP mode. 1 = Buck3 enters DVS mode adjusting to another output voltage when entering DPSLP mode. (default)
D[3:1]	B3_WAKEUP_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set Buck3 wake-up delay time when exiting SLEEP or DPSLP mode.
D[0]	B3_FPWM	0	R/W	0 = PSM (default) 1 = Forced PWM mode This bit is high priority. If both FPWM bit = 1 and LPM bit = 1, the DC/DC enters forced PWM mode.

REG0x33: B3_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	1	R/W	Reserved
D[6:0]	B3_VSET0	001 1110	R/W	Buck3 Output Voltage: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~1111111: 1.3V Output voltage = 0.5V + DEC(0x33[6:0]) × 10mV

REG0x34: B3_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B3_VSET1	001 1001	R/W	Buck3 Output Voltage: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~1111111: 1.3V Output voltage = 0.5V + DEC(0x34[6:0]) × 10mV

REGISTER MAPS (continued)

REG0x35: B3_VSET2_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B3_VSET2	001 1001	R/W	Buck3 Output Voltage: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~1111111: 1.3V Output voltage = 0.5V + DEC(0x35[6:0]) × 10mV

REG0x36: B3_DVS_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	1	R/W	Reserved
D[6:0]	B3_DVS_VSET0	001 0100	R/W	Buck3 Output Voltage in SLEEP/DPSLP: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~1111111: 1.3V Output voltage = 0.5V + DEC(0x36[6:0]) × 10mV

REG0x37: B3_DVS_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B3_DVS_VSET1	000 1111	R/W	Buck3 Output Voltage in SLEEP/DPSLP: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~ 1111111: 1.3V Output voltage = 0.5V + DEC(0x37[6:0]) × 10mV

REG0x38: B3_DVS_VSET2_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	B3_DVS_VSET2	000 1111	R/W	Buck3 Output Voltage in SLEEP/DPSLP: Offset = 0.5V Step = 10mV Max = 1.3V 1010000 ~1111111: 1.3V Output voltage = 0.5V + DEC(0x38[6:0]) × 10mV

REGISTER MAPS (continued)

REG0x39: B4_CFG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	B4_FREQ_SET	01	R/W	Set Buck4 Frequency 00 = 1.5MHz 01 = 2MHz (default) 10 = 2.5MHz 11 = 3MHz
D[5:4]	B4_ILIM_SET	01	R/W	Set Buck4 Valley Current Limit 00 = 2A 01 = 3A (default) 10 = 4A 11 = 5A
D[3:2]	B4_DVS_SET	10	R/W	Set Buck4 DVS Slew Rate 00 = 2.5mV/μs 01 = 5mV/μs 10 = 10mV/μs (default) 11 = 20mV/μs
D[1:0]	B4_SS	01	R/W	Set Buck4 Soft-Start Time 00 = 30μs 01 = 55μs (default) 10 = 115μs 11 = 175μs

REG0x3A: B4_CFG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5]	B4_MODE	0	R/W	Set Buck4 mode at factory when GPIO4 is not set as B4/L1 operation mode and voltage select. 0 = Buck mode (default) 1 = LDO mode
D[4:2]	B4_WAKEUP_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set Buck4 wake-up delay time when exiting SLEEP or DPSLP mode.
D[1]	B4_FPWM	0	R/W	0 = PSM (default) 1 = Forced PWM mode This bit is high priority. If both FPWM bit = 1 and LPM bit = 1, the DC/DC enters forced PWM mode.
D[0]	Reserved	0	R/W	Reserved

REG0x3B: B4_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B4_SS_LDO	1	R/W	Set Buck4-LDO Soft-Start Time 0 = 55μs 1 = 100μs (default)
D[6:0]	B4_VSET0	000 1010	R/W	Buck4 Output Voltage: Offset = 0.8V Step = 10mV Max = 2.0V 1111000 ~1111111: 2.0V Output voltage = 0.8V + DEC(0x3B[6:0]) × 10mV

REGISTER MAPS (continued)

REG0x3C: B4_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B4_LDO_ILIM_SET	0	R/W	Set Buck4-LDO Current Limit 0 = 400mA (default) 1 = 500mA
D[6:0]	B4_VSET1	000 1010	R/W	Buck4 Output Voltage: Offset = 0.8V Step = 10mV Max = 2.0V 111 1000 ~111 1111: 2.0V Output voltage = 0.8V + DEC(0x3C[6:0]) × 10mV

REG0x3D: B4_VSET2_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	1	R/W	Reserved
D[6:0]	B4_VSET2	000 1010	R/W	Buck4 Buck/LDO Mode Output Voltage: Offset = 0.8V Step = 10mV Max = 2.0V 1111000 ~1111111: 2.0V Output voltage = 0.8V + DEC(0x3D[6:0]) × 10mV

REG0x3E: LDO_CFG_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	L1_ILIM_SET	1	R/W	Set LDO1 Current Limit 0 = 400mA 1 = 500mA (default)
D[6]	L1_SS	1	R/W	Set LDO1 Soft-Start Time 0 = 55μs 1 = 100μs (default)
D[5]	L1_MODE	0	R/W	Set LDO1 mode at factory when GPIO4 is not set as B4/L1 operation mode and voltage select. 0 = LDO mode (default) 1 = LSW mode
D[4]	L2_ILIM_SET	1	R/W	Set LDO2 Current Limit 0 = 400mA 1 = 500mA (default)
D[3]	L2_SS	1	R/W	Set LDO2 Soft-Start Time 0 = 55μs 1 = 100μs (default)
D[2]	L2_MODE	0	R/W	Set LDO2 mode at factory when GPIO6 is not set as L2 operation mode select. 0 = LDO mode (default) 1 = LSW mode
D[1]	L1_OVP_EN	0	RW	0 = Disable LDO1 OVP function (default) 1 = Enable LDO1 OVP function
D[0]	L2_OVP_EN	0	RW	0 = Disable LDO2 OVP function (default) 1 = Enable LDO2 OVP function

REGISTER MAPS (continued)

REG0x3F: LDO_CFG_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	L1_WAKEUP_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set LDO1 wake-up delay time when exiting SLEEP or DPSLP mode.
D[4:2]	L2_WAKEUP_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set LDO2 wake-up delay time when exiting SLEEP or DPSLP mode.
D[1]	EN_DISCHG_L1_OVP	1	RW	0 = Disable discharge resistor when LDO1 OVP 1 = Enable discharge resistor when LDO1 OVP (default)
D[0]	EN_DISCHG_L2_OVP	1	RW	0 = Disable discharge resistor when LDO2 OVP 1 = Enable discharge resistor when LDO2 OVP (default)

REG0x40: L1_VSET0_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5:0]	L1_VSET0	01 0000	R/W	LDO1 Output Voltage: Offset = 1V Step = 50mV Max = 2.7V 100010 ~111111: 2.7V Output voltage = 1V + DEC(0x40[5:0]) × 50mV

REG0x41: L1_VSET1_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:0]	L1_VSET1	01 0000	R/W	LDO1 Output Voltage: Offset = 1V Step = 50mV Max = 2.7V 100010 ~111111: 2.7V Output voltage = 1V + DEC(0x41[5:0]) × 50mV

REGISTER MAPS (continued)

REG0x42: L2_VSET_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	10	R/W	Reserved
D[5:0]	L2_VSET	01 0000	R/W	LDO2 Output Voltage: Offset = 1V Step = 50mV Max = 2.7V 100010 ~111111: 2.7V Output voltage = 1V + DEC(0x42[5:0]) × 50mV

REG0x43: EN_CTRL_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_EN	1	R/W	0 = Buck1 disable 1 = Buck1 enable (default)
D[6]	B2_EN	1	R/W	0 = Buck2 disable 1 = Buck2 enable (default)
D[5]	B3_EN	1	R/W	0 = Buck3 disable 1 = Buck3 enable (default)
D[4]	B4_EN	1	R/W	0 = Buck4 disable 1 = Buck4 enable (default)
D[3]	L1_EN	1	R/W	0 = LDO1 disable 1 = LDO1 enable (default)
D[2]	L2_EN	1	R/W	0 = LDO2 disable 1 = LDO2 enable (default)
D[1:0]	Reserved	01	R/W	Reserved

REG0x44: DISCH_CTRL_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_DISCH	1	R/W	0 = Disable Buck1 discharge resistor 1 = Enable Buck1 discharge resistor (default)
D[6]	B2_DISCH	1	R/W	0 = Disable Buck2 discharge resistor 1 = Enable Buck2 discharge resistor (default)
D[5]	B3_DISCH	1	R/W	0 = Disable Buck3 discharge resistor 1 = Enable Buck3 discharge resistor (default)
D[4]	B4_DISCH	1	R/W	0 = Disable Buck4 discharge resistor 1 = Enable Buck4 discharge resistor (default)
D[3]	L1_DISCH	1	R/W	0 = Disable LDO1 discharge resistor 1 = Enable LDO1 discharge resistor (default)
D[2]	L2_DISCH	1	R/W	0 = Disable LDO2 discharge resistor 1 = Enable LDO2 discharge resistor (default)
D[1:0]	Reserved	01	R/W	Reserved

REGISTER MAPS (continued)

REG0x45: DISCH_CTRL_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	B1_DISCH_SET	01	R/W	Set Buck1 Discharge Resistance. 00 = 5Ω 01 = 10Ω (default) 10 = 20Ω 11 = 40Ω
D[5:4]	B2_DISCH_SET	00	R/W	Set Buck2 Discharge Resistance. 00 = 5Ω (default) 01 = 10Ω 10 = 20Ω 11 = 40Ω
D[3:2]	B3_DISCH_SET	01	R/W	Set Buck3 Discharge Resistance. 00 = 5Ω 01 = 10Ω (default) 10 = 20Ω 11 = 40Ω
D[1:0]	B4_DISCH_SET	01	R/W	Set Buck4 Discharge Resistance. 00 = 5Ω 01 = 10Ω (default) 10 = 20Ω 11 = 40Ω

REG0x46: DISCH_CTRL_REG2

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	L1_DISCH_SET	01	R/W	Set LDO1 Discharge Resistance. 00 = 10Ω 01 = 20Ω (default) 10 = 40Ω 11 = 80Ω
D[5:4]	L2_DISCH_SET	01	R/W	Set LDO2 Discharge Resistance. 00 = 10Ω 01 = 20Ω (default) 10 = 40Ω 11 = 80Ω
D[3:0]	Reserved	0101	R/W	Reserved

REG0x47: LPM_CTRL_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[6]	B2_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[5]	B3_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[4]	B4_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[3]	L1_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[2]	L2_LPM	0	R/W	0 = PSM mode (default) 1 = LPM mode
D[1:0]	Reserved	10	R/W	Reserved

REGISTER MAPS (continued)

REG0x48: SLEEP_CTRL_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_ON_SLEEP	1	R/W	0 = Buck1 turns off when PMIC enters SLEEP mode. 1 = Buck1 stays on and enters LPM mode when PMIC enters SLEEP mode. (default)
D[6]	B2_ON_SLEEP	1	R/W	0 = Buck2 turns off when PMIC enters SLEEP mode. 1 = Buck2 stays on and enters LPM mode when PMIC enters SLEEP mode. (default)
D[5]	B3_ON_SLEEP	1	R/W	0 = Buck3 turns off when PMIC enters SLEEP mode. 1 = Buck3 stays on and enters LPM mode when PMIC enters SLEEP mode. (default)
D[4]	B4_ON_SLEEP	0	R/W	0 = Buck4 turns off when PMIC enters SLEEP mode. (default) 1 = Buck4 stays on and enters LPM mode when PMIC enters SLEEP mode.
D[3]	L1_ON_SLEEP	1	R/W	0 = LDO1 turns off when PMIC enters SLEEP mode. 1 = LDO1 stays on and enters LPM mode when PMIC enters SLEEP mode. (default)
D[2]	L2_ON_SLEEP	1	R/W	0 = LDO2 turns off when PMIC enters SLEEP mode. 1 = LDO2 stays on and enters LPM mode when PMIC enters SLEEP mode. (default)
D[1]	SLEEP_EN	0	R/W	0 = PMIC is in normal mode, if DPSLP_EN is also 0. (default) 1 = PMIC is in SLEEP mode and all rails follow the settings in this register to turn off or enter LPM.
D[0]	Reserved	0	R/W	Reserved

REG0x49: DPSLP_CTRL_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_ON_DPSLP	0	R/W	0 = Buck1 turns off when PMIC enters DPSLP mode. (default) 1 = Buck1 stays on and enters LPM mode when PMIC enters DPSLP mode.
D[6]	B2_ON_DPSLP	0	R/W	0 = Buck2 turns off when PMIC enters DPSLP mode. (default) 1 = Buck2 stays on and enters LPM mode when PMIC enters DPSLP mode.
D[5]	B3_ON_DPSLP	1	R/W	0 = Buck3 turns off when PMIC enters DPSLP mode. 1 = Buck3 stays on and enters LPM mode when PMIC enters DPSLP mode. (default)
D[4]	B4_ON_DPSLP	1	R/W	0 = Buck4 turns off when PMIC enters DPSLP mode. 1 = Buck4 stays on and enters LPM mode when PMIC enters DPSLP mode. (default)
D[3]	L1_ON_DPSLP	1	R/W	0 = LDO1 turns off when PMIC enters DPSLP mode. 1 = LDO1 stays on and enters LPM mode when PMIC enters DPSLP mode. (default)
D[2]	L2_ON_DPSLP	1	R/W	0 = LDO2 turns off when PMIC enters DPSLP mode. 1 = LDO2 stays on and enters LPM mode when PMIC enters DPSLP mode. (default)
D[1]	DPSLP_EN	0	R/W	0 = PMIC is in normal mode, if SLEEP_EN is also 0. (default) 1 = PMIC is in DPSLP mode and all rails follow the settings in this register to turn off or enter LPM.
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x4A: B1_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B1_ON_DLY	0100	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4A[7:4]) × 0.5ms Set Buck1 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	B1_OFF_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set Buck1 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	0	R/W	Reserved

REG0x4B: B2_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B2_ON_DLY	0100	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4B[7:4]) × 0.5ms Set Buck2 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	B2_OFF_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set Buck2 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	0	R/W	Reserved

REG0x4C: B3_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B3_ON_DLY	0010	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4C[7:4]) × 0.5ms Set Buck3 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	B3_OFF_DLY	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set Buck3 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	1	R/W	Reserved

REGISTER MAPS (continued)

REG0x4D: B4_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	B4_ON_DLY	0011	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4D[7:4]) × 0.5ms Set Buck4 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	B4_OFF_DLY	000	R/W	000 = 0ms (default) 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms 110 = 4ms 111 = 8ms Set Buck4 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	1	R/W	Reserved

REG0x4E: L1_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	L1_ON_DLY	0001	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4E[7:4]) × 0.5ms Set LDO1 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	L1_OFF_DLY	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set LDO1 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	0	R/W	Reserved

REG0x4F: L2_TIME_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	L2_ON_DLY	0001	R/W	Offset = 0ms Step = 0.5ms Delay time = DEC(0x4F[7:4]) × 0.5ms Set LDO2 turn-on delay time between the SYSMON and when it starts to turn on.
D[3:1]	L2_OFF_DLY	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set LDO2 turn-off delay time when entering SLEEP or DPSLP mode, or PWRDIS.
D[0]	Reserved	0	R/W	Reserved

REGISTER MAPS (continued)

REG0x50: WAKEUP_DLY_GPIO3_REG0

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	B1_WAKEUP_DLY_GPIO3_H	101	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms (default) 110 = 4ms 111 = 8ms Set Buck1 wake-up delay time when exiting SLEEP or DPSLP mode.
D[4:2]	B1_WAKEUP_DLY_GPIO3_L	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set Buck1 wake-up delay time when exiting SLEEP or DPSLP mode.
D[1:0]	Reserved	00	R	Reserved

REG0x51: WAKEUP_DLY_GPIO3_REG1

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	B2_WAKEUP_DLY_GPIO3_H	100	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms (default) 101 = 2ms 110 = 4ms 111 = 8ms Set Buck2 wake-up delay time when exiting SLEEP or DPSLP mode.
D[4:2]	B2_WAKEUP_DLY_GPIO3_L	101	R/W	000 = 0ms 001 = 0.25ms 010 = 0.5ms 011 = 0.75ms 100 = 1ms 101 = 2ms (default) 110 = 4ms 111 = 8ms Set Buck2 wake-up delay time when exiting SLEEP or DPSLP mode.
D[1:0]	Reserved	00	R	Reserved

REG0x52: PWRDIS_REG

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R	Reserved
D[2:0]	PWRDIS_DLY_TIME	000	R/W	PMIC will enter power-off sequence with the delay time after the high level detected PWRDIS signal. 000 = 0ms (default) 001 = 0.5ms 010 = 1.0ms 011 = 2.0ms 100 = 4.0ms 101 = 8.0ms 110 = 16ms 111 = disable PWRDIS function

APPLICATION INFORMATION

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

1. Bypass VIN_Bx pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN_Bx pin on the top layer eliminates the need for vias. Refer to the pin descriptions for the specific VIN_Bx and PGNDx pins of each buck converter.

2. Keep the switch node trace between each SW_Bx pin and the inductor as short as possible. For optimal routing, run this trace between the pads of the input capacitor. Using 0805-sized input capacitors is recommended. Avoid placing sensitive analog signal traces near these high-frequency, high dV/dt nodes to minimize noise interference.

3. Position the LDO input capacitor near the VIN_LDO1/AVIN pin, ensuring a direct connection to VIN_LDO1/AVIN and AGND on the top layer for optimal performance.

4. Place the Buck output capacitors close to the inductor, ensuring direct connections with short, wide traces to both the inductor and ground plane. The output capacitor ground should be tightly linked to the input capacitor ground. Use multiple vias if necessary to maintain low impedance.

5. Each FB_Bx pin should be Kelvin connected to its output capacitor using the shortest possible trace while maintaining adequate distance from switching nodes to minimize noise injection. The IC regulates the output voltage based on this Kelvin connection.

6. The PGNDx and AGND pins must be electrically connected. Since the AGND plane serves as the ground for analog, digital, and LDO circuits, full isolation from other PCB grounds is not required. However, ensure that Buck converter switching currents do not flow through the analog ground connections to prevent interference. Connect the AGND and PGND pins to the ground planes using vias placed next to the bypass capacitors for optimal grounding.

7. Ensure that all open-drain outputs have appropriate pull-up resistors.

8. Figure 19 illustrates the recommended power and signal connections, as well as the routing beneath the IC. For a detailed routing example, refer to the SGM260421 evaluation kit.

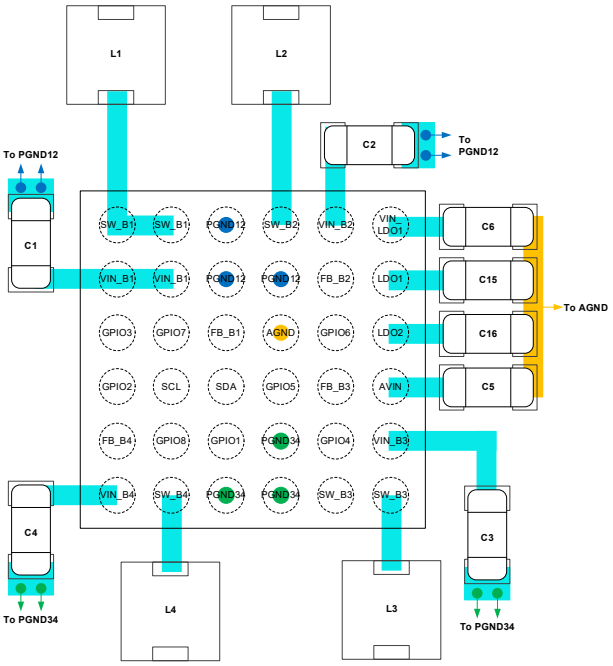


Figure 19. Recommended Layout

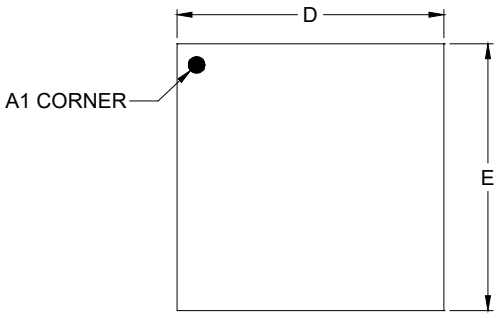
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

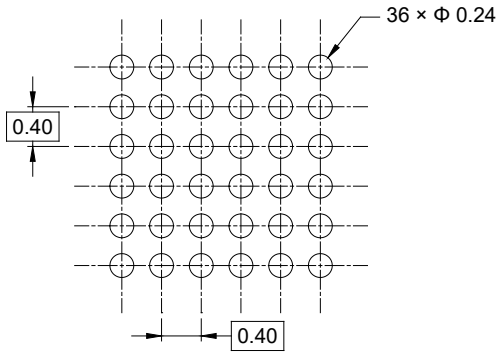
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

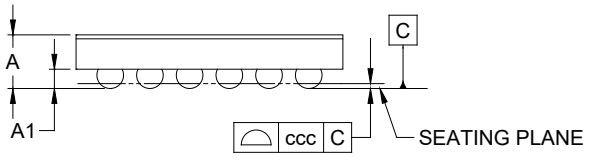
WLCSP-2.69×2.69-36B



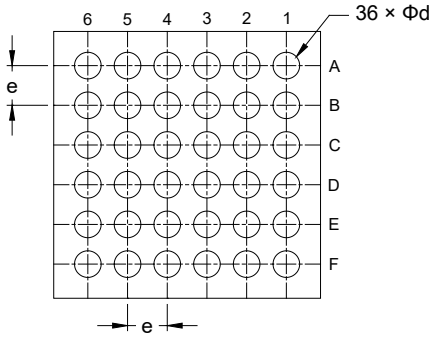
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



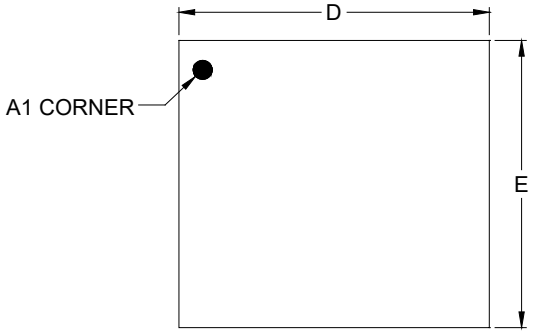
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.585
A1	0.174	-	0.214
D	2.658	-	2.718
E	2.658	-	2.718
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

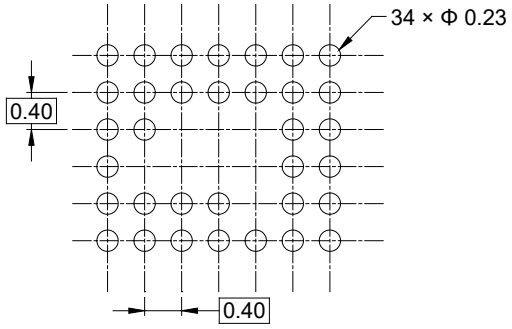
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

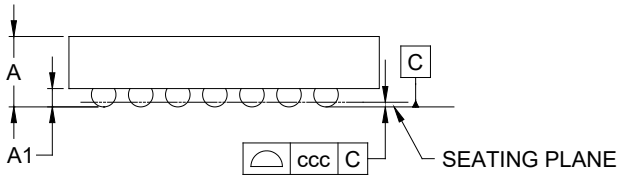
FOCSP-3.35×3.1-34B



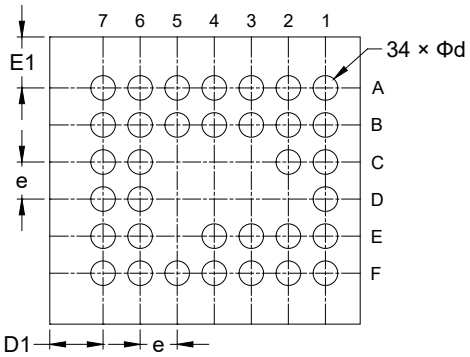
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



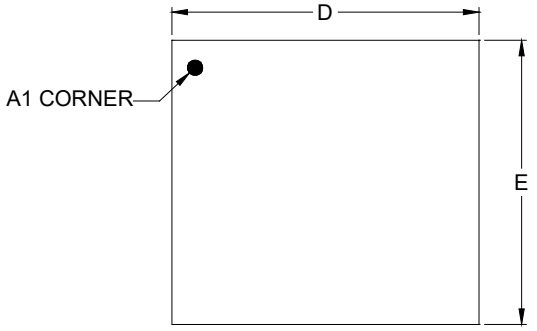
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.810
A1	0.178	-	0.218
D	3.300	-	3.400
D1	0.575 REF		
E	3.050	-	3.150
E1	0.550 REF		
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

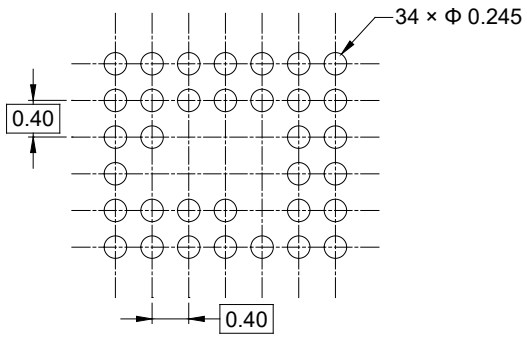
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

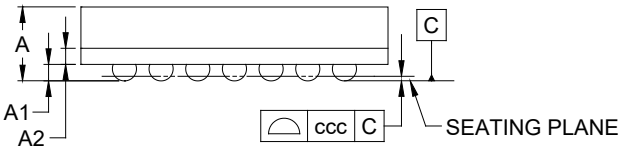
TBGA-3.35×3.1-34B



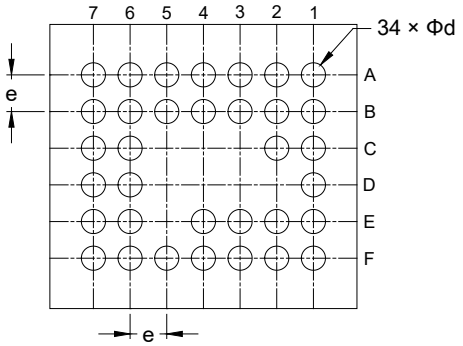
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



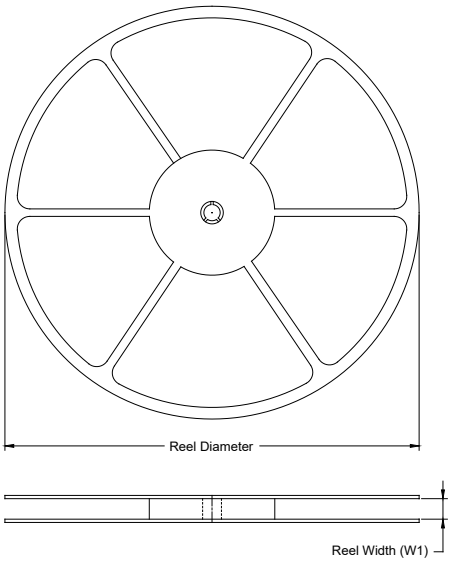
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.900
A1	0.130	-	0.230
A2	0.176 REF		
D	3.250	-	3.450
E	3.000	-	3.200
d	0.213	-	0.313
e	0.400 BSC		
ccc	0.080		

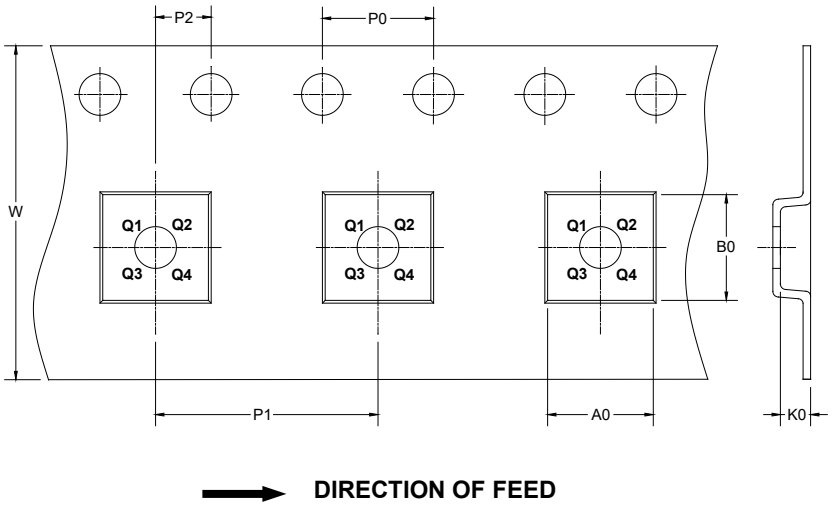
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



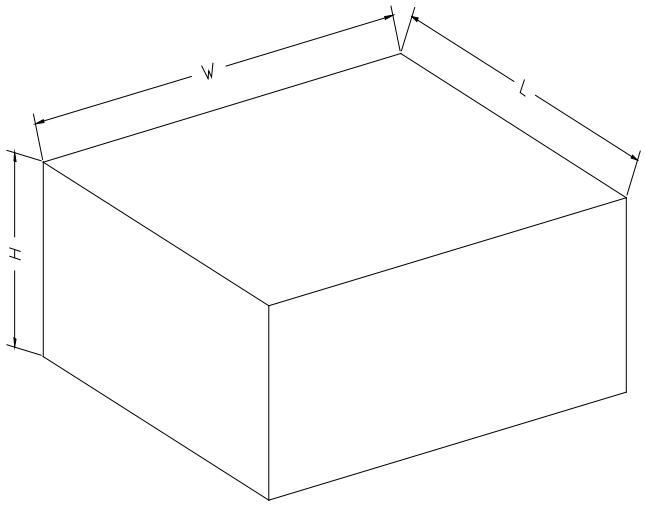
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.69×2.69-36B	7"	9.5	2.90	2.90	0.75	4.0	4.0	2.0	8.0	Q1
FOCSP-3.35×3.1-34B	13"	12.4	3.28	3.54	0.96	4.0	8.0	2.0	12.0	Q2
TBGA-3.35×3.1-34B	13"	12.4	3.40	3.65	1.15	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002