SGM61282
8A, 23V, 500kHz Synchronous Buck Converter with 3.3V LDO

GENERAL DESCRIPTION

The SGM61282 is a constant on-time (COT) mode synchronous Buck converter that integrates low R_{DSON} power MOSFETs. The main control loop of SGM61282 uses COT mode control, which can provide very fast transient response. With internal low R_{DSON} switches, the SGM61282 is capable of delivering 8A output current over a wide input voltage range. The output voltage of SGM61282-3.3 is fixed to 3.3V.

The SGM61282 is available in a Green space-saving UTQFN-3×3-23L package.

APPLICATIONS

Industrial and Commercial Low Power Systems
Laptop, Notebook Computers
LCD Monitors and TVs
Green Electronics/Appliances
DSP, FPGA and ASIC Power Supplies

FEATURES

- **8A Output Current with Input Voltage Range:**
  - **SGM61282-3.3: V_{IN} = 4.5V to 23V**
- **Fixed Output Voltage:**
  - **SGM61282-3.3: 3.3V**
- **Constant On-Time Control**
- **Fully Support All MLCC Output Capacitors**
- **Integrated Power MOSFET Switches:**
  26mΩ (Upper) and 12mΩ (Lower)
- **Fixed 500kHz Switching Frequency for CCM**
- **LDO Output Voltage 3.3V with 100mA Current Supply**
- **Output Soft-Start Function**
- **Built-in Output Discharge Function**
- **Cycle-by-Cycle Over-Current Protection**
- **Input Under-Voltage Lockout**
- **Thermal Shutdown Protection**
- **Output Over/Under-Voltage Protection**
- **Available in a Green UTQFN-3×3-23L Package**

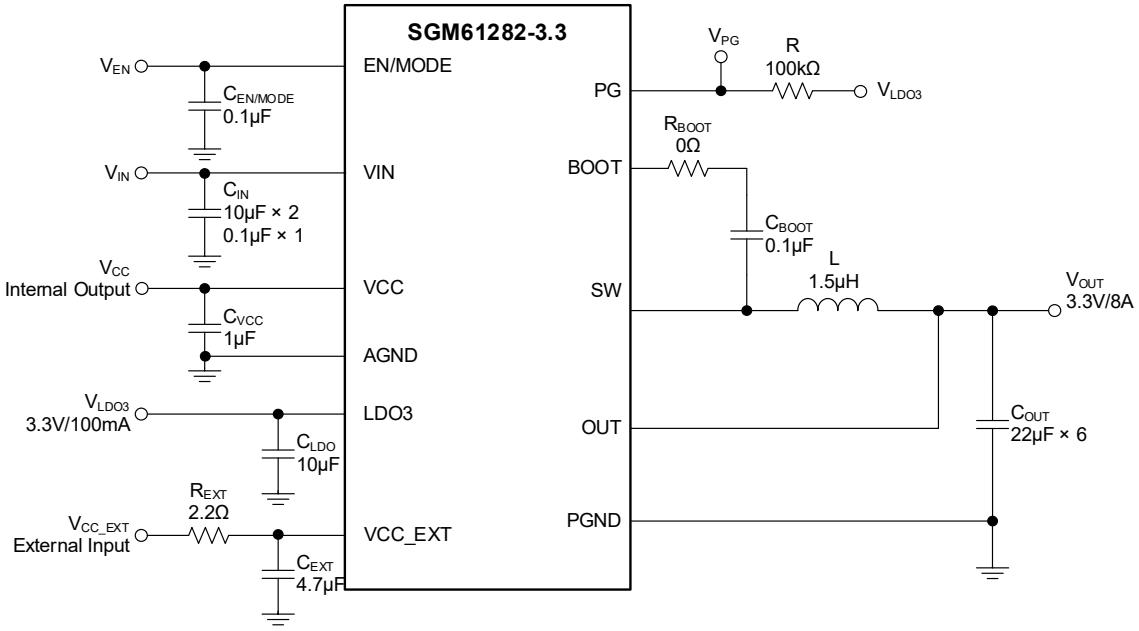


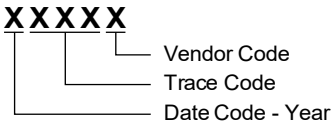
Figure 1. Typical Application Circuit for SGM61282-3.3

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61282-3.3	UTQFN-3×3-23L	-40℃ to +125℃	SGM61282-3.3XUUI23G/TR	0H5 XUUI23 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... -0.3V to 28V
Enable Pin Voltage, $V_{EN/MODE}$ ..... -0.3V to 28V
FB Pin Voltage, V_{FB} ..... -0.3V to 6V
VOUT Pin Voltage, V_{OUT}
SGM61282-3.3 ..... -0.3V to 4.5V
Switch Voltage, SV ..... -0.3V to (V_{IN} + 0.3V)
< 10ns ..... -5V to 28V
BOOT Voltage, V_{BS} ..... (V_{SW} - 0.3V) to (V_{SW} + 6V)
Other I/O Pin Voltages ..... -0.3V to 6V
Package Thermal Resistance (1)
UTQFN-3×3-23L, θ_{JA} ..... 43.1℃/W
UTQFN-3×3-23L, θ_{JB} ..... 4.8℃/W
UTQFN-3×3-23L, $\theta_{JC(TOP)}$ ..... 20.4℃/W
UTQFN-3×3-23L, $\theta_{JC(BOT)}$ ..... 3.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. Reference to JEDEC JESD-51 standard.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage, V_{IN}
SGM61282-3.3 ..... 4.5V to 7.5V (1)
SGM61282-3.3 ..... 7.5V to 23V
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:

1. It is not suggested to be used in this condition. When it works in large duty, abrupt load variations can destabilize its operating characteristics. It may cause UVLO or retry after OC.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

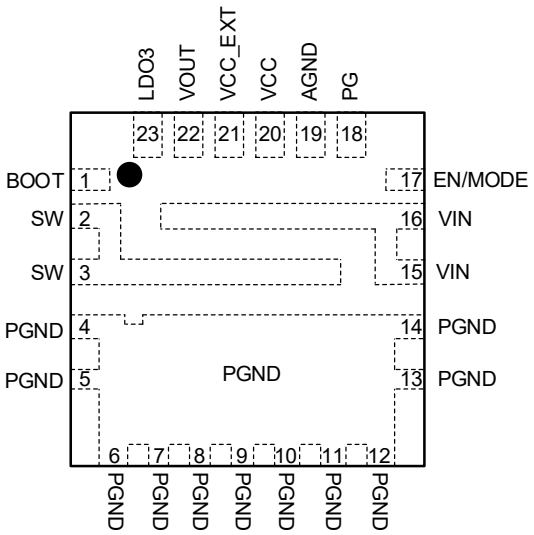
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM61282-3.3 (TOP VIEW)



UTQFN-3×3-23L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	I	Bootstrap Pin. Supply upper gate driver. A high quality and low ESR ceramic capacitor 0.1μF ceramic capacitor between BOOT pin and SW pin. Ensure the 0.1μF ceramic capacitor is placed near the IC.
2, 3	SW	O	Internal Switches Output. Connect these two pins to the output inductor and away from sensitive traces and signals.
4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	PGND	G	Power Ground. Ground returns from the low-side power MOSFET and its driver. Solder directly to a large PCB PGND plane and connect thermal vias under the PGND pins to minimize parasitic and thermal resistance.
15, 16	VIN	P	Power Supply Input Pin. VIN pins are used to supply the internal bias voltage, VCC and LDO. Use wide PCB traces and multiple vias for connections. Apply at least two layers for the input trace. Ceramic capacitors (C = 10μF/0805 × 2ea + 0.1μF/0603 × 1ea) must be connected as close as possible to the VIN pin to the PGND pin.
17	EN/MODE	I	Enable Control. Pull this pin high to turn on the Buck converter. Logic low ($V_{EN/MODE}$ < 0.3V) shuts down the converter. Do not leave this pin floating. EN/MODE pin voltage between 0.88V to 1.5V set in audible noise cancellation or EN/MODE pin voltage between 2.3V to VIN set in PSM.
18	PG	O	Power Good Indicator. Open-drain output when the output voltage is higher than 89%. An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor is from 10kΩ to 100kΩ.
19	AGND	G	Analog Ground. Analog ground of the Buck converter. AGND must be connected to the PGND plane through a single point.
20	VCC	O	5.5V Linear Regulator Output for Internal Control Circuit. A capacitor 1μF (TYP) should be connected to AGND. Do not connect externally to the load.
21	VCC_EXT	I	External Voltage Input for VCC. If VCC_EXT pin is connected to the external bias voltage 5.25V, the internal LDO for VCC can be replaced by VCC_EXT and the power consumption is further reduced. An RC filter (R = 2.2Ω/0603 and C = 4.7μF/0603) between bias voltage 5V and VCC_EXT pin is necessary.
22	VOUT	O	Output Voltage Sense Pin. Directly connect this pin to the DC/DC output voltage point. The pin also provides the bypass input for LDO3 output.
23	LDO3	O	3.3V LDO Output. Decouple using at least a 4.7μF ceramic capacitor to PGND. This pin is also capable sourcing 100mA current for external load. When the VIN voltage exceeds the UVLO rising threshold, the internal 3.3V LDO is enabled. Additionally, after the soft-start cycle is completed, LDO3 switches to the VOUT pin.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V. The typical values are referenced to T_A = T_J = +25℃. Both minimum and maximum values are referenced to T_A = T_J = -40℃ to +125℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
VIN Input Voltage Range	V_{IN}		4.5		23	V
VIN Input Shutdown Current	I_{SD_VIN}	$V_{EN/MODE}$ = 0V		72		μA
VIN Input Quiescent Current	I_{Q_VIN}	$V_{EN/MODE}$ = 5V, switch-off	105	145	185	μA
Under-Voltage Lockout						
Input UVLO Threshold	V_{UVLO}	SGM61282-3.3V, rising V_{IN}	3.8	4.3	4.6	V
UVLO Hysteresis	V_{HYS}			0.25		V
Logic Input Threshold						
EN Input Low Threshold	V_{EN_LTH}	Shutdown	0.3	0.55	0.8	V
EN Input High Threshold	V_{EN_HTH}	Enable	0.4	0.64	0.88	V
Audible Noise Cancellation	V_{EN_H1}	Audible noise cancellation			1.5	V
PSM	V_{EN_H2}	Power saving mode	2.3			V
EN Input Current	I_{EN}	$V_{EN/MODE}$ = 0.1V	0		4	μA
Output Voltage						
Output Voltage	V_{OUT}	T_A = T_J = +25℃	3.201	3.3	3.399	V
Discharge Pull Low Resistance	R_{DIS}	$V_{EN/MODE}$ = 0V, T_A = T_J = +25℃	30	50	100	Ω
Soft-Start						
Soft-Start Time	t_{SS}	From V_{EN_HTH} to PG release to High	1.4	2.5	3.6	ms
Output Rising Time	t_R	10% × V_{OUT} to 90% × V_{OUT}		0.9		ms
Power Switch						
Upper Switch-On Resistance	R_{DSON_HS}			26		mΩ
Lower Switch-On Resistance	R_{DSON_LS}			12		mΩ
Current Limit						
Lower FET Valley Current Limit	I_{LIM_LS}	T_A = T_J = +25℃	8	12	16	A
Switching Frequency						
Switching Frequency	f_{SW}	CCM mode	350	500	650	kHz
Timer Control						
Minimum On-Time	t_{ON_MIN}	V_{IN} = V_{IN_MAX}		88		ns
Minimum Off-Time	t_{OFF_MIN}			145		ns
Audible Noise Cancellation						
Operation Period				29		μs
Output Over-Voltage Protection (OVP)						
Output Over-Voltage Threshold	O_{VP_TH}	V_{FB}/V_{FF}/V_{OUT} rising	114	120	126	%
Output Over-Voltage Deglitch Time (1)	t_{OVP_DEG}			10		μs
Output Under-Voltage Protection (UVP)						
Output Under-Voltage Falling Threshold	U_{VP_FTH}	V_{FB}/V_{FF}/V_{OUT} falling	60	65	70	%
Output Under-Voltage Rising Threshold	U_{VP_RTH}	V_{FB}/V_{FF}/V_{OUT} rising		70		
Output Under-Voltage Deglitch Time (1)	t_{UVP_DEG}	FB forced below UVP_FTH threshold		10		μs
UVP Blanking Time	t_{UVP_BLANK}	From V_{EN_HTH}	1.4	2.5	3.6	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V. The typical values are referenced to T_A = T_J = +25℃. Both minimum and maximum values are referenced to T_A = T_J = -40℃ to +125℃, unless otherwise specified.)

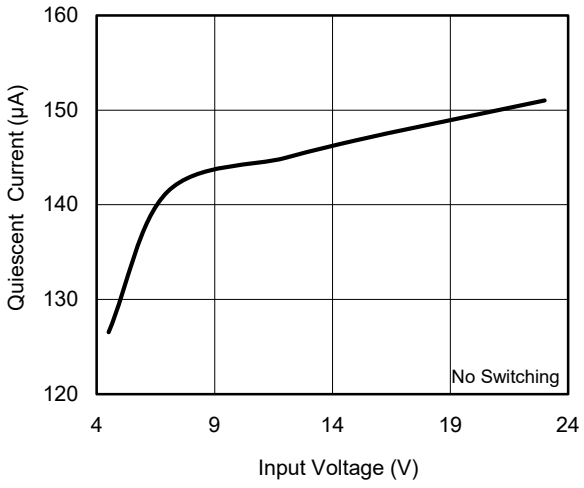
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Good Output						
PG Threshold	PG_{TH_LtoH}	$V_{FB}/V_{FF}/V_{OUT}$ rising	84	89	94	%
PG Hysteresis	PG_{TH_HtoL}			12		%
PG Deglitch Time (1)	t_{PG_DEG}	PG active after UVP blanking time		20		μs
LDO Regulator and Bypass Switch						
LDO Output Voltage	V_{LDO3}	$V_{EN/MODE}$ = 0V, T_A = T_J = +25℃	3.15	3.3	3.45	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO} = 20mA, $V_{EN/MODE}$ = 0V		200		mV
LDO Output Current Limit	$LDO_{\_ILM}$		120	200	300	mA
LDO Bypass MOS Switch R_{ON}	R_{ON_LDOBP}			0.9		Ω
LDO Bypass MOS Turn-on Threshold	V_{TH_LDOBP}			2.9		V
LDO Bypass Switch-over Hysteresis			0.3	0.4	0.5	V
VCC Regulator and Bypass Switch						
VCC Regulator Voltage	V_{CC}	Internal regulator		5.5		V
VCC Bypass MOS Switch R_{ON}	R_{ON_VCCBP}			4		Ω
VCC Bypass MOS Turn-on Threshold	V_{TH_VCCBP}	T_A = T_J = +25℃	4.55	4.9	5.25	V
VCC Bypass Switch-Over Hysteresis		T_A = T_J = +25℃	0.1	0.2	0.3	V
Thermal Protection						
OTP Shutdown Threshold	T_{SD}			150		℃
OTP Hysteresis	T_{HYS}			20		℃

NOTE: 1. Guaranteed by design.

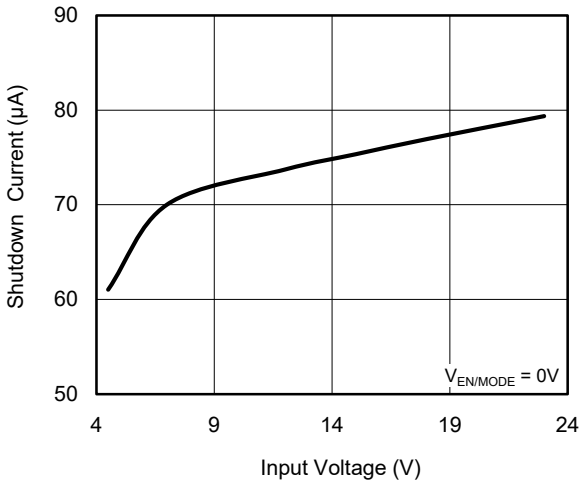
TYPICAL PERFORMANCE CHARACTERISTICS

L = 1.5μH, V_{OUT} = 3.3V, $V_{EN/MODE}$ = 5V, PSM, unless otherwise noted.

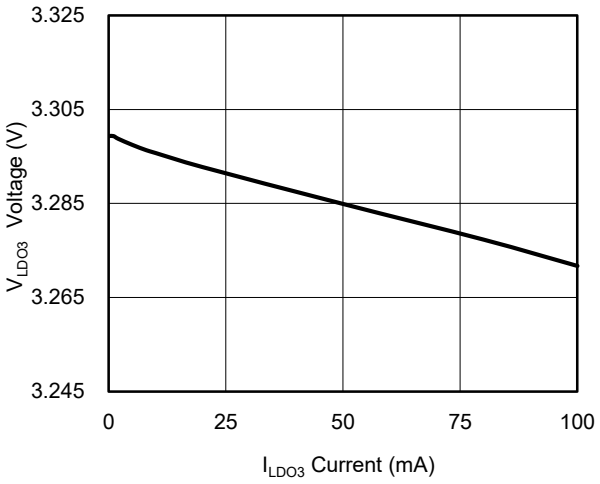
Quiescent Current vs. Input Voltage



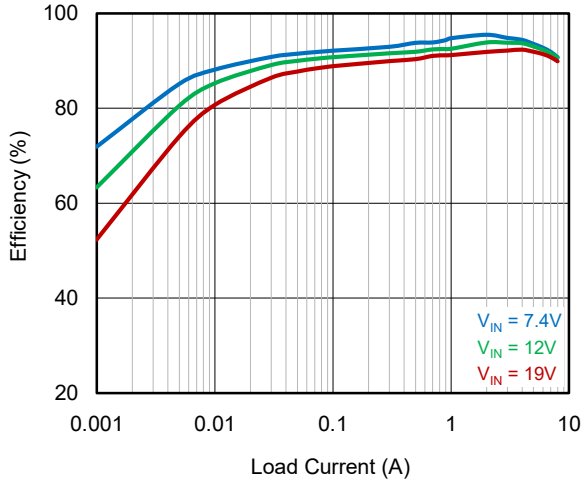
Shutdown Current vs. Input Voltage



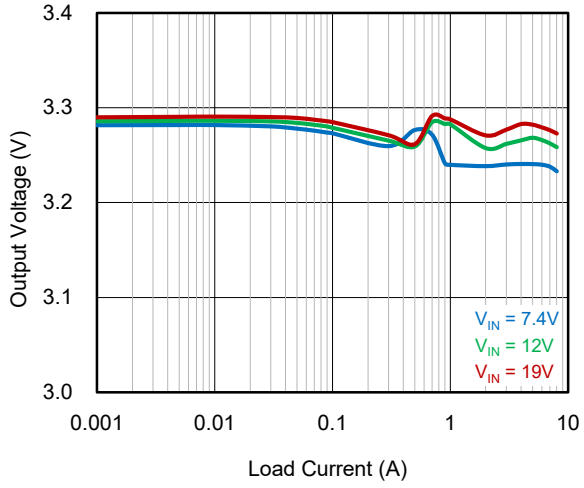
V_{LDO3} Voltage vs. I_{LDO3} Current



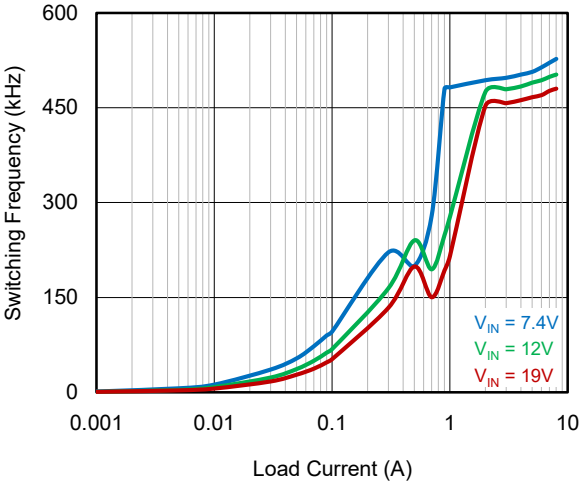
Efficiency vs. Load Current



Output Voltage vs. Load Current

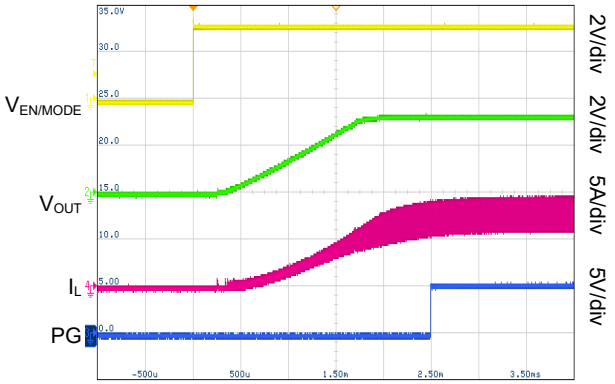


Switching Frequency vs. Load Current



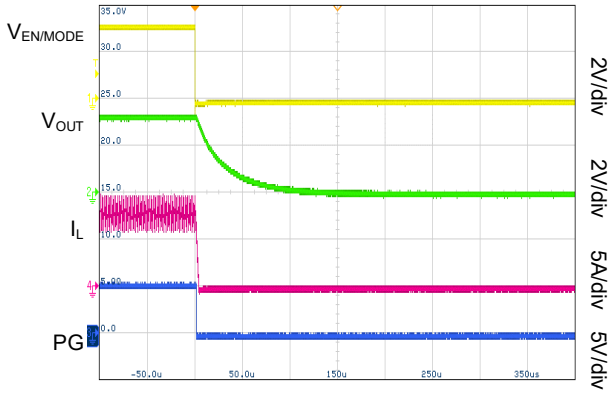
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power On from EN/MODE



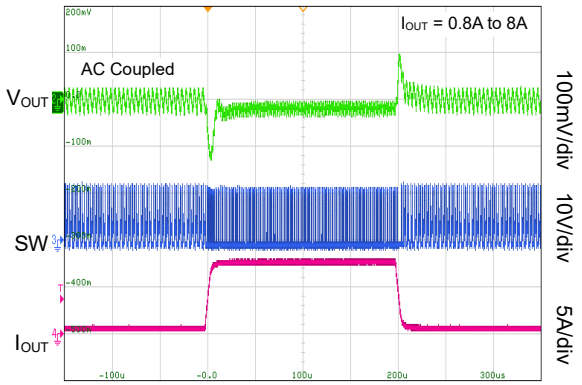
Time (500μs/div)

Power Off from EN/MODE



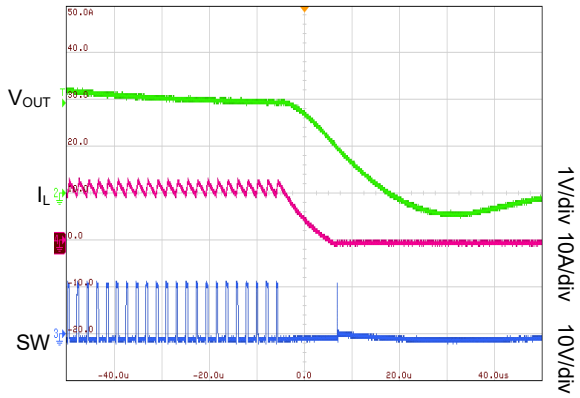
Time (50μs/div)

Load Transient Response



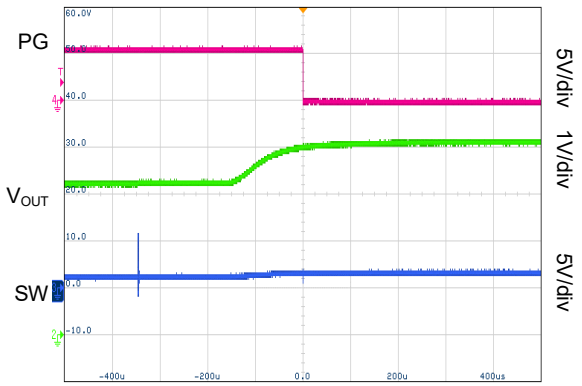
Time (50μs/div)

Over-Current Limit



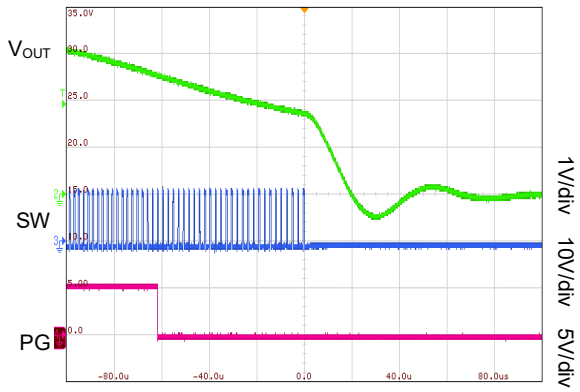
Time (10μs/div)

VOUT OVP with Latched Mode



Time (20μs/div)

VOUT UVP with Latched Mode



FUNCTIONAL BLOCK DIAGRAM

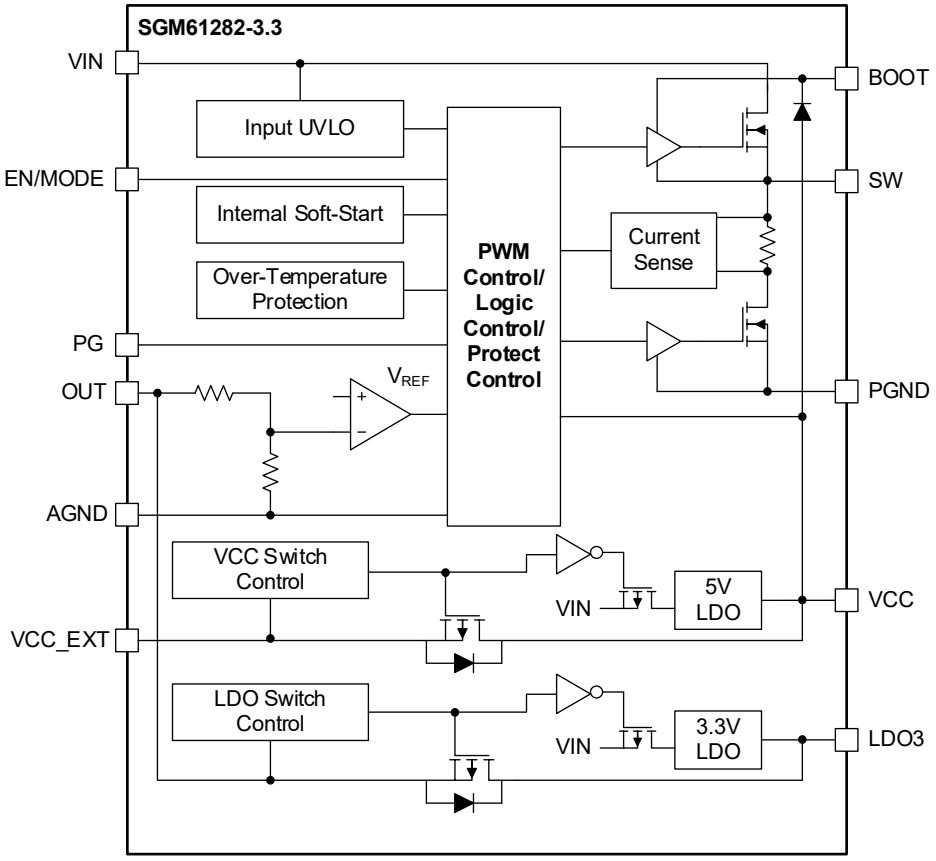


Figure 2. Block Diagram for SGM61282-3.3

DETAILED DESCRIPTION

The SGM61282 is a wide input voltage synchronous Buck converter with constant on-time (COT) control and integrated low R_{DSON} power MOSFETs. The COT control loop allows stable operation and fast transient response even with low ESR output ceramic capacitors and no complicated external compensation. It can deliver 8A output current due to its integrated synchronous Buck converter with low R_{DSON} switches. The input range for SGM61282-3.3 is from 4.5V to 23V.

The proprietary technology used in the COT control for this device, provides excellent load and line regulation and very fast transient response along with high flexibility.

Transient response is almost instantaneous because the COT is not clock-based unlike other methods using clocked PWM where the loop reacts to the events in the next clock cycles. Therefore, the inductor current reacts to deviations immediately to keep the output in regulation.

This device can employ both low ESR (like POSCAP or SP-CAP) and ultra-low ESR ceramic capacitors for output capacitance.

A linear regulator with 100mA output capacity is provided in the device. If V_{OUT} exceeds 3.1V (SGM61282-3.3), the regulator source will automatically switch from the input to the output through OUT pin to minimize the losses.

Under-Voltage Lockout Protection

The input voltage (V_{IN}) is continuously monitored and if it falls below the under-voltage lockout falling threshold, the device shuts down. The UVLO is necessary to avoid device malfunction due to low supply voltage such as insufficient gate voltage for turning the power switches to fully on-state. The UVLO is non-latching and if V_{IN} exceeds the under-voltage lockout rising threshold (if EN/MODE is logic high), device will exit shutdown and resume switching.

Enable/Disable and Mode Selection

The EN/MODE pin can be used to enable or shutdown the device and select the mode. If EN/MODE pin is a logic low voltage (below 0.55V), device will shut down. If EN/MODE pin is a logic high (above 0.64V) and V_{IN} > V_{UVLO}, the device will be enabled.

This pin is also used to select the audible noise cancellation or power saving mode (PSM). If the EN/MODE pin voltage is in the 0.88V to 1.5V range, the device is allowed to enter audible noise cancellation. In audible noise cancellation, the minimum switching frequency is kept at 34kHz. So audible noise cancellation could prevent the audio noise. If the EN/MODE pin voltage is higher than 2.3V, the device goes into PSM to get higher efficiency.

The LDO output and VCC are in on-state as long as V_{IN} > V_{UVLO}. See Table 1 for the SGM61282 power logic.

Table 1. SGM61282 Power Logic

PN.	EN/MODE	VCC	OUT	LDO3
SGM61282-3.3	1	1	1	1
	0	1	0	1

NOTE: 1: Input High Threshold, 0: Input Low Threshold.

External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

The high-side (HS) switch gate driver needs a voltage higher than VIN to turn on the gate of the high-side NMOSFET switch (for example, 5V + VIN or higher). The external bootstrap capacitor (C_{BOOT}) is used to provide this higher voltage for supplying the HS gate driver. C_{BOOT} is charged through the internal bootstrap diode from VCC when the low-side (LS) switch turns on and SW node is at around 0V. When the LS switch turns off and HS switch turns on, the SW voltage will rise to the VIN rail voltage and the C_{BOOT} voltage will supply the HS driver.

Refer to Figure 3 for C_{BOOT} and R_{BOOT} combinations. Use a 0.1μF ceramic capacitor (C_{BOOT}) with lower ESR and a series 0Ω resistor (R_{BOOT}) is suggested to be less than 10Ω) between the BST and the SW pins for bootstrapping.

The R_{BOOT} helps to control the turn-on time of the HS switch and is good to compromise the switching loss and the EMI radiation. The gate driver is designed for fast turn-on and minimal switching loss (that is, for good efficiency). But the additional resistance of the R_{BOOT} can slow down the turn-on (V_{SW} rising) to reduce the EMI at the expense of small increase in the switching loss due to the longer turn-on time of the HS switch.

DETAILED DESCRIPTION (continued)

Soft-Start Time

An internal 0.9ms (TYP) soft-start ramp circuit is implemented to gradually increase the PWM reference voltage for output regulation, in order to limit the startup inrush current from the source and to prevent unwanted over-current protection trips during power-up. This timer starts when EN/MODE goes high (if V_{IN} > V_{UVLO}) or when VIN exceeds the under-voltage lockout rising threshold if EN/MODE is already high.

LDO3 Linear Regulator

The LDO3 (SGM61282-3.3) can deliver 100mA to external loads. The LDO should be decoupled with at least 10μF ceramic capacitor. When VOUT exceeds above 3.1V, the source of the LDO will automatically switch from VIN to OUT by an internal MOSFET to minimize LDO losses.

VCC Linear Regulator

VCC regulator is powered from VIN to power the internal circuitry and the gate drivers. It should be decoupled with a 1μF ceramic capacitor close to the device.

Power Good Output (PG)

The PG pin is an open-drain output with a pull-up resistor which will go to logic high if the output voltage is near its expected value. It is recommended to connect a 100kΩ pull-up resistor to a high rail which is not larger than 5V. VPG will be pulled low, if VOUT drops below 79% (TYP) of its nominal value and will go high if it exceeds 90% of the nominal regulation value. PG is held low during soft-start state. To avoid false signaling, PG responds with a 20μs delay and changes state if at the end of this delay, the new state is still valid.

Output Over-Voltage Protection and Under-Voltage Protection

An over-voltage protection (OVP) is triggered if the V_{OUT} exceeds the over-voltage threshold (above regulation) for about 10μs or longer. Upon OVP trip, the HS switch remains off and the LS switch remains on until the inductor current drops to zero and then the device will shut down.

Output voltage is also protected against under-voltage protection (UVP). If the output voltage falls and remains below the under-voltage threshold for about 10μs, the device shuts down. After OVP or UVP, the device will shut down in latch-off mode and will not restart automatically. An EN toggle or VIN power cycling is needed to restart the device.

Power-Saving Mode (PSM)

In light loads, the SGM61282 can enter the PSM mode to keep the efficiency high. In PSM, upon detection of zero inductor current, the LS switch turns off and the output capacitor will take longer time to discharge (t_{OFF} extends) until the VOUT (or V_{FB}) drops to the level needed to begin a new cycle (HS turn on or t_{ON} pulse).

Output Current Limit

A cycle-by-cycle valley current detection is implemented to limit the output current. During t_{OFF} portion of each cycle (in which LS is conducting), the current of the synchronous rectifier (LS switch) is monitored by measuring its drain-to-source voltage that is proportional to its current. This measurement is temperature compensated for better accuracy. If the valley current exceeds the threshold, the one-shot timer that produces the constant on-time (for the t_{ON} period) will be disabled and not allowed until the inductor current, which is going through LS during t_{OFF}, drops below the valley current limit. During current limiting, the output voltage will drop because the required load current is not supplied by the inductor. If the output voltage drops below the output UVP level (see Output Over/Under-Voltage Protection section), the device will shut down and stop switching.

Audible Noise Cancellation

To avoid acoustic noise when the PSM frequency drops below audible range (20kHz), the audible noise cancellation can be activated by bringing the EN voltage between 0.88V and 1.5V. In this mode, the device could keep the minimum switching period to about 29μs (about 33.3kHz), which is called audible noise cancellation. This mode can keep the switching frequency above the hearing range even in no load condition.

Thermal Shutdown

The junction temperature (T_J) is constantly monitored for over-temperature protection (OTP). If T_J exceeds the T_{SD} threshold (+150°C, TYP for SGM61282-3.3), the device shuts down to avoid damage. OTP is a latch-off mode protection and an EN toggle or V_{IN} power cycling is needed to restart the device.

APPLICATION INFORMATION

Typical Application

The schematic of a typical application circuit that is used for SGM61282-3.3 evaluation module is given in Figure 2.

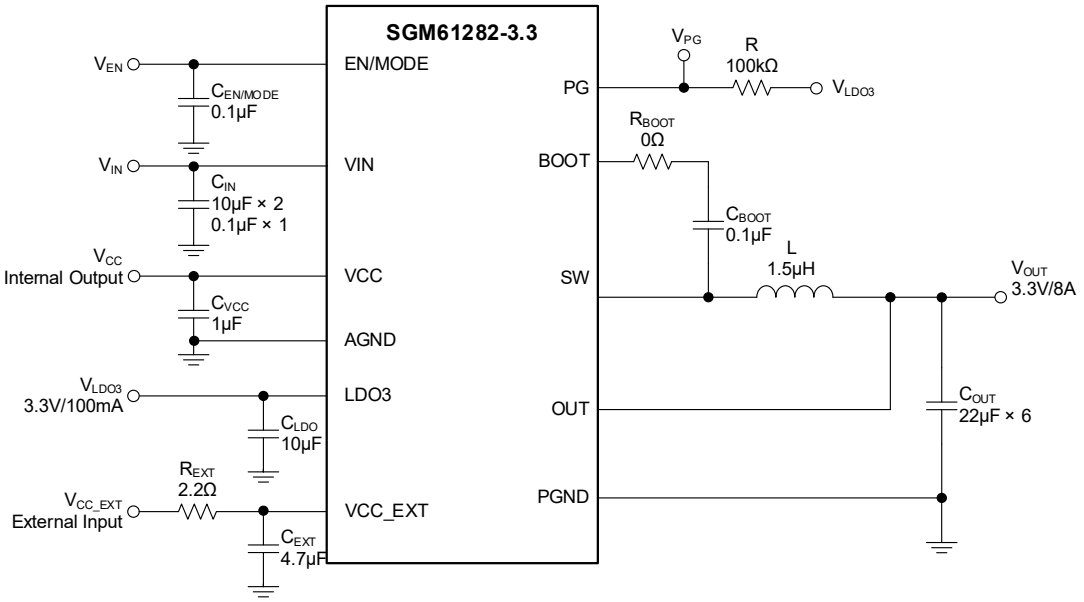


Figure 3. Typical Application Circuit for SGM61282-3.3

Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	4.5V to 23V
Output Voltage	3.3V
Output Current (MAX)	8A

Table 3. Suggested Typical Component Selections for the Application of SGM61282-3.3 (1)

Reference	Description
L	1.5μH
C_{LDO}	10μF/6.3V/0603
R_{EXT}	2.2Ω/0603
C_{EXT}	4.7μF/6.3V/0603
C_{IN}	10μF/35V/0805 × 2 0.1μF/50V/0603 × 1
C_{OUT}	22μF/6.3V/0805 × 6
R_{BOOT}	0Ω/0603
C_{BOOT}	0.1μF/50V/0603
C_{VCC}	1μF/6.3V/0603
$C_{EN/MODE}$	0.1μF/50V/0603

NOTE: 1. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

Power Supply Recommendations

SGM61282-3.3 is fixed 3.3V output voltage version. This device is not suggested to be used in the notebook with 2-series battery. Because the voltage of 2-series battery is smaller than 7.5V, the device works in the large duty status. At this condition, the device OC and UVLO value has large various.

This device is suggested to be used in the notebook with larger than 2-Series battery, the battery voltage is larger than 7.5V.

Input Capacitor Selection

For the input capacitor selection, SGM61282 requires high-quality ceramic decoupling capacitors, such as X5R or X7R or similar. These types of capacitors are commonly used for power regulator capacitors due to their stable dielectric material, which results in less capacitance variation and greater temperature stability. When choosing the input capacitors, the voltage rating of capacitor should have a safe margin from maximum input voltage. Choosing an input capacitor with a voltage rating 1.5 times higher than the maximum input voltage is a safe design practice. The input RMS current can be calculated by Equation 1:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times {I_{OUT}}^2 + \frac{\Delta {I_L}^2}{12}\right]} \quad (1)$$

APPLICATION INFORMATION (continued)

To select a suitable capacitor for the RMS current rating, it is recommended to use multiple capacitors with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. Therefore, two 10μF low ESR capacitors are placed at the input. The input ripple voltage can be calculated by Equation 2:

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{C_{IN} \times f_{SW} \times V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Inductor

When selecting an inductor, it is important to specify both the inductance and the peak current required. Inductor selection is usually flexible, and depending on the tradeoff between size, cost, and circuit efficiency. Lower inductor values can reduce size and cost, and improve transient response. However, the inductor ripple current and output voltage ripple are increased, and the efficiency is also reduced due to the higher peak current. In contrast, higher inductance values result in higher efficiency, but at the cost of increased physical size or increased resistance due to the need for more turns of wire. In addition, the transient response will be slower due to the additional time it takes to change the current in the inductor. The approximate inductor value can be calculated by using Equation 3:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L} \quad (3)$$

With the selected inductor value, the ripple current (ΔI_L) and the corresponding peak inductor current I_{L_PEAK} can be calculated using Equation 4 and Equation 5:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (4)$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{\Delta I_L}{2} \quad (5)$$

where,

I_{OUT_MAX} is the maximum load current. To ensure the full-load range requirement, the saturation current rating (I_{SAT}) must be larger than the I_{L_PEAK}. To achieve optimal efficiency, select an inductor with low DC resistance that meets size and cost requirements. An inductor with a shielded ferrite core is the best choice for the application, which minimizes the core losses and causes fewer EMI and noise issues.

Output Capacitor Selection

To achieve the best performance, ceramic capacitors are recommended to be used at the output. The capacitance should be chosen based on the desired output ripple level and the transient response, including over-shoot and undershoot during the load transient.

In a Buck converter, the output ripple is mainly caused by the inductor current ripple and its effect on the output capacitor ESR and storage charge, which are called ESR ripple and capacitance ripple, respectively. Due to the extremely low ESR and relatively small capacitance of ceramic capacitors, the amplitudes of the two types of ripple are similar. In applications where ripple performance is important, both ESR ripple and capacitive ripple should be considered.

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C} \quad (6)$$

$$V_{RIPPLE\_ESR} = \Delta I_L \times R_{ESR} \quad (7)$$

$$V_{RIPPLE\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} \quad (8)$$

In most applications, transient response is usually the more stringent criterion. The output capacitor must either supply the increased load current or absorb the excess inductor current (as the load current decreases) until the control loop can readjust the inductor current to the new load level. Typically, COT structure has a very fast transient response and small output transients.

However, under some application conditions, such as at low output voltages and low duty cycles, the use of small ceramic capacitors increases the magnitude of output voltage variation when the load changes fast. The following section describes the calculation of worst-case voltage variations in response to very fast load steps.

The following function is to calculate the ESR step:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR} \quad (9)$$

The magnitude of the capacitive undershoot on positive load steps (sag) is determined by various factors, including the load step, the capacitance of the output capacitor, the inductance value, the voltage difference between the input and output, and the maximum duty cycle.

APPLICATION INFORMATION (continued)

The maximum duty cycle in a quick transition is influenced by the on-time and minimum off-time because the COT control method increases current by spacing out on-times with minimal off-times as fast as possible. To find the estimated on-time (ignoring parasitic effects) and maximum duty cycle for a specific input and output voltage, following Equations can be used:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (10)$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}} \quad (11)$$

The effective on-time duration may be slightly extended as the integrated circuit adjusts for voltage reductions within the circuit. However, these adjustments can be disregarded as the on-time duration is increased to account for the voltage losses. The output voltage sag can be determined by calculating it as Equation 12:

$$V_{sag} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN\_MAX} \times D_{MAX} - V_{OUT})} \quad (12)$$

The magnitude of the capacitive overshoot on negative load steps (soar) is determined by the load step, the capacitance of the output capacitor, the inductance value, and the output voltage, as shown in Equation 13:

$$V_{soar} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}} \quad (13)$$

Many applications typically do not encounter immediate full-load changes, and the integrated circuit's high switching frequency and rapid transient response can effectively manage voltage regulation under all circumstances. However, in scenarios involving low-voltage CPU cores or DDR memory supply applications, especially devices operating at high clock frequencies and rapidly switching between sleep modes, voltage sag or soar can cause problems. In such cases, mitigating excessive voltage transients can be achieved by either increasing the quantity of ceramic output capacitors or incorporating additional bulk capacitance. For applications characterized by significant rapid transients, it is advisable to calculate over-shoot and undershoot to ensure that over-voltage protection and under-voltage protection mechanisms are not triggered.

PCB LAYOUT INFORMATION

Designing a good PCB layout has a significant impact on the performance of a switching power supply. For the SGM61282, the layout design can be more critical due to the high switching frequency, high output current and more sensitivity of the COT controllers to the noise. One of the goals of a good layout is to minimize the EMI radiations and the influence (coupling) of the switching noise on the sensitive feedback routes. The voltage gradients induced on the ground planes or other sensitive routes should be minimized to avoid switching instability and deviation from regulation point.

The following layout guidelines are recommended to get the best performance from the SGM61282.

- Consider short, straight, and wide copper traces for the main current paths.
- Place the input capacitor and the output capacitor close to the device with the shortest possible connection traces.
- Keep the SW node area minimal. Also keep this node and the components directly connected to it away from sensitive copper traces and feedback elements (such as FB and OUT pins). Avoid using vias for SW node and make it thick and short for high current.
- Along with the SW, the PGND pin serves as a main heatsinking path. Connect PGND to a large ground plane and stitch it with thermal vias to ground planes on the other layers and specifically to the back side of the PCB for heat sinking and noise reduction.
- Feedback route must be wide and away from the SW node. The input of the 100mA LDO is supplied directly from the OUT feedback line.
- For less parasitic inductance, use multiple vias under the device close to VIN, PGND and the decoupling capacitors pads.

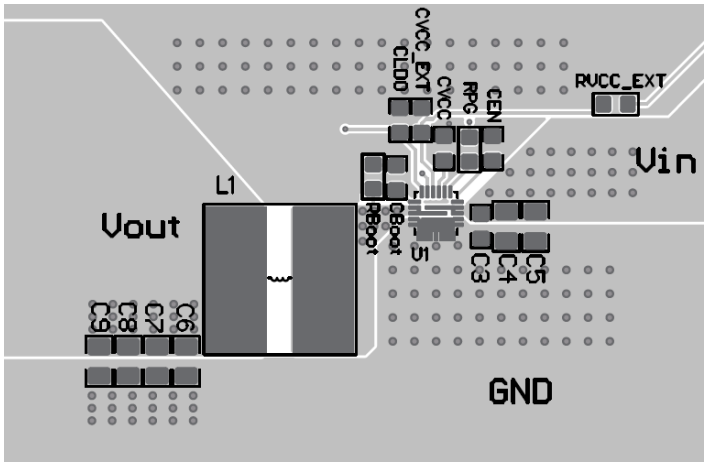


Figure 4. PCB Example

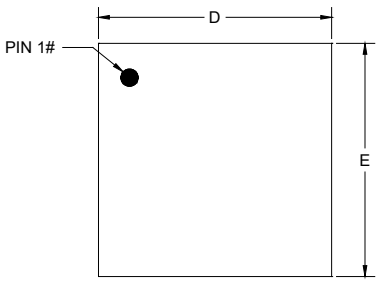
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

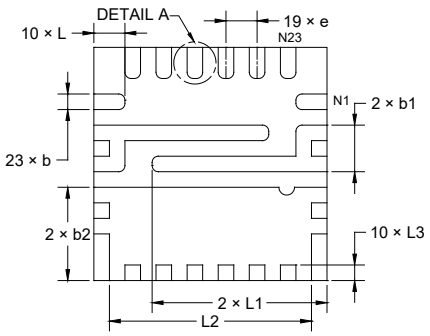
Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

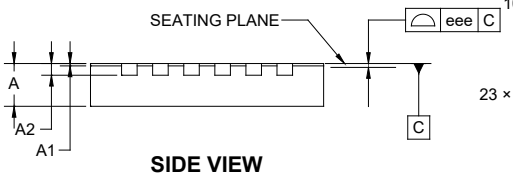
UTQFN-3×3-23L



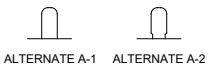
TOP VIEW



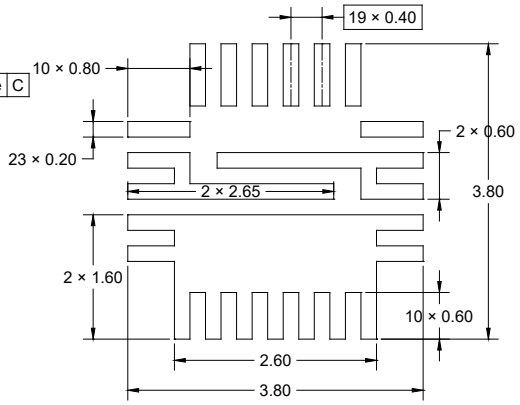
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



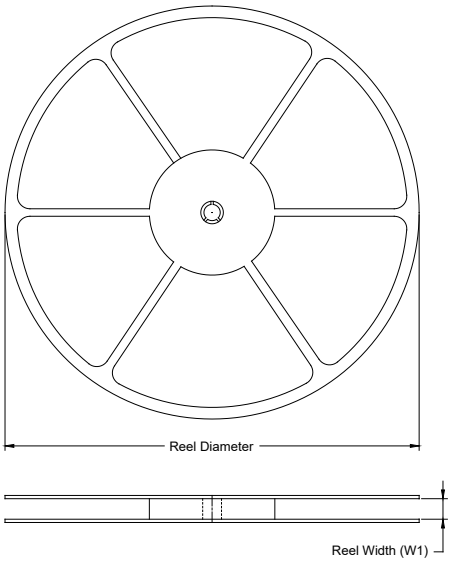
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	-	0.600
A1	0.000	-	0.050
A2	0.150 REF		
b	0.150	-	0.250
b1	0.500	-	0.700
b2	1.100	-	1.300
D	2.900	-	3.100
E	2.900	-	3.100
e	0.400 BSC		
L	0.300	-	0.500
L1	2.150	-	2.350
L2	2.500	-	2.700
L3	0.200 REF		
eee	0.080		

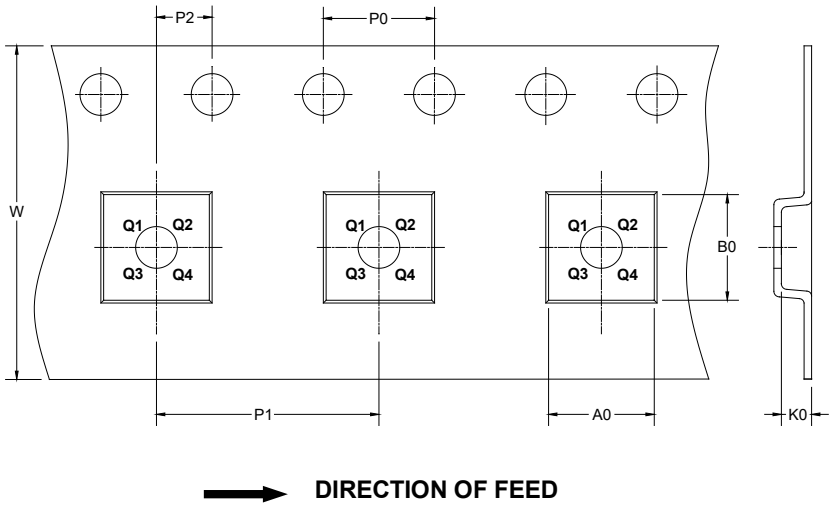
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



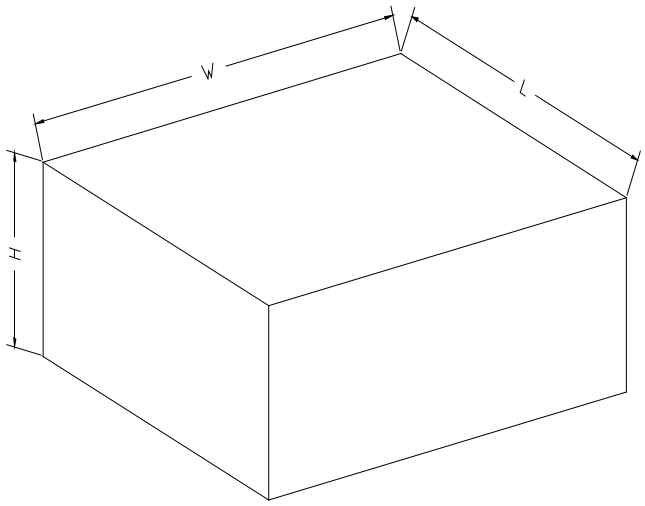
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-3×3-23L	13"	12.4	3.25	3.25	0.75	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002