SGM25110T
2.7V to 16V, 10A, 4.2mΩ eFuse with Transient Over-Current Blanking Timer

GENERAL DESCRIPTION

The SGM25110T eFuse integrates power management and comprehensive circuit protection in compact TQFN package. Requiring minimal externals, these ICs provide robust defense against short-circuits, overloads and excessive inrush currents.

A single external capacitor configures both the output voltage slew rate and inrush current magnitude. When input voltage exceeds an adjustable over-voltage threshold, the output shields loads from input over-voltage conditions. In response to output overload, the devices actively limit current during startup and disconnect the circuit during steady-state operation.

Both the over-current protection threshold and transient over-current blanking timer are user-programmable. The current limit control pin simultaneously provides analog load current monitoring.

The SGM25110T is available in a Green TQFN-2×2-10L package.

SIMPLIFIED SCHEMATIC

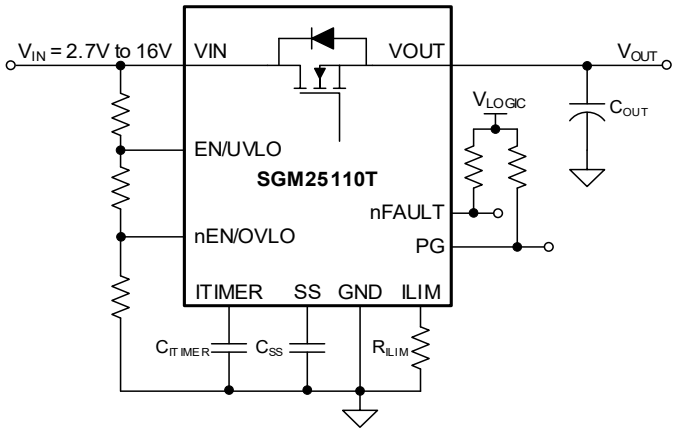


Figure 1. Simplified Schematic

FEATURES

- **Wide Input Voltage Range: 2.7V to 16V**
- **Integrated Switch with 4.2mΩ (TYP) R_{DSON}**
- **Programmable Over-Voltage Lockout (OVLO)**
- **Programmable Over-Current Protection with Accuracy: ±7% (At +25℃ for I_{OUT} ≥ 3A, TYP)**
- **Programmable Transient Blanking Timer (ITIMER) Allowing 2 × I_{LIM} Current (MAX)**
- **IMON Report Accuracy: ±6% (At +25℃ for I_{OUT} ≥ 3A, TYP)**
- **Fast-Trip Response for Short-Circuit Protection**
  - **640ns (TYP) Response Time**
  - **Programmable (2 × I_{LIM}) and Fixed Thresholds**
- **Active-High Enable Input with Programmable Under-Voltage Lockout Threshold (UVLO)**
- **Active-Low Enable Input with Programmable Over-Voltage Lockout Threshold (OVLO)**
- **Programmable Output Slew Rate Control**
- **Option to Drive an External FET for Reverse Current Blocking when Disabled**
- **Over-Temperature Protection**
- **Quick Output Discharge**
- **Digital Outputs**
  - **Power Good and Fault Indication**
- **Available in a Green TQFN-2×2-10L Package**

APPLICATIONS

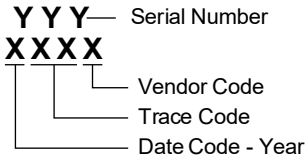
Optical Modules
Industrial PC
UHDTV
Enterprise Routers/Data Center Switches
Server/PC Motherboard/Add-On Cards

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25110TAA	TQFN-2×2-10L	-40℃ to +125℃	SGM25110TAAXTSP10G/TR	36O XXXX	Tape and Reel, 3000
SGM25110TAL	TQFN-2×2-10L	-40℃ to +125℃	SGM25110TALXTSP10G/TR	36P XXXX	Tape and Reel, 3000
SGM25110TBA	TQFN-2×2-10L	-40℃ to +125℃	SGM25110TBAXTSP10G/TR	36Q XXXX	Tape and Reel, 3000
SGM25110TBL	TQFN-2×2-10L	-40℃ to +125℃	SGM25110TBLXTSP10G/TR	36R XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE OPTION TABLE

Model	Over-Voltage Response	Over-Current Response	Reverse Current Blocking FET Driver	Response to Fault
SGM25110TAA	Adjustable OVLO	Circuit-Breaker	No	Auto-Retry
SGM25110TAL				Latch-Off
SGM25110TBA			Yes	Auto-Retry
SGM25110TBL				Latch-Off

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 20V
Output Voltage Range ..... -0.3V to V_{IN} + 0.3V
Output Voltage Pulse ..... -0.8V
Enable Pin Voltage Range ..... -0.3V to 6.5V
nEN/OVLO Pin Voltage Range ..... -0.3V to 6.5V
SS Pin Voltage Range ..... Internally Limited
ITIMER Pin Voltage Range ..... Internally Limited
PG Pin Voltage Range ..... -0.3V to 6.5V
nFAULT Pin Voltage Range ..... -0.3V to 6.5V
ILIM Pin Voltage Range ..... Internally Limited
Continuous Switch Current ..... Internally Limited
Package Thermal Resistance
TQFN-2×2-10L, θ_{JA} ..... 67.2℃/W
TQFN-2×2-10L, θ_{JB} ..... 4.1℃/W
TQFN-2×2-10L, θ_{JC} ..... 40.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.7V to 16V
Output Voltage Range ..... V_{IN}
Enable Pin Voltage Range ..... 5V (MAX)
nEN/OVLO Pin Voltage Range ..... 0.5V to 1.5V
SS Pin Voltage Range ..... V_{IN} + 5V (MIN)
ITIMER Pin Voltage Range ..... 4V (MIN)
PG Pin Voltage Range ..... -0.3V to 6.5V
nFAULT Pin Voltage Range ..... -0.3V to 6.5V
ILIM Pin Resistance to GND ..... 600Ω to 4400Ω
Continuous Switch Current, T_J ≤ +125℃ ..... 10A (MAX)
Operating Junction Temperature Range ..... -40℃ to +125℃

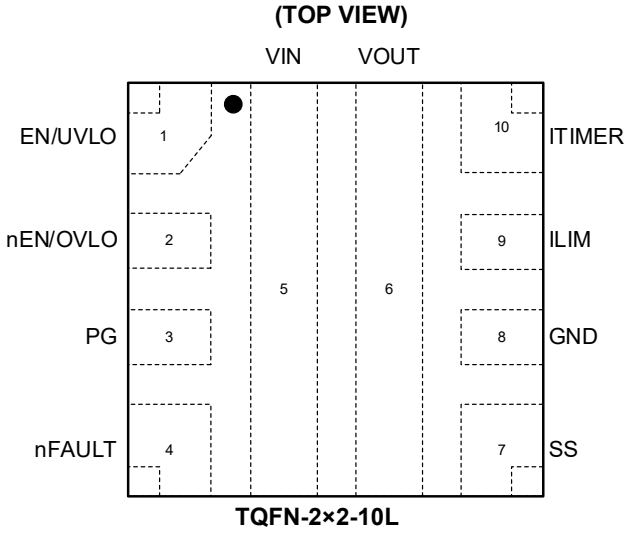
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	AI	Active-High Enable. This pin configures the UVLO threshold voltage through an external resistor divider network tied between the input power supply and GND. Do not leave this pin floating.
2	nEN/OVLO	AI	Active-Low Enable. This pin configures the OVLO threshold voltage through an external resistor divider network tied between the input power supply and GND. Do not leave this pin floating.
3	PG	DO	Power Good Indicator. Open-drain signal which is high when power FET is fully ON and ready to supply power.
4	nFAULT	DO	Active-Low Fault Indicator. Open-drain signal which is pulled low when a fault is detected.
5	VIN	P	Power Input.
6	VOUT	P	Power Output.
7	SS	AO	SS Pin. A capacitor to GND sets output turn-on slew rate which is fastest when floating. For SGM25110TBx variants, drives external FET for reverse current blocking.
8	GND	G	Ground Pin.
9	ILIM	AO	Dual-Function Pin. An external resistor to GND sets over-current thresholds (startup/ steady-state) and pin voltage acts as analog load current monitor. Do not leave this pin floating.
10	ITIMER	AO	ITIMER Pin. A capacitor to GND sets over-current blanking interval. Output current may temporarily exceed limit, below fast-trip threshold. Open for fastest over-current response.

NOTE: AI = analog input, AO = analog output, DO = digital output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{ILIM} = 611Ω, V_{OUT} = open, I_{TIMER} = open, nFAULT = open, SS = open, PG = open. All voltages referenced to GND, and all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
Supply Quiescent Current	I_{Q_ON}				158	300	μA
Supply OFF State Current	I_{Q_OFF}	$V_{SD_F} < V_{EN} < V_{UVLO_F}$			49	120	μA
Supply Shutdown Current	I_{SD}	$V_{EN} < V_{SD_F}$			3	26	μA
Supply UVP Rising Threshold	V_{UVP_R}			2.41	2.52	2.64	V
Supply UVP Falling Threshold	V_{UVP_F}			2.18	2.28	2.38	V
Output Load Current Monitor							
Analog Load Current Monitor Gain	G_{IMON}	IMON:IOUT, $I_{OUT} < I_{LIM}$	I_{OUT} = 1.5A	82.8	95.3	98.9	μA/A
			I_{OUT} = 3A	88.8	95.3	99.3	
			I_{OUT} = 4.5A	89.8	95.3	100.6	
			I_{OUT} = 8A	90.8	95.3	101.6	
			I_{OUT} = 10A	91.2	95.3	101.9	
Over-Current Protection							
Over-Current Threshold	I_{LIM}	R_{ILIM} = 3320Ω		1.82	2.02	2.22	A
		R_{ILIM} = 2212Ω		2.76	2.99	3.22	
		R_{ILIM} = 1102kΩ		5.43	5.9	6.37	
		R_{ILIM} = 750Ω		7.94	8.62	9.3	
		R_{ILIM} = 611Ω		9.71	10.55	11.38	
Circuit-Breaker Threshold	I_{SPFLTI}	ILIM pin open (single point failure)				0.4	A
		ILIM pin shorted to GND (single point failure)			2.36	3.3	
Fixed Fast-Trip Current Threshold	I_{FT}				39.5		A
Scalable Fast-Trip Threshold	I_{SC_GAIN}	I_{LIM} ratio			193		%
VOUT Threshold to Exit Current Limit Foldback	V_{FB}				1.91		V
On-Resistance							
On-Resistance	R_{DSON}	V_{IN} = 2.7V to 16V, I_{OUT} = 3A	T_J = +25℃		4.29		mΩ
			T_J = -40℃ to +125℃			8.5	
Enable/Under-Voltage Lockout							
EN/UVLO Rising Threshold	V_{UVLO_R}			1.176	1.208	1.239	V
EN/UVLO Falling Threshold	V_{UVLO_F}			1.057	1.089	1.122	V
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}			0.45	0.74		V
EN/UVLO Pin Leakage Current	I_{ENLKG}			-0.2		0.2	μA
Over-Voltage Lockout							
OVLO Rising Threshold	V_{OV_R}			1.174	1.204	1.236	V
OVLO Falling Threshold	V_{OV_F}			1.044	1.083	1.122	V
OVLO Pin Leakage Current	I_{OVLKG}	0.5V < V_{OVLO} < 1.5V		-0.2		0.2	μA
Over-Current Fault Timer							
ITIMER Pin Internal Discharge Current	I_{ITIMER}	$I_{OUT} > I_{LIM}$		1.412	2.1	2.83	μA
ITIMER Pin Internal Pull-Up Resistance	R_{ITIMER}				19		kΩ
ITIMER Pin Internal Pull-Up Voltage	V_{INT}			2.52	2.67	2.82	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{ILIM} = 611Ω, V_{OUT} = open, I_{TIMER} = open, nFAULT = open, SS = open, PG = open. All voltages referenced to GND, and all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ITIMER Comparator Threshold	V_{ITIMER_F}	I_{OUT} > I_{LIM}	0.97	1.15	1.34	V
ITIMER Discharge Differential Voltage Threshold	ΔV_{ITIMER}	I_{OUT} > I_{LIM}	1.34	1.52	1.7	V
Power Good Indication						
PG Pin Voltage while De-asserted	V_{PGD}	V_{IN} < V_{UVP_F}, V_{EN} < V_{SD_F}, weak pull-up (I_{PG} = 26μA)		0.56	0.8	V
		V_{IN} < V_{UVP_F}, V_{EN} < V_{SD_F}, strong pull-up (I_{PG} = 242μA)		0.7	0.9	
		V_{IN} > V_{UVP_R}		0	0.2	
PG Pin Leakage Current,	I_{PGLKG}				3	μA
nFAULT Indication						
nFAULT Pin Leakage Current	I_{FLTLKG}		-1		1	μA
nFAULT Pin Internal Pull-Down Resistance	R_{FLTB}			13.26		Ω
Over-Temperature Protection						
Thermal Shutdown Rising Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling		10		℃
SS						
SS Pin Internal Charging Current	I_{SS}	SS pin internal charging current	1.39	3.46	5.54	μA
Quick Output Discharge						
Quick Output Discharge Resistance	R_{QOD}	V_{EN} < V_{UVLO_F}	420	476	541	Ω

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	V_{OVLO} > V_{OV_R} to V_{OUT}↓		1.2		μs
Circuit-Breaker Response Time	t_{CB}	I_{TIMER} = Open, I_{OUT} > I_{LIM} + 30% to V_{OUT}↓		3		μs
Short-Circuit Response Time	t_{SC}	I_{OUT} > 3 × I_{LIM} to output current cut off		640		ns
Fixed Fast-Trip Response Time	t_{FT}	I_{OUT} > I_{FT} to I_{OUT}↓		640		ns
Thermal Shutdown Auto-Retry Interval	t_{TSD_RST}	Device enabled and T_J < T_{SD} – T_{HYS}		110		ms
PG Assertion De-glitch Time	t_{PGA}			14		μs
PG De-assertion De-glitch Time	t_{PGD}			14		μs

SWITCHING CHARACTERISTICS

The slew rate of the rising output voltage is regulated internally and remains invariant throughout the entire operating voltage range. This ensures that the turn-on timing remains unaffected by load conditions. By connecting a capacitor from SS to GND, it can adjust the rising slew rate. As the value of C_{SS} increases, the rising slew rate (SR) will slow down. Turn-off delay and fall time are defined by the RC time constant of the load network. These switching characteristics apply exclusively to startup sequences under steady-state supply conditions, requiring full pre-enable discharge of the load voltage. Unless specified otherwise, typical values are measured at T_J = +25℃ with a load resistance (R_L) of 100Ω and a load capacitance (C_{OUT}) of 1μF.

PARAMETER	SYMBOL	V_{IN}	C_{SS} = Open	C_{SS} = 1800pF	C_{SS} = 3300pF	UNITS
Output Rising Slew Rate	SR_{ON}	2.7V	8.77	1.35	0.78	V/ms
		5V	14.6	1.42	0.84	
		12V	27.84	1.68	0.98	
Turn-On Delay	t_{D_ON}	2.7V	0.32	0.79	1.15	ms
		5V	0.39	1.01	1.46	
		12V	0.39	1.49	2.35	
Rise Time	t_R	2.7V	0.24	1.66	2.77	ms
		5V	0.26	2.82	4.78	
		12V	0.36	5.74	9.84	
Turn-On Time	t_{ON}	2.7V	0.588	2.4	3.89	ms
		5V	0.68	3.67	6.09	
		12V	0.756	7.12	12.39	
Turn-Off Delay	t_{D_OFF}	2.7V	13	14.6	13.7	μs
		5V	8.9	8.9	9.9	
		12V	7.4	6.7	7.5	

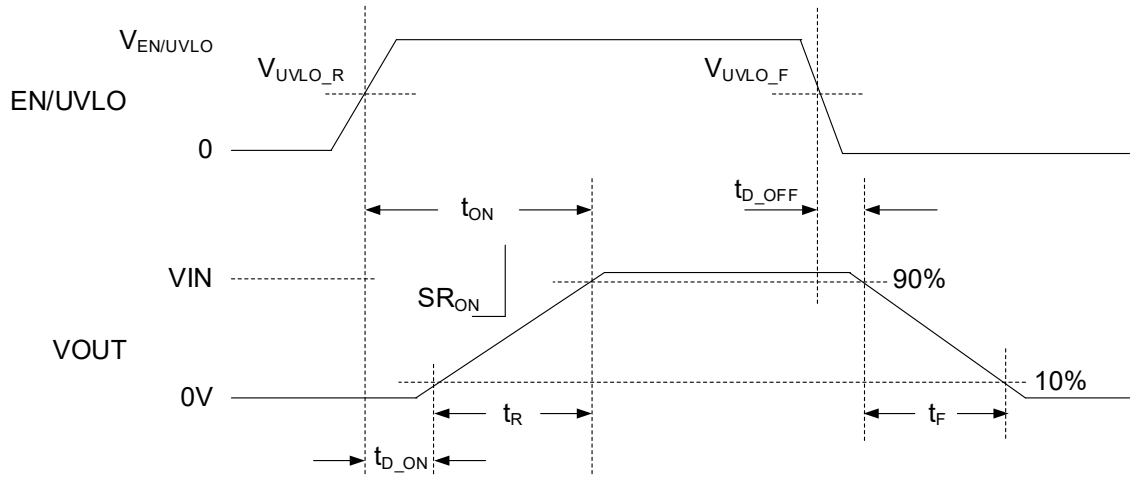
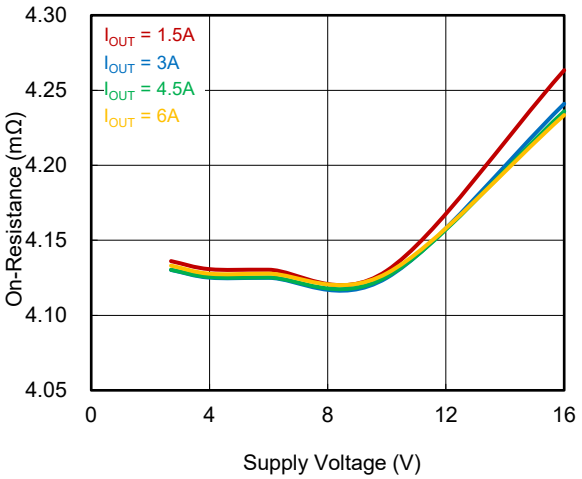


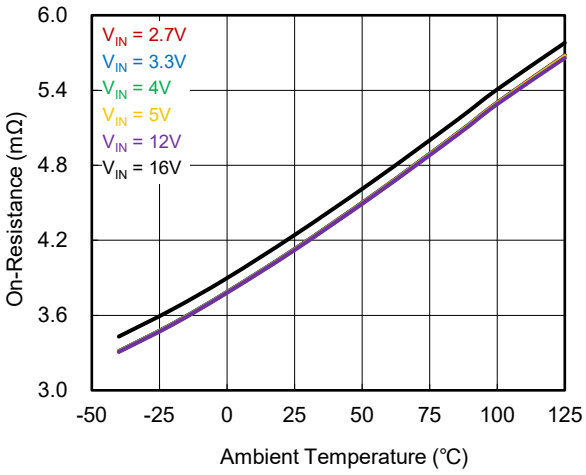
Figure 2. Switching Times

TYPICAL PERFORMANCE CHARACTERISTICS

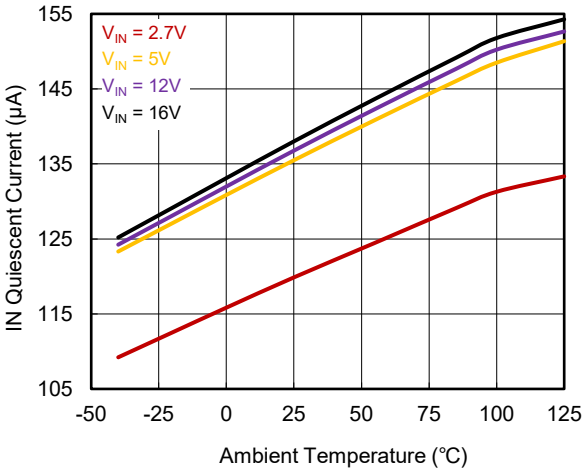
On-Resistance vs. Supply Voltage (T_A = +25℃)



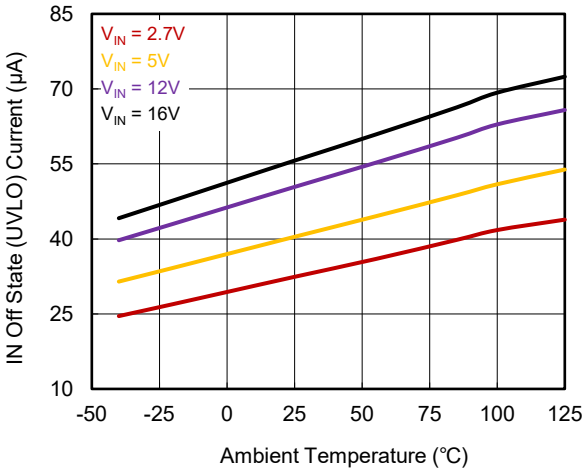
On-Resistance vs. Temperature (I_{OUT} = 3A)



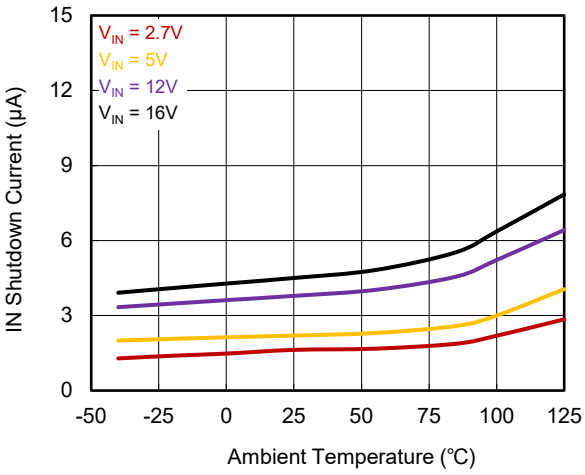
IN Quiescent Current vs. Temperature



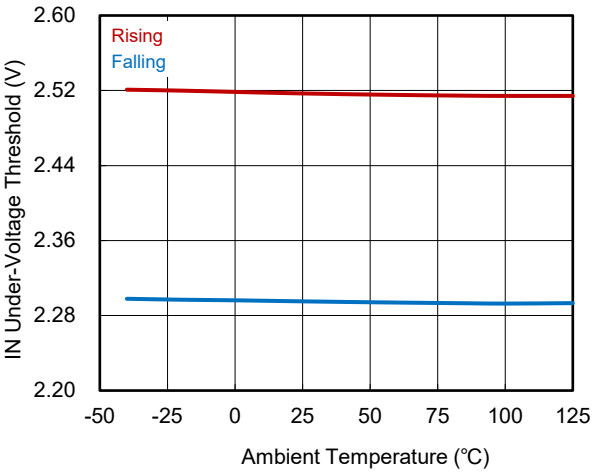
IN Off State (UVLO) Current vs. Temperature



IN Shutdown Current vs. Temperature

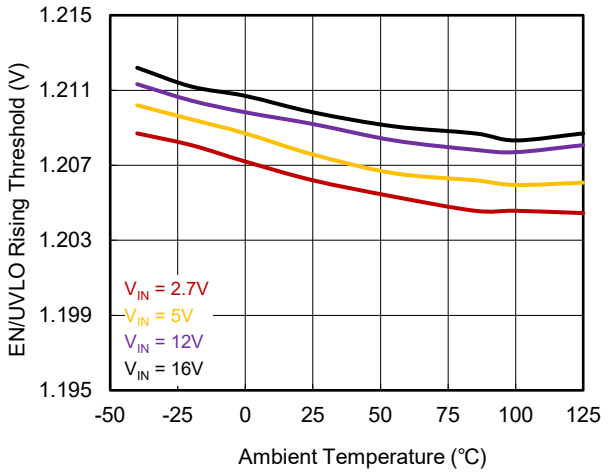


IN Under-Voltage Threshold vs. Temperature

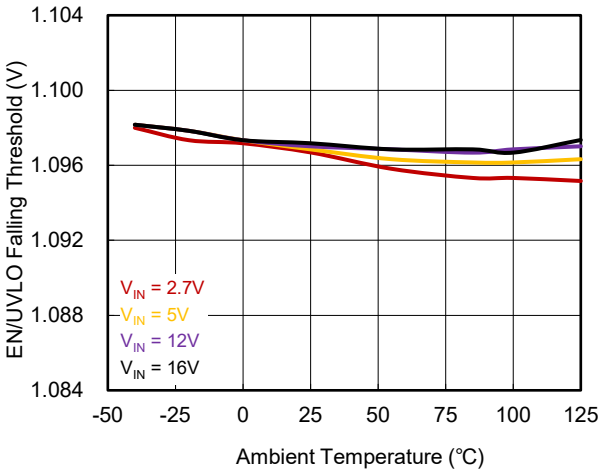


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

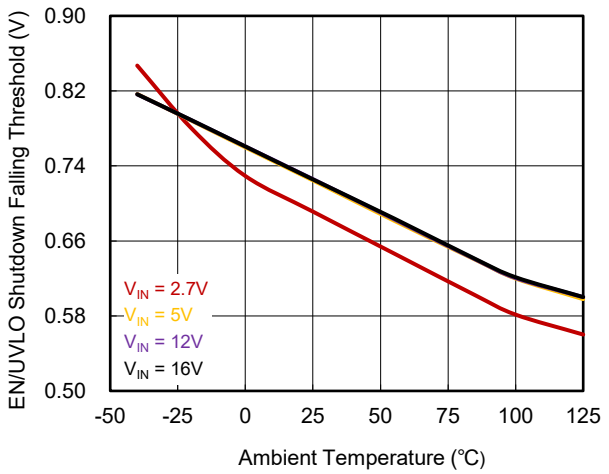
EN/UVLO Rising Threshold vs. Temperature



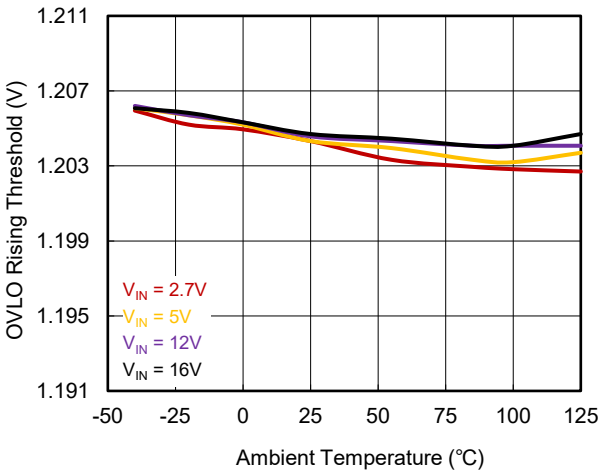
EN/UVLO Falling Threshold vs. Temperature



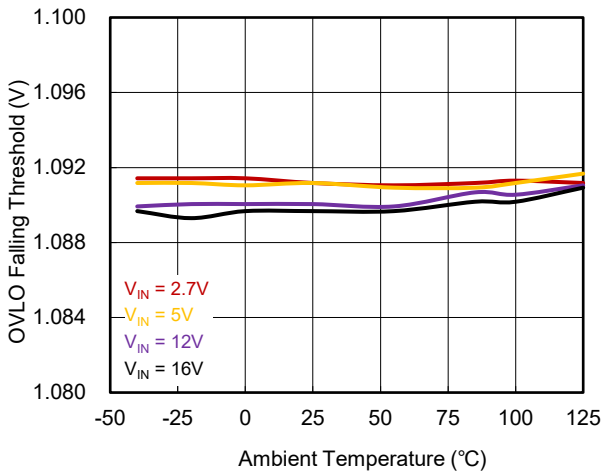
EN/UVLO Shutdown Falling Threshold vs. Temperature



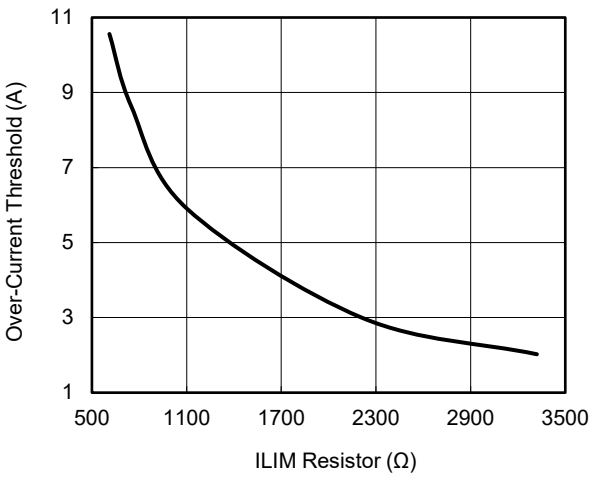
OVLO Rising Threshold vs. Temperature



OVLO Falling Threshold vs. Temperature

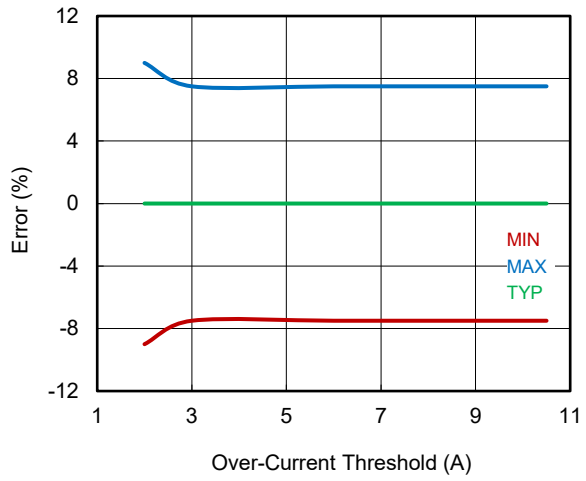


Over-Current Threshold vs. ILIM Resistor

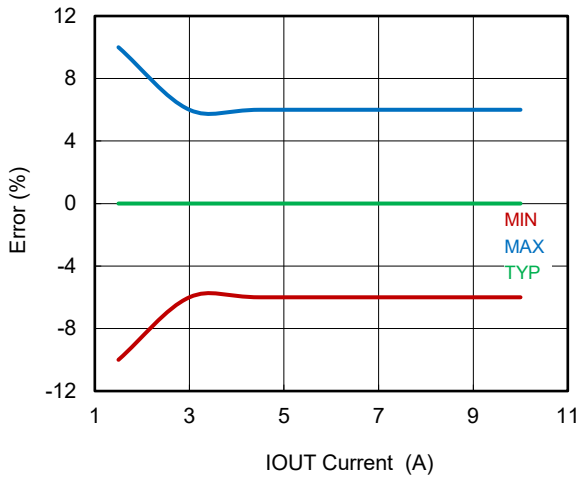


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

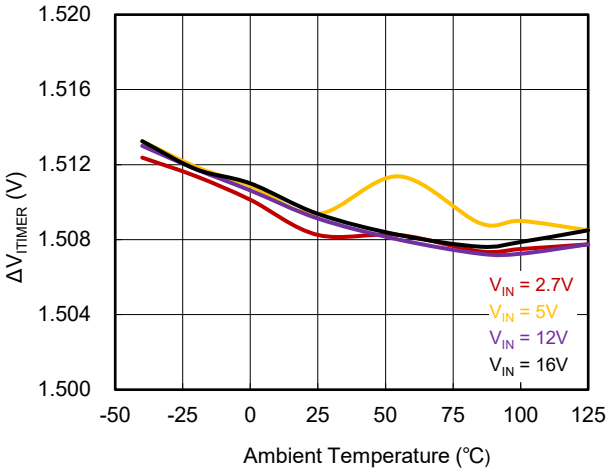
Over-Current Threshold Accuracy



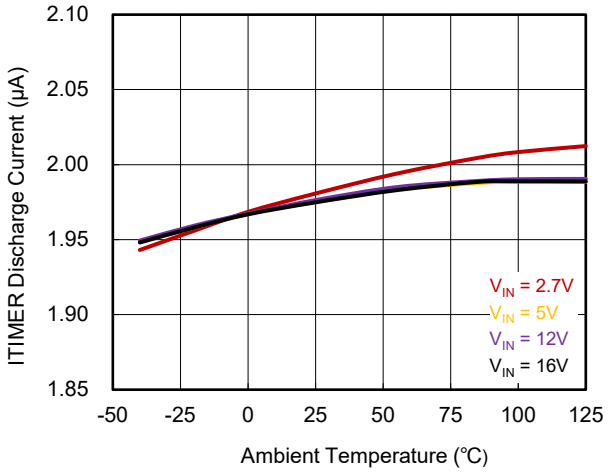
Analog Current Monitor Gain Accuracy



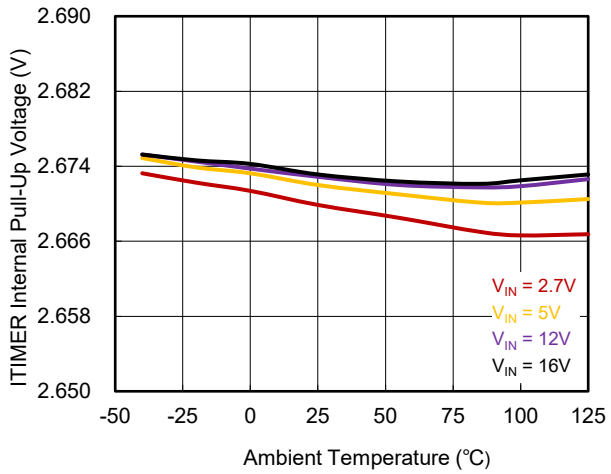
ITIMER Discharge Differential Voltage Threshold vs. Temperature



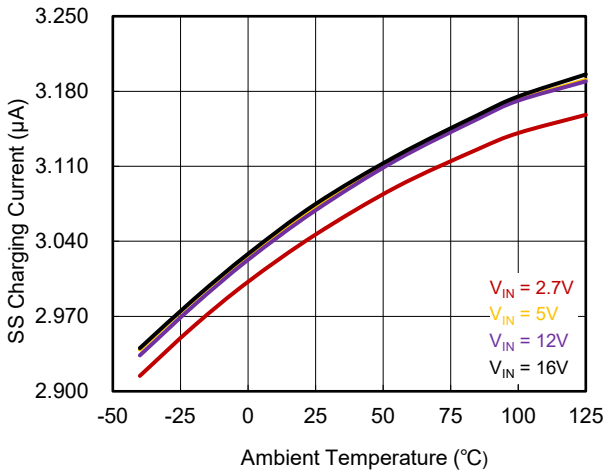
ITIMER Discharge Current vs. Temperature



ITIMER Internal Pull-Up Voltage vs. Temperature

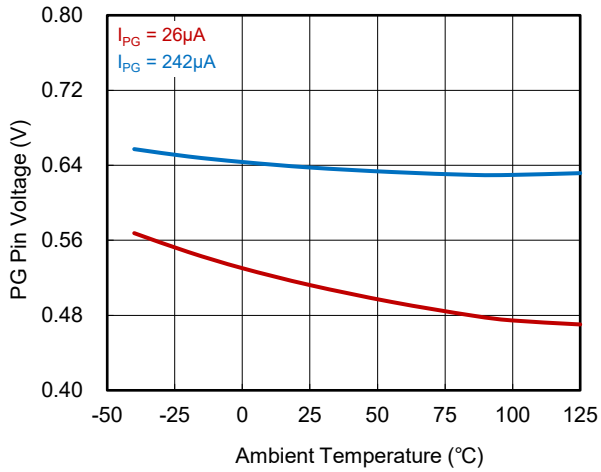


SS Charging Current vs. Temperature

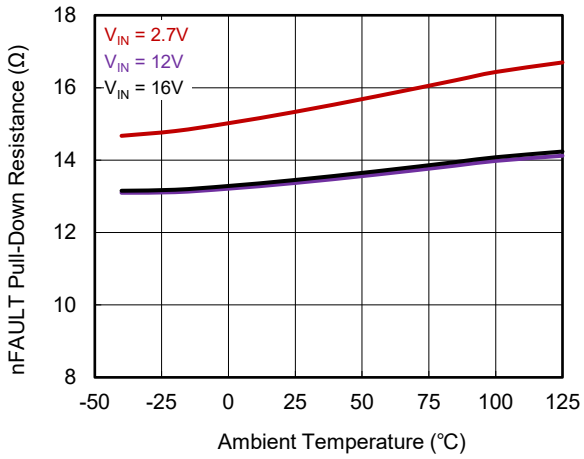


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

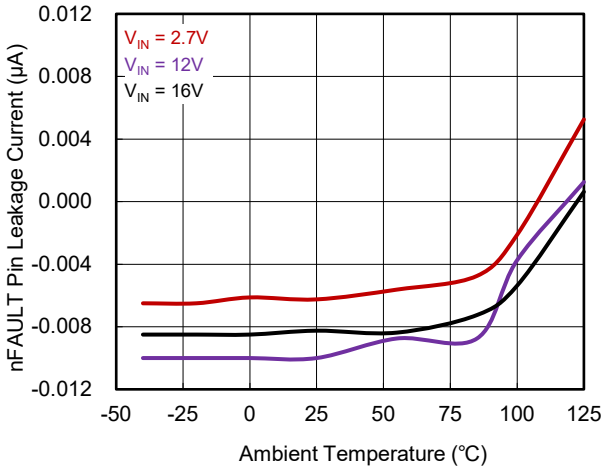
PG Pin Voltage vs. Temperature (V_{IN} = 0V)



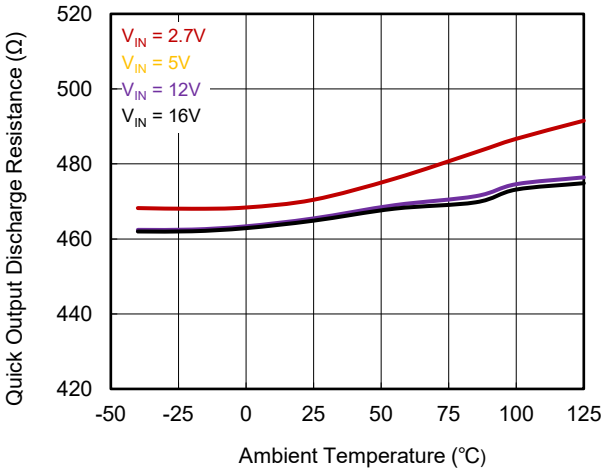
nFAULT Pin Pull-Down Resistance vs. Temperature



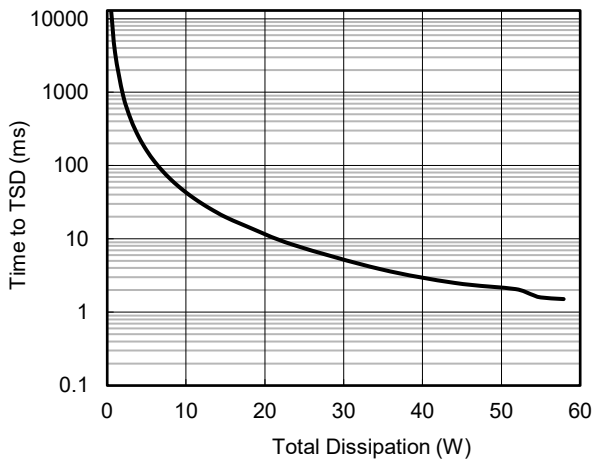
nFAULT Pin Leakage Current vs. Temperature



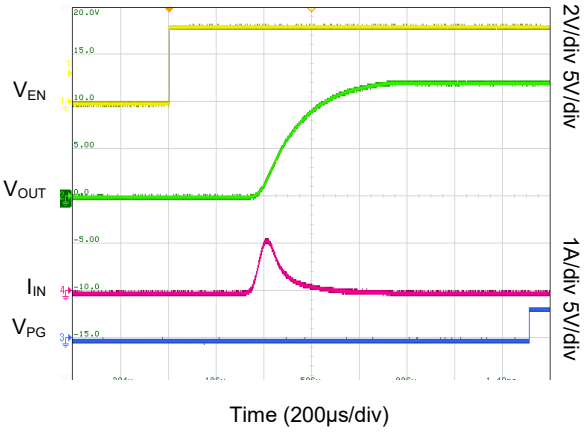
Quick Output Discharge Resistance vs. Temperature



Time to TSD vs. Total Dissipation

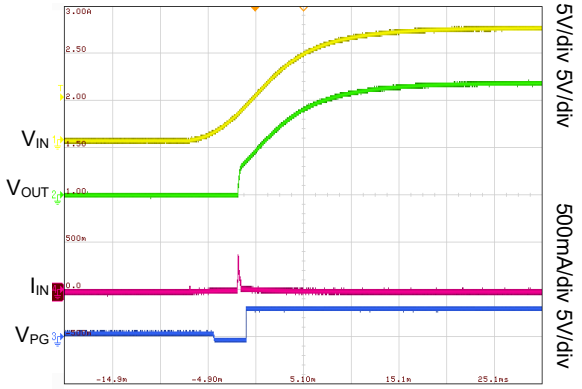


Startup with Enable



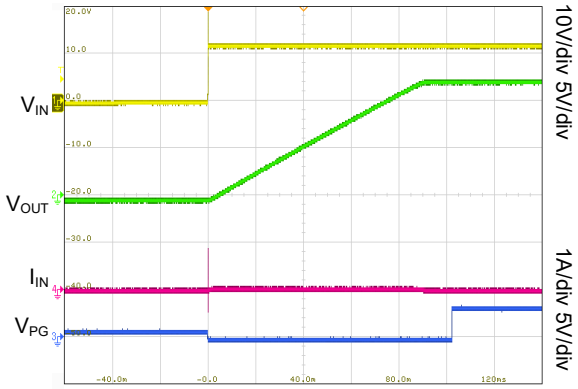
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Startup with Supply



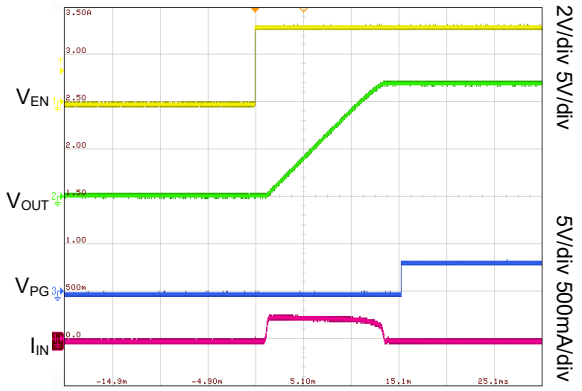
Time (5ms/div)

Input Hot-Plug



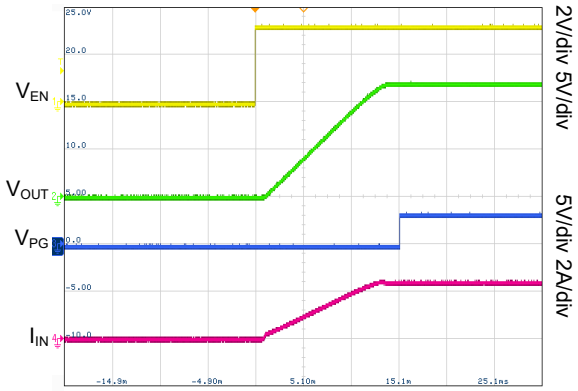
Time (20ms/div)

Inrush Current with Capacitive Load



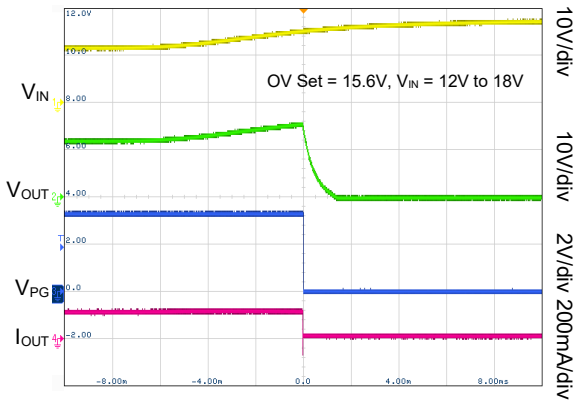
Time (5ms/div)

Inrush Current with Resistive and Capacitive Load



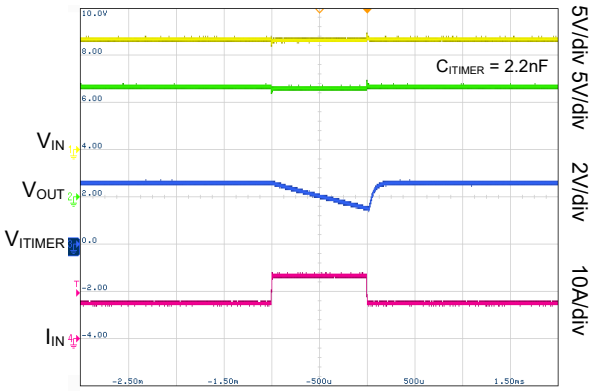
Time (5ms/div)

Over-Voltage Lockout Response



Time (2ms/div)

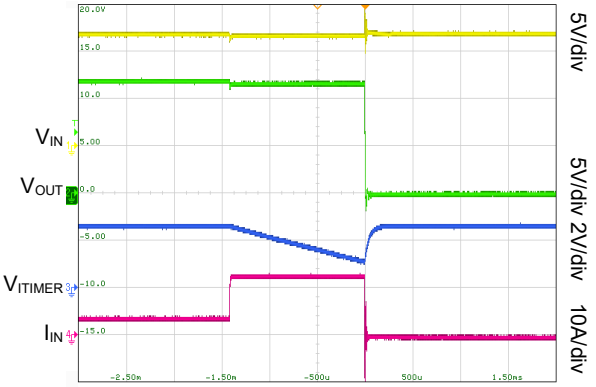
Transient Over-Current Blanking Timer Response



Time (500μs/div)

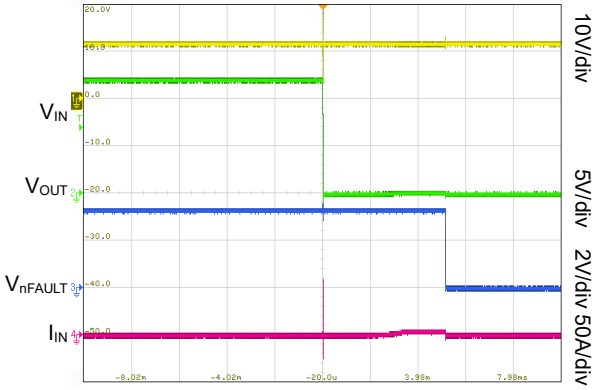
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Circuit-Breaker Response



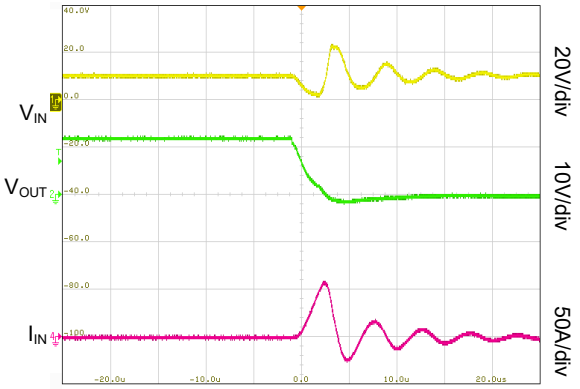
Time (500μs/div)

Output Short-Circuit During Steady-State



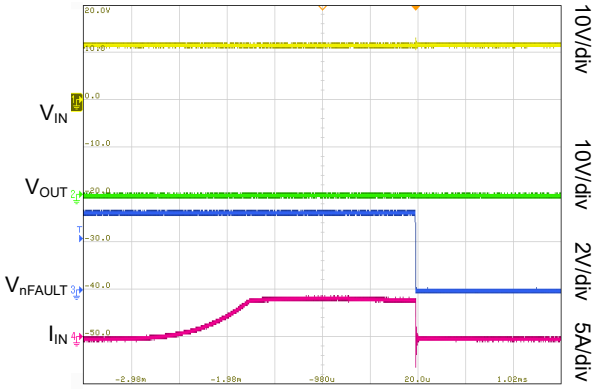
Time (2ms/div)

Output Short-Circuit During Steady-State (Zoomed In)



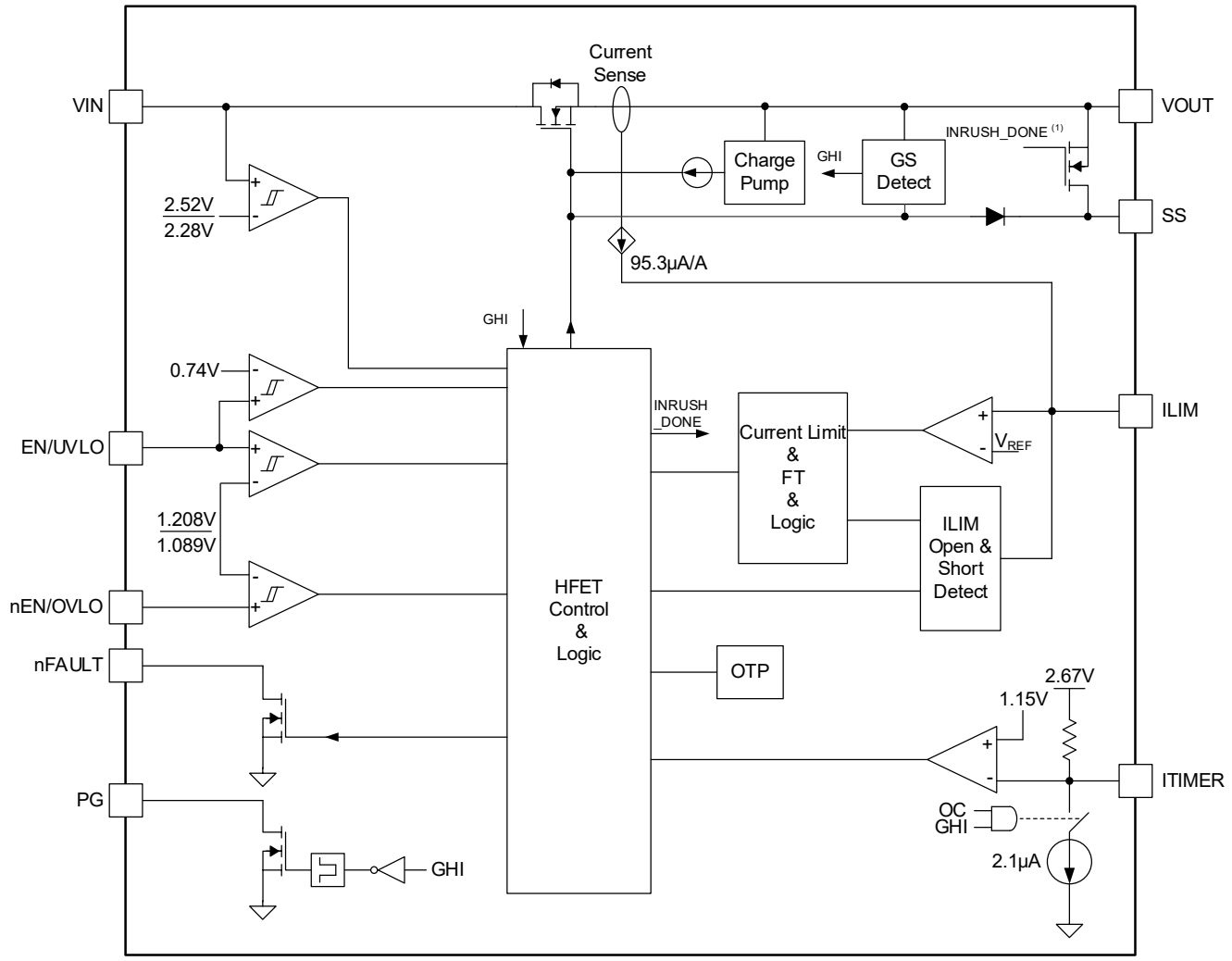
Time (5μs/div)

Power Up into Short-Circuit



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. Not applicable for SGM25110TBx variants.

Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM25110T is an eFuse integrated with a power path, specifically engineered to ensure safe power delivery in a system. This device initiates normal operation by means of monitoring the input bus. When the input supply voltage (V_{IN}) surpasses the under-voltage protection threshold (V_{UVP}), the device proceeds to sample the EN/UVLO control pin. A high-level signal (> V_{UVLO}) on this pin activates the internal power path to commence conduction, permitting current transmission from the VIN terminal to the VOUT terminal. When the EN/UVLO pin is maintained at a low-level (< V_{UVLO}), the internal power path enters the shutdown state.

Following a successful startup procedure, the device actively supervises the load current and input supply voltage while regulating the internal power FET. This control mechanism prevents the load current from exceeding the user-configurable over-current protection threshold (I_{LIM}) and clamps over-voltage transients once they surpass the user-configurable over-voltage lockout threshold (V_{OVLO}). Additionally, the device offers rapid short-circuit over-current protection, shielding the system from destructive voltage and current magnitudes. A user-configurable over-current blanking timer enables the system to tolerate moderate transient peaks in the load current waveform without triggering the eFuse. This functionality delivers a robust protection scheme that is immune to transients while targeting genuine faults, thus maximizing system operational availability.

The device further incorporates an integrated thermal-sensor-based shutdown circuitry for self-protection, activating when the junction temperature (T_J) surpasses the specified maximum operating threshold.

Feature Description

As a feature-rich power management device, the SGM25110T eFuse provides detection, protection, and system fault indication in a compact form factor.

Under-Voltage Lockout (UVLO and UVP)

The SGM25110T provides under-voltage protection to prevent operation at low input voltages. A fixed threshold (V_{UVP}) is monitored on the VIN pin, while a user-defined threshold can be set on the EN/UVLO pin using an external resistor divider. The configuration for this adjustable set point is shown in Figure 4 and calculated using Equation 1.

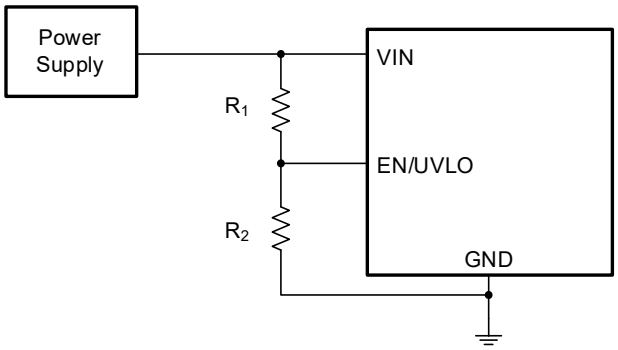


Figure 4. Adjustable Supply UVLO Threshold

$$V_{IN_UV} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

Over-Voltage Lockout (OVLO)

The SGM25110T devices feature an adjustable over-voltage lockout (OVLO) function to protect the load from excessive input voltage. The threshold is set by the user via the nEN/OVLO pin. When the voltage on this pin exceeds the rising threshold (V_{OV_R}), the device turns off the output. The output remains off until the pin voltage drops below the falling threshold (V_{OV_F}). The difference between these thresholds provides the necessary hysteresis. The resistor divider network for programming the desired OVLO set point is configured as shown in Figure 5 and calculated by Equation 2.

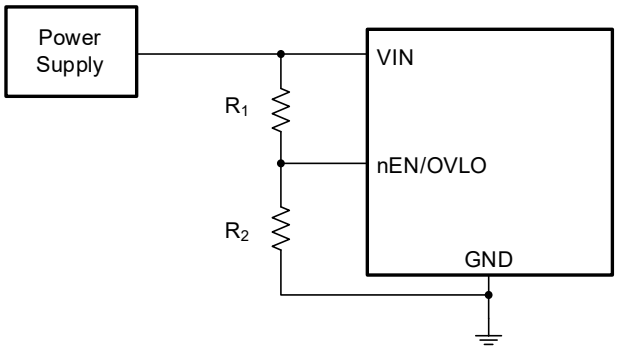


Figure 5. Adjustable Over-Voltage Protection

$$V_{IN_OV} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

Upon recovery from an OVLO event, the SGM25110TAx variants initiate startup with inrush current control. See Figure 6.

DETAILED DESCRIPTION (continued)

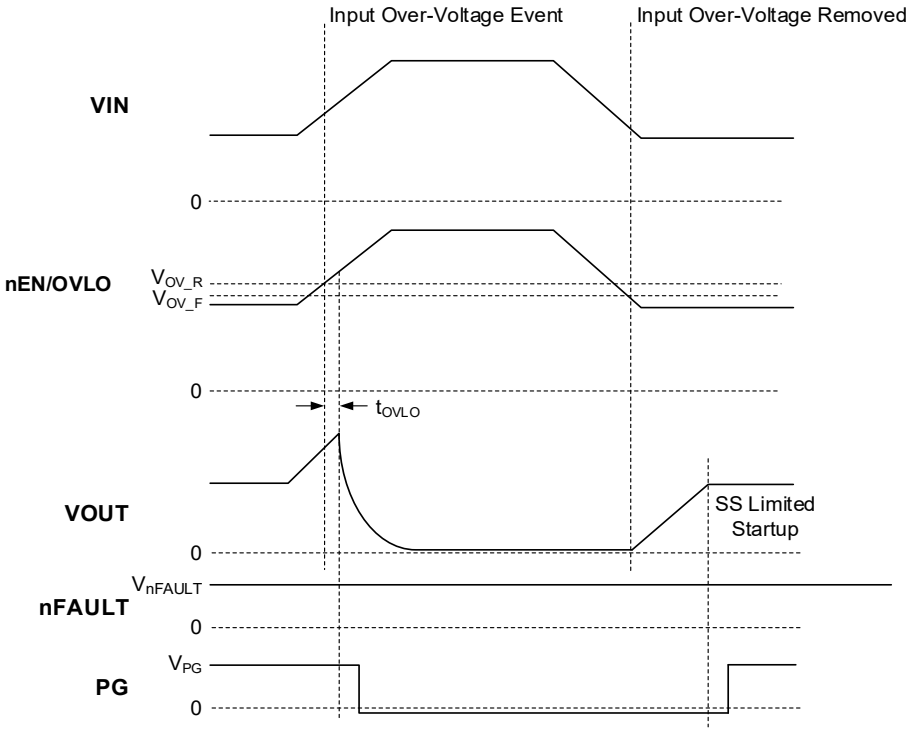


Figure 6. SGM25110TAx Over-Voltage Lockout and Recovery

Inrush Current, Over-Current, and Short-Circuit Protection

The SGM25110T integrates four-level over-current protection scheme:

1. Adjustable Slew Rate (SR): For inrush current control during startup.

2. Adjustable Current Limit (I_{LIM}): Provide sustained protection against overloads during both startup and steady-state operation.

3. Adjustable Fast-Trip (I_{SC}): Enable quick response to severe over-current faults.

4. Fixed Fast-Trip (I_{FT}): Deliver immediate protection against steady-state severe over-current faults.

Slew Rate (SR) and Inrush Current Control

A large inrush current can flow during hot-plug events or when charging a substantial output capacitance at startup. This current risks damaging input connectors and causing system supply droop, which may trigger unexpected resets. Since the turn-on inrush current is directly proportional to both the load capacitance and the rising slew rate, Equation 3 calculates the required slew rate (SR) to limit the inrush current (I_{INRUSH}) for a specific load capacitance (C_{OUT}).

$$SR\left(\frac{V}{ms}\right)=\frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)} \quad (3)$$

The output rising slew rate at turn-on is configurable by connecting a capacitor to the SS pin, which serves to limit the inrush current. The value of this external capacitor (C_{SS}) is calculated using Equation 4.

$$C_{SS}\ (pF)=\frac{3300}{SR\left(\frac{V}{ms}\right)} \quad (4)$$

To achieve the fastest possible output slew rate, the SS pin should be left open.

DETAILED DESCRIPTION (continued)

Circuit-Breaker during Steady-State

The SGM25110TAx circuit-breaker variants incorporate a user-adjustable transient fault blanking interval prior to output shutdown in response to over-current conditions. When the load current exceeds the programmable I_{LIM} threshold (set via resistor R_{ILIM}) but remains below the fast-trip level (2 × I_{LIM}), an internal 2.1μA current sink begins discharging the external ITIMER capacitor (C_{ITIMER}). This initiates the blanking timer. The device differentiates between transient and sustained faults based on this timer. If the over-current condition ceases before C_{ITIMER} discharges by ΔV_{ITIMER}, the ITIMER pin is internally pulled up to V_{INT}, resetting the timer without triggering a shutdown, allowing brief load transients to pass. Conversely, if the over-current persists until C_{ITIMER} discharges by ΔV_{ITIMER}, the circuit-breaker immediately turns off the power FET. Following any discharge event that leads to a shutdown, C_{ITIMER} is automatically recharged to V_{IN}, ensuring the full blanking interval is available for the subsequent over-current event. The required R_{ILIM} value to set the desired I_{LIM} threshold is calculated using Equation 5.

$$R_{ILIM}\ (\Omega) = \frac{6585}{I_{LIM}\ (A)} \quad (5)$$

The allowable duration for transient currents is adjusted by selecting an appropriate capacitor from the ITIMER pin to GND. The required C_{ITIMER} value to achieve a desired blanking interval is calculated using Equation 6.

$$C_{ITIMER}\ (nF) = \frac{t_{ITIMER}(ms) \times I_{ITIMER}(\mu A)}{\Delta V_{ITIMER}\ (V)} \quad (6)$$

For configurable fault response timing, the ITIMER pin should typically be left open to achieve minimum circuit interruption delay. Shorting this pin to ground provides similarly fast response but increases quiescent current, and is therefore not recommended. The capacitor on this pin (C_{ITIMER}) sets the over-current blanking interval; note that while a larger capacitance extends the programmed blanking time, it also increases the recharge duration to V_{INT}. A subsequent over-current event occurring before complete recharge will result in an effectively shorter blanking period. In low-voltage applications, a 30kΩ resistor in series with C_{ITIMER} is recommended to improve noise immunity. Post-fault behavior is variant-dependent: the SGM25110TAL remains latched off, while the SGM25110TAA restarts automatically after a fixed delay.

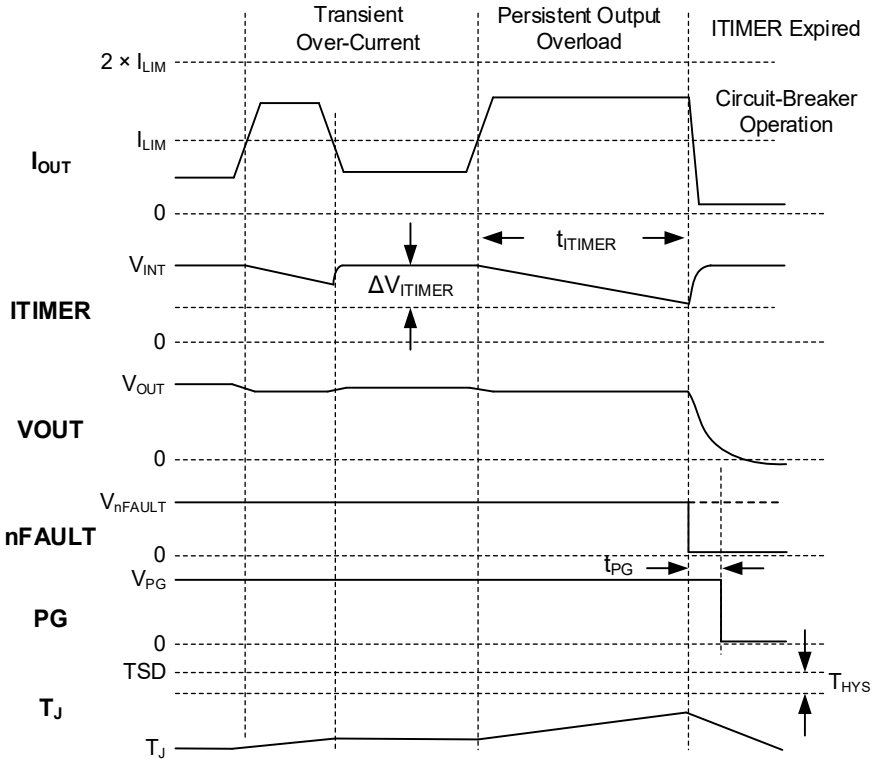


Figure 7. SGM25110TAx Over-Current Response

DETAILED DESCRIPTION (continued)

Active Current Limiting During Startup

To protect against over-current during startup, the SGM25110TAx provides active current limiting. If the load current rises above the I_{LIM} threshold (established via R_{ILIM}) but stays under 2 × I_{LIM}, the internal control loop engages to regulate the FET and limit the current to I_{LIM}. Equation 7 is provided to calculate the R_{ILIM} value for a desired current limit threshold.

$$R_{ILIM}\ (\Omega) = \frac{6585}{I_{ILIM}\ (A)} \quad (7)$$

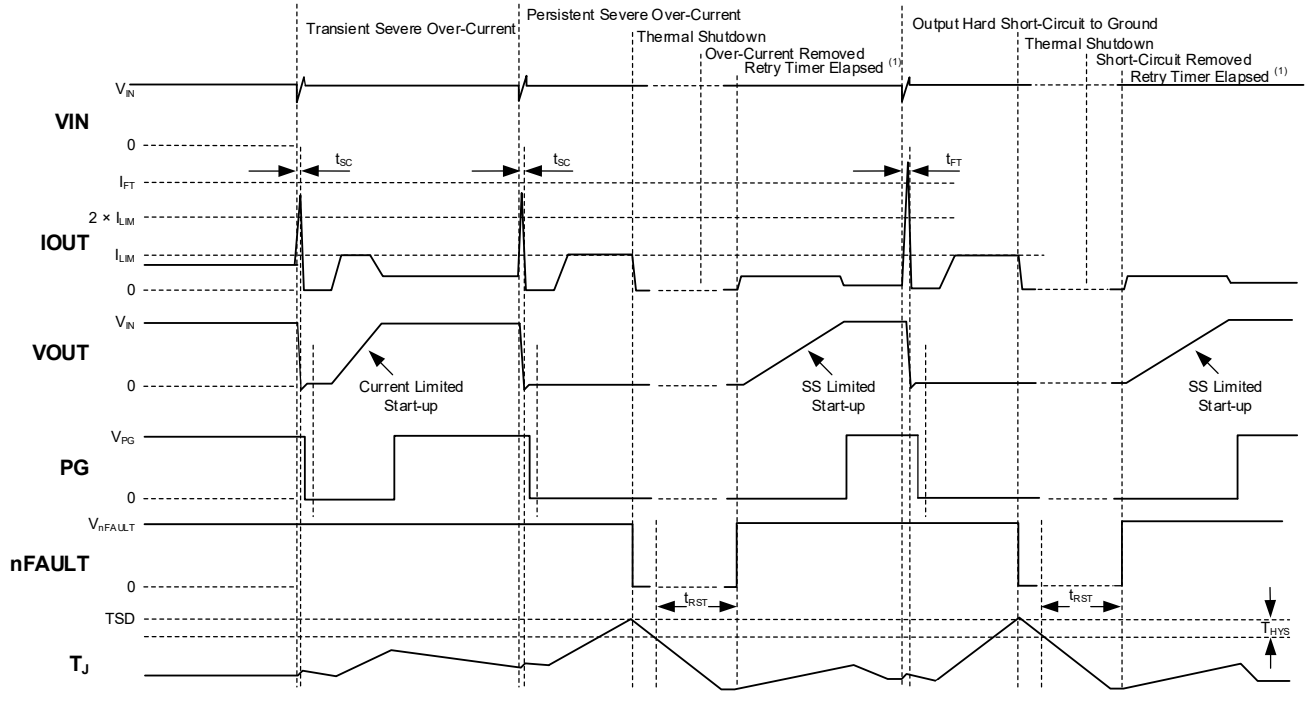
The current limit behavior requires proper configuration of the ILIM pin. Leaving this pin open sets the current limit to nearly zero, causing the device to enter current limit even under minimal load. Under normal operation with a valid R_{ILIM} resistor, the current limit circuit employs a foldback mechanism. In the foldback region (0V < V_{OUT} < V_{FB}), the active current limit threshold is reduced below the target steady-state over-current threshold (I_{LIM}).

Under active current-limiting operation, the reduction in output voltage results in increased power dissipation across the internal FET. If the resulting rise in junction temperature (T_J) exceed the thermal shutdown threshold (T_{SD}), the device disables the output. Following a thermal shutdown event, the fault response is determined by the device variant: the SGM25110TxL series maintains a latched-off state, whereas the SGM25110TxA series automatically initiates a restart sequence after a fixed internal delay.

Short-Circuit Protection

In response to an output short-circuit event, which causes a rapid increase in current, the device employs a fast-trip protection mechanism. This mechanism utilizes two parallel detection paths: a user-scalable threshold (I_{SC} = 2 × I_{LIM}) and a fixed, higher threshold (I_{FT}). The scalable threshold allows adjustment for low-current system compatibility, avoiding the limitations of a single fixed value. When either threshold is exceeded, the internal comparator triggers a complete shutdown of the FET within the specified t_{FT} interval.

Following this shutdown, after a deglitch delay, the device attempts recovery by restarting the FET in a current-limited mode, rather than with SS control. This approach enables faster output voltage recovery and minimizes droop after a transient event. If the fault condition persists, the device remains in current limit, leading to increased power dissipation and a rise in T_J until thermal shutdown is activated.



NOTE: 1. Only applicable to SGM25110TxA (Auto-retry variant).

Figure 8. Short-Circuit Response

DETAILED DESCRIPTION (continued)

Analog Load Current Monitor

An analog current sense output is provided on the ILIM pin to allow system monitoring of the load current. This voltage (V_{LIM}), which is proportional to the current through the FET, is developed across the external resistor R_{ILIM}.

$$I_{LOAD}\ (A) = \frac{V_{ILIM}\ (\mu V)}{G_{IMON}\ (\mu A/A) \times R_{ILIM}\ (\Omega)} \quad (8)$$

The ILIM pin is sensitive to capacitive loading. Careful layout design is required to ensure the total parasitic capacitance on this pin remains below 50pF for stable operation.

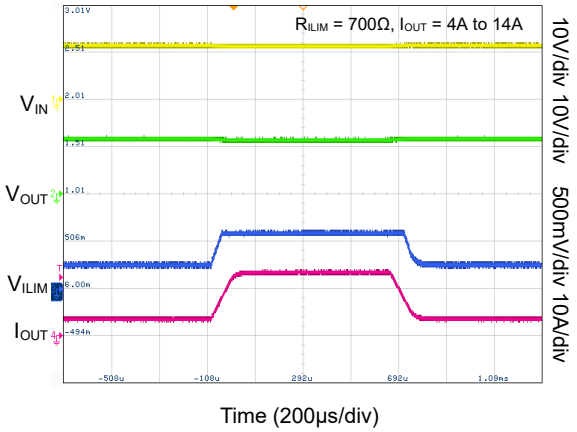


Figure 9. Analog Load Current Monitor Response

Over-Temperature Protection (OTP)

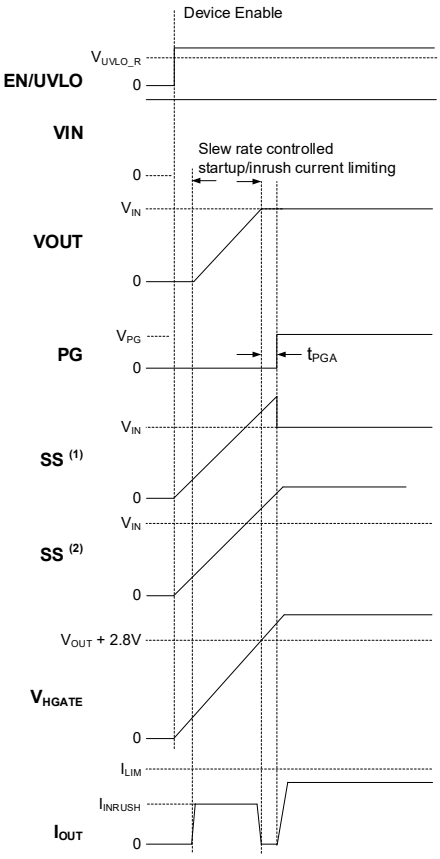
The device features continuous die temperature (T_J) monitoring with shutdown at the T_{SD} threshold and recovery only after T_J drops below (T_{SD} - T_{HYS}). Variants are distinguished by their fault response: the SGM25110TxL latches off until manually reset, and the SGM25110TxA, after cooling by T_{HYS} and a t_{RST} delay, attempts an automatic restart.

Table 1. Thermal Shutdown

Device	Enter TSD	Exit TSD
SGM25110TxL	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} cycled to 0V and then above V_{UVP_R} or EN/UVLO toggled below V_{SD_F}
SGM25110TxA	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} cycled to 0V and then above V_{UVP_R} or EN/UVLO toggled below V_{SD_F} or t_{RST} timer expired

Power Good Indication (PG)

The SGM25110TAx provides an active-high, open-drain PG output, which requires an external pull-up. During power-up, PG is initially held low while the device executes a controlled inrush sequence by gradually turning on the FET. Once the FET gate reaches full overdrive (signifying inrush completion), PG is asserted high after a deglitch delay (t_{PGA}). The PG signal remains high in steady state but is de-asserted (pulled low) whenever the FET is turned off, following a separate deglitch period (t_{PGD}).



NOTES:
1. Applicable only for SGM25110TAx variants.
2. Applicable only for SGM25110TBx variants.

Figure 10. SGM25110T PG Timing Diagram

Table 2. PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
UVP or UVLO	Shutdown	L	
OVLO	Shutdown	L	t_{PGD}
Steady State	NA	H	t_{PGA}
Transient Over-Current	NA	H	
Persistent Overload	Circuit-breaker	L	$t_{ITIMER} + t_{PGD}$
Output Short-Circuit to GND	Fast-trip followed by current limit	L	t_{PGD}
ILIM Pin Open	Shutdown (1)	L (1)	t_{PGD}
ILIM Pin Shorted to GND	Shutdown (2)	L (2)	t_{PGD}
Over-Temperature	Shutdown	L	t_{PGD}

NOTES:
1. ILIM pin open (single point failure), I_{SPFLTI} = 0.4A (MAX).
2. ILIM pin shorted to GND (single point failure), I_{SPFLTI} = 2.36A (TYP).

DETAILED DESCRIPTION (continued)

When the device is unpowered, the PG pin is intended to remain at a low logic level. However, as there is no active internal pull-down in this state, the pin voltage is determined by the external circuit. If the PG pin is connected to a separate, always-present pull-up supply, a residual voltage may appear due to the pin's sink current, which depends on the pull-up voltage and resistor value. To prevent this voltage from being misinterpreted as a logic high by external circuitry, the sink current must be minimized through careful selection of the pull-up network.

Fault Response and Indication

The device's response to different fault conditions is summarized in the table below. An active-low external fault indication pin is also provided for system monitoring.

To clear an internal fault latch, either cycle V_{IN} to 0V or pull EN/UVLO below V_{SD}. This also releases nFAULT and resets the SGM25110TxA's t_{RST} timer. Note that pulling EN/UVLO below only the UVLO threshold does not affect a latched device (both variants). For the SGM25110TxA, automatic restart and nFAULT pin de-assertion occur upon t_{RST} timer expiry.

Table 3. Fault Summary

Event	Protection Response	Fault Latched Internally	nFAUALT Pin Status
Over-Temperature	Shutdown	Y	L
UVP or UVLO	Shutdown	N	H
Input Over-Voltage	Shutdown	N	H
Transient Over-Current (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	N
Persistent Over-Current	Circuit-breaker	Y	N/A
Output Short-Circuit to GND	Circuit-breaker followed by current limit	N	H
ILIM Pin Open (during Steady State)	Shutdown	N	L
ILIM Pin Shorted to GND	Shutdown	Y	L

Quick Output Discharge (QOD)

The SGM25110T provides an integrated output discharge function for rapidly clearing residual charge on large output capacitors, thereby preventing an undefined bus voltage. This function is activated by holding the EN/UVLO pin low (V_{EN} < V_{UVLO_F}), which enables an internal pull-down FET on the VOUT pin. Its operation increases internal power dissipation, potentially raising the T_J. Consequently, to avoid long-term degradation, the function is automatically disabled when T_J exceeds T_{SD}.

Reverse Current Blocking FET Driver

The SGM25110TBx variants support reverse current blocking through an external N-FET. This FET is placed in series with the eFuse in a common-source configuration (see Figure 11), with its gate controlled by the eFuse's SS pin. During normal on-state operation, the SS pin is driven high to fully enhance the external FET, creating a low-impedance path from input to output. Conversely, whenever the eFuse is turned off, the SS pin is pulled low, turning off the blocking FET to eliminate any current path from output back to input.

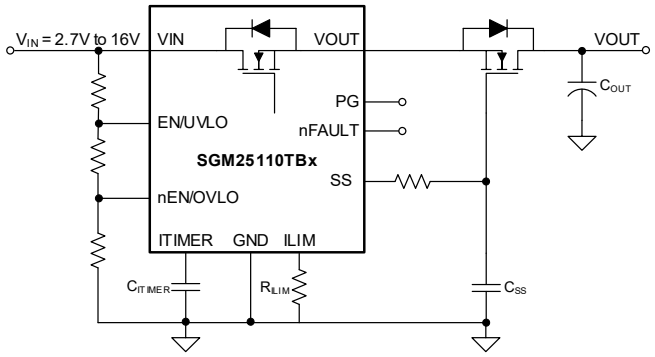


Figure 11. Reverse Current Blocking Using External FET-SGM25110TBx

Device Functional Modes

When operated within its recommended operating conditions, the device functions in a single, specified mode.

APPLICATION INFORMATION

The SGM25110T is a 2.7V to16V, 10A eFuse, offering adjustable OVP/UVP and inrush current control for power rail protection. It suits applications like server cards, optical modules, enterprise routers, industrial PCs, and UHDTVs.

Single Device, Self-Controlled

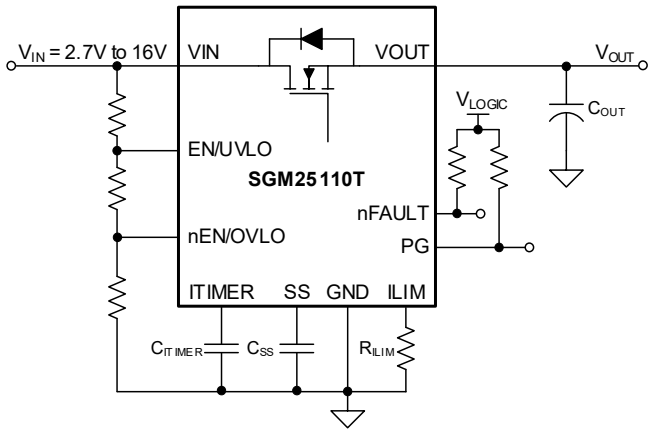


Figure 12. Single Device, Self-Controlled

Other variations

In a host-MCU controlled system, the device can be enabled/disabled via the host GPIO connected to the EN/UVLO or nEN/OVLO pins. For current monitoring, the ILIM pin can be interfaced with an MCU ADC input, with care taken to limit the pin's parasitic capacitance below 50pF as recommended by SGMICRO for stable operation.

Parallel Operation

For applications requiring higher steady-state current, two SGM25110T devices can be connected in parallel as shown in Figure 13. The first device initiates startup, providing inrush current limiting. Its PG pin holds the second device's EN/UVLO low, keeping it off. Once the inrush sequence completes, the first device asserts its PG high, enabling the second device. The second device then asserts its own PG to signal that it is fully on, indicating the parallel combination is ready to deliver full current. In steady state, both devices share current nearly equally, with potential slight imbalance due to R_{DSON} variations and PCB trace resistance mismatches.

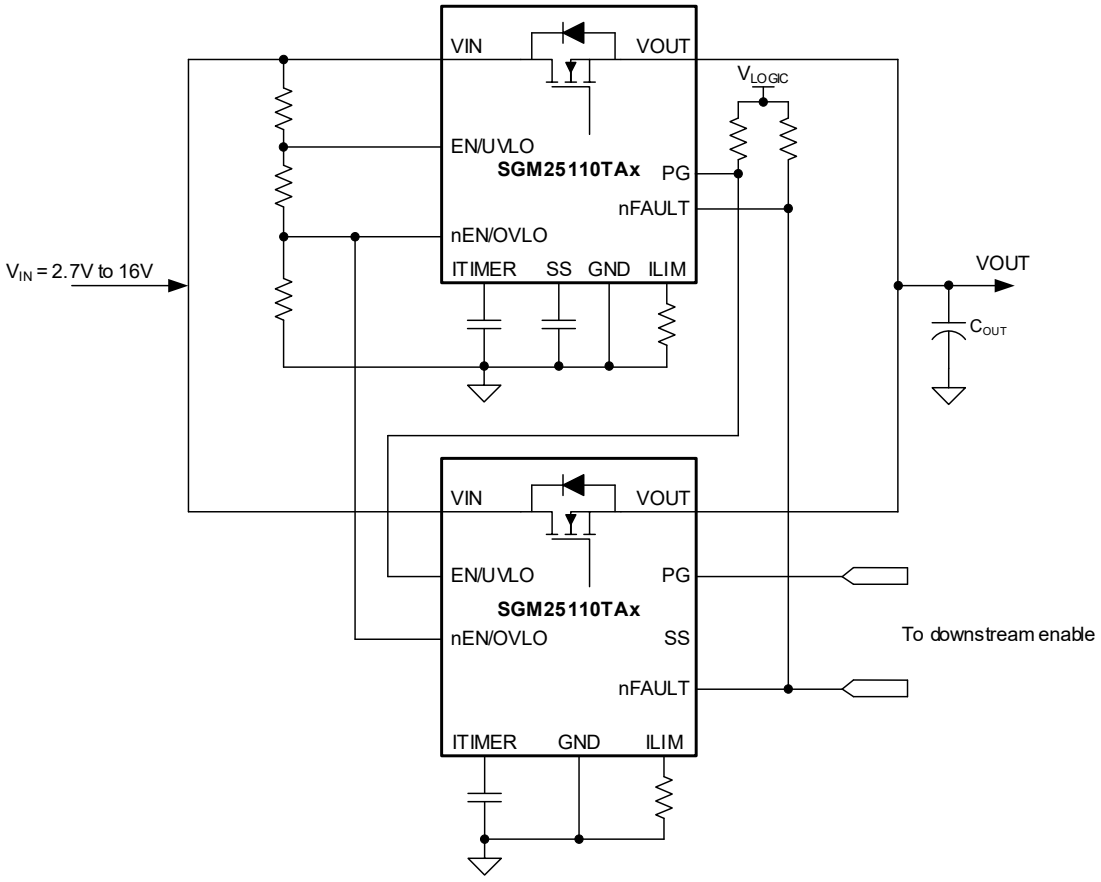
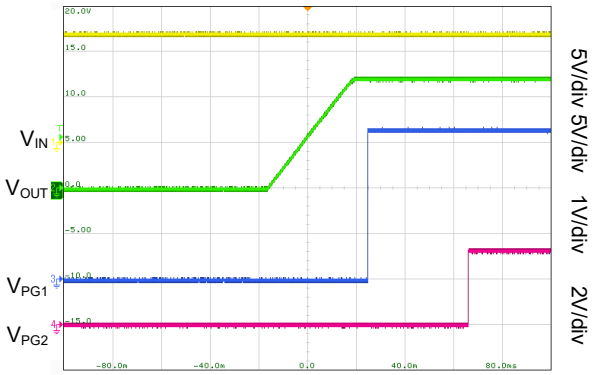


Figure 13. Two SGM25110TAx Devices Connected in Parallel for Higher Steady-State Current Capability

APPLICATION INFORMATION (continued)

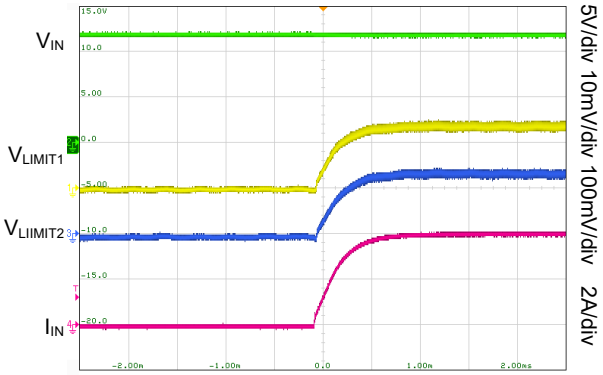
Application Curves

Parallel Devices Sequencing during Startup



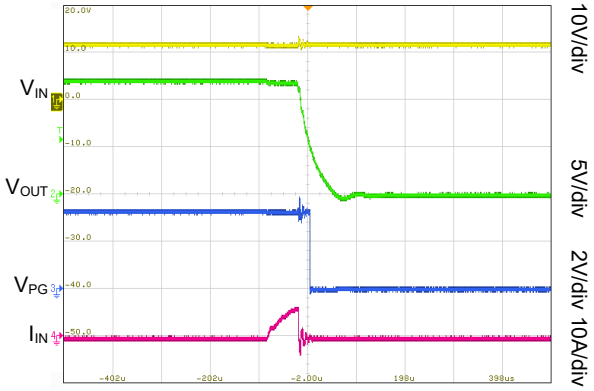
Time (20ms/div)

Parallel Devices Load Current During Steady-State



Time (500μs/div)

Over-Current Shutdown



Time (100μs/div)

APPLICATION INFORMATION (continued)

Typical Application

The SGM25110TAx is suited for protecting the power rail in optical modules, which are critical in high-bandwidth systems like networking equipment and data-center switches. These modules, such as the prevalent QSFP-DD type supporting up to 400Gbit/s, require a tightly regulated 3.3V supply (±5%). A typical optical line card power tree uses an eFuse for protection alongside a DC/DC converter that steps 12V down to 3.3V with ±2% accuracy, followed by an LC filter to suppress high-frequency noise, ensuring the module's voltage precision.

Given the tight voltage regulation requirement, the total allowable drop is 3.3V × 3% ≈ 100mV. The DC resistance of the inductor 'L' accounts for approximately 1.5% (50mV), leaving a budget of 1.5% (50mV) for the protection device. With a maximum load current of 5.5A per module, this translates to a maximum allowable R_{DSON} of less than 9mΩ. The SGM25110TAx eFuse, with a typical R_{DSON} of 6mΩ, meets this specification with additional margin, thereby simplifying system design.

The connection shown in Figure 14 uses the module's ModPrsL signal (internally pulled to ground) for power control. Upon hot-plug insertion, this signal asserts a low level on the OVLO pin, which triggers the SGM25110TAx eFuse to power up the module. This design guarantees that the power rail is active only when a module is installed, preventing voltage exposure on empty ports.

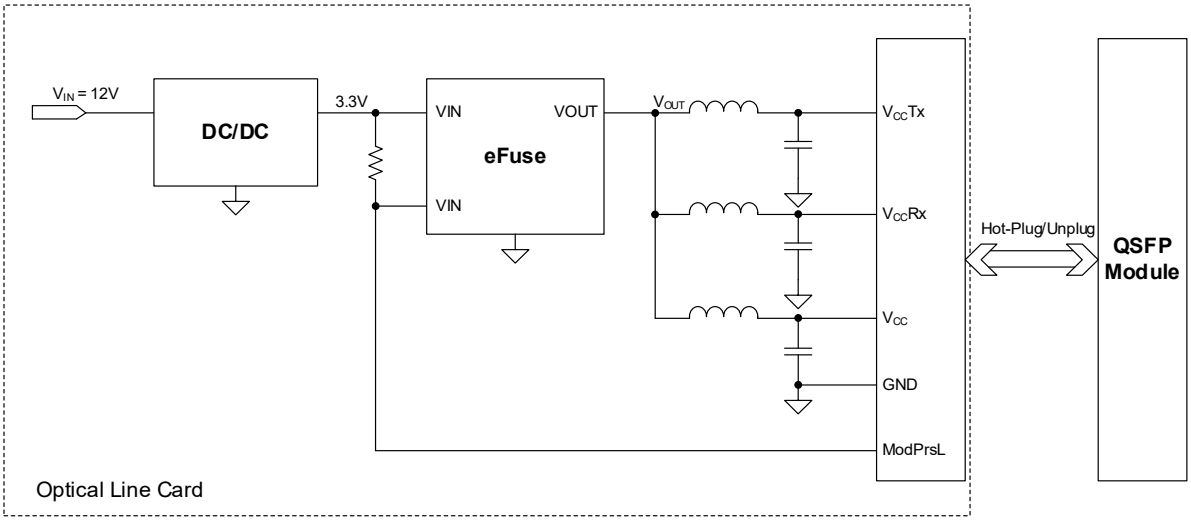


Figure 14. Power Tree Block Diagram of a Typical Optical Line Card

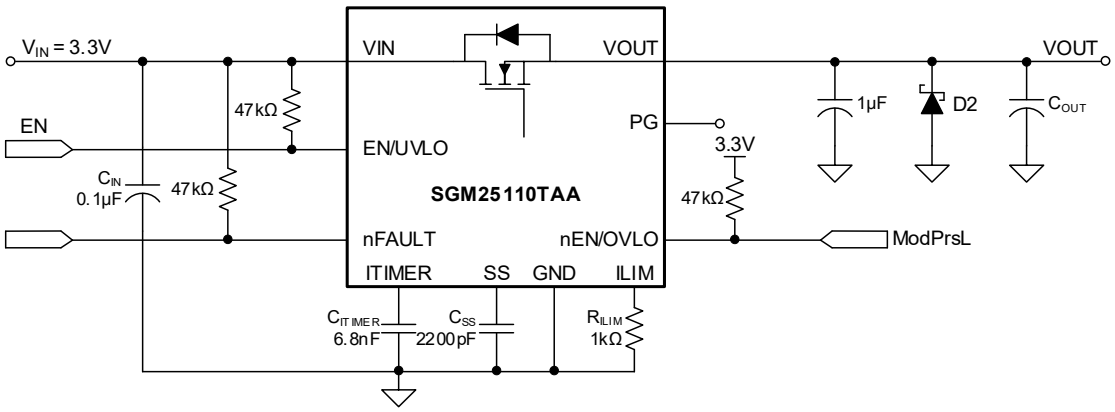


Figure 15. Optical Module Port Protection

APPLICATION INFORMATION (continued)

Design Requirements

Table 4. Design Requirements

PARAMETER	VALUE
Input Supply Voltage	3.3V
Maximum Voltage Drop in the Path	±5%
Maximum Continuous Current	5.5A
Load Transient Blanking Interval	5ms
Output Capacitance	10μF
Output Rise Time	2.2ms
Over-Current Threshold	6.5A
Fault Response	Auto-retry

Detailed Design Procedure

Device Selection

Based on the requirement for a retry response after a fault, the SGM25110TA variant is selected following reference to the Device Option Table.

Setting Output Voltage Rise Time (t_R)

A successful design requires maintaining the device junction temperature below its absolute maximum rating under all conditions, including both steady-state and dynamic startup events. Since dynamic power dissipation during startup can exceed static levels by an order of magnitude, careful selection of the startup time and inrush current limit is critical to avoid thermal shutdown. This selection is based on the system output capacitance. The required slew rate (SR) to achieve the target output rise time is calculated as follows:

$$SR\ (\frac{V}{ms}) = \frac{V_{IN}\ (V)}{t_R\ (ms)} = \frac{3.3V}{2.2ms} = 1.5\frac{V}{ms} \quad (9)$$

To achieve the calculated slew rate, the required capacitance on the SS pin (C_{SS}) is determined by the following formula:

$$C_{SS}\ (pF) = \frac{3300}{SR\ (\frac{V}{ms})} = \frac{3300}{1.5\frac{V}{ms}} = 2200pF \quad (10)$$

Select the nearest standard capacitor value of 2200pF. The inrush current for this slew rate is then calculated as:

$$I_{INRUSH}\ (mA) = C_{OUT}\ (\mu F) \times SR\ (\frac{V}{ms}) = 10\mu F \times 1.5\frac{V}{ms} = 15mA \quad (11)$$

The average power dissipated within the device during the inrush phase is derived from the following formula:

$$PD_{INRUSH}\ (mW) = 0.5 \times V_{IN}\ (V) \times I_{INRUSH}\ (mA) = 0.5 \times 3.3V \times 15mA = 25mW \quad (12)$$

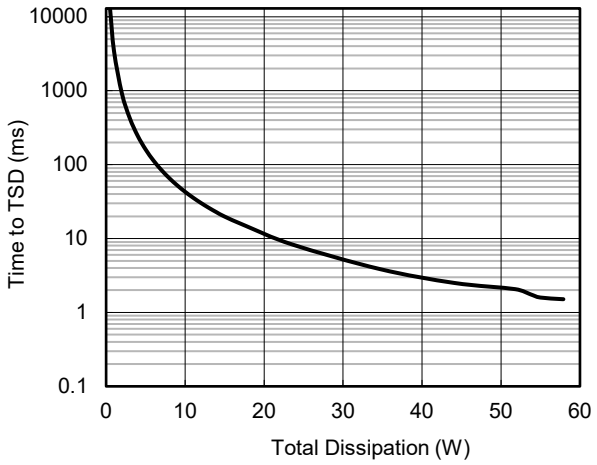


Figure 16. Thermal Shutdown Plot during Inrush

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time to avoid startup failure. To avoid startup failure, the device's thermal shutdown time must exceed the output voltage ramp-up time under the given power dissipation condition.

Setting Over-Current Threshold (ILIM)

The over-current protection (circuit-breaker) threshold is programmed via an external resistor, R_{ILIM}. Its required value is calculated using the following formula:

$$R_{ILIM}\ (\Omega) = \frac{6585}{I_{LIM}\ (\Omega)} = \frac{6585}{6.5A} = 1013\Omega \quad (13)$$

Choose the nearest 1% standard resistor value as 1kΩ.

Setting Over-Current Blanking Interval

To set the desired over-current blanking timer interval, calculate the required C_{ITIMER} as follows.

$$C_{ITIMER}\ (nF) = \frac{t_{ITIMER}\ (ms) \times I_{ITIMER}\ (\mu A)}{\Delta V_{ITIMER}(V)} = \frac{5ms \times 2.1\mu A}{1.51V} = 6.95nF \quad (14)$$

Choose the nearest standard capacitor value as 6.8nF.

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM25110T operates from a supply voltage range 2.7V to 16V. To ensure stable operation when the input supply is located more than a few inches away, it is recommended to use an input ceramic bypass capacitor greater than 0.1μF. Furthermore, the power supply itself must be rated to deliver currents above the set current limit to prevent voltage droop during over-current or short-circuit events.

Transient Protection

During short-circuit or overload event when current is interrupted, parasitic inductance causes voltage spikes: a positive spike at the input and a negative spike at the output. The amplitude of these transients is directly proportional to the inductance in series with the respective pins. Unmitigated, they risk exceeding the device's absolute maximum ratings. Effective countermeasures include: minimizing lead lengths and inductance; employing a large PCB ground plane; placing a Schottky diode from VOUT to GND to clamp negative spikes. Add a low-ESR capacitor (> 1μF) very close to the VOUT pin, and use a low-value ceramic input capacitor (C_{IN} = 1μF) with a voltage rating at least twice the input supply to absorb energy and dampen ringing. Equation 15 provides an estimate for the required input capacitance.

$$V_{SPIKE_ABS} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

The formula parameters are defined as: V_{IN} (nominal supply voltage), I_{LOAD} (load current), L_{IN} (effective source inductance), and C_{IN} (input capacitance). For enhanced reliability, incorporating a Transient Voltage Suppressor (TVS) is often advisable. Its primary role is to clamp transients below the device's absolute maximum ratings. Additionally, a TVS absorbs surplus energy that could otherwise generate high-speed voltage spikes on the IC's input supply pin. These spikes risk coupling into sensitive internal circuitry and inducing unpredictable operation. Refer to Figure 15 for a typical circuit implementation with these protective elements.

Output Short-Circuit Measurements

Obtaining repeatable short-circuit test results is challenging due to variations in multiple factors:

- Source bypassing
- Input lead characteristics
- PCB layout
- Component tolerances
- Output shorting method
- Short location relative to the device
- Measurement instrumentation

Additionally, the physical short itself exhibits microscopic bouncing and arcing, introducing inherent randomness. To obtain realistic results, ensure a consistent configuration and methodology. Note that actual waveforms will vary from those shown in this datasheet due to setup differences.

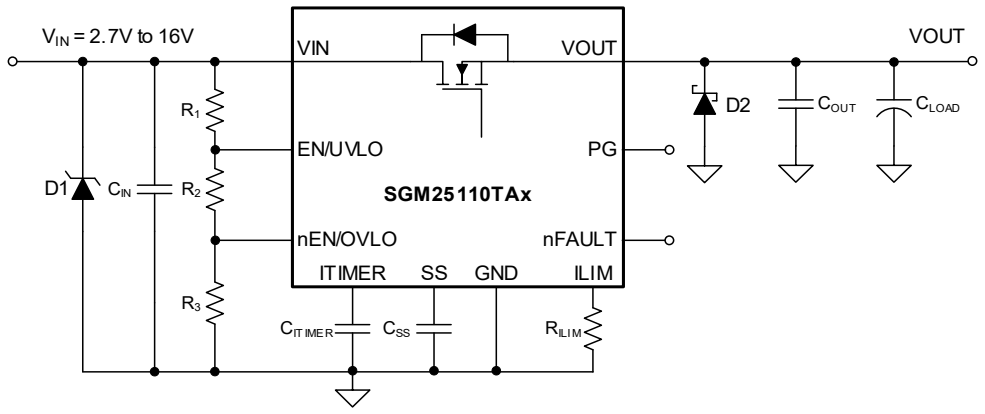


Figure 17. Circuit Implementation with Optional Protection Components

LAYOUT GUIDELINES

• To establish robust power integrity, SGMICRO advises integrating a monolithic ceramic bypass capacitor ≥ 0.1μF between the VIN supply rail and GND reference plane, ensuring effective high-frequency ripple attenuation and enhanced EMI resilience for stable system operation across diverse applications.

• The ideal installation of the bypass capacitor entails positioning it in immediate proximity to the VIN supply pin and GND ground terminal of the device. Special attention must be given to minimizing the current-loop area enclosed by the capacitor connection traces, the input terminal, and the integrated circuit's ground pin, thereby reducing parasitic inductance and optimizing high-frequency filtering performance during PCB layout design.

• The design of high current power transmission paths necessitates minimizing conductor length to reduce parasitic impedances, while ensuring the cross-sectional area is sized to withstand at least twice the rated full-load current. This sizing criterion incorporates safety margins for transient overload conditions and thermal dissipation, ensuring long-term system reliability and efficient energy transfer.

• The GND pin of the IC must be connected directly to the PCB ground plane via the shortest possible trace. The PCB ground should be a solid copper plane or dedicated ground island. SGMICRO recommends an isolated ground island specifically for the eFuse, one that carries no high-current paths and functions as a low-noise reference for all critical analog signals within the eFuse. This local ground plane must then be tied to the system's main power ground plane via a star-point connection to minimize noise coupling and ensure signal integrity. The GND terminal of the IC must be bonded directly to the PCB's ground plane using the shortest feasible trace to minimize parasitic inductance. The PCB ground structure should comprise a dedicated copper plane or isolated ground island. For the eFuse, SGMICRO recommends implementing a separate, dedicated ground plane island that is exclusively reserved for critical analog signals. This dedicated plane, which carries no high-current paths, serves as a low-impedance reference potential for maintaining signal integrity. The device's local ground plane must be connected to the system's power ground plane through a star-point connection to prevent ground-loop noise coupling and ensure galvanic isolation between subsystems.

• The VIN and VOUT pins serve as primary heat dissipation pathways and must be connected to maximize thermally conductive paths by bonding to extensive copper areas on both the top and bottom PCB layers. This connection should be augmented with densely distributed thermal vias beneath the device to facilitate efficient heat transfer. The strategic placement of vias helps mitigate voltage gradients across the VIN and VOUT pads, enabling uniform current distribution through the device. This design approach is critical for optimizing on-resistance performance, enhancing current sensing accuracy, and ensuring long-term thermal reliability by minimizing localized hotspots and electrical stress.

• Locate the following support components close to their connection pins: R_{ILIM}, C_{SS}, C_{ITIMER} and resistors for the EN/UVLO, nEN/OVLO pins.

• Route the opposing end of the component directly to the GND pin of the device using the shortest possible routing. Minimize parasitic impedances impacting current limiting (R_{ILIM}), over-current blanking duration, and soft-start timing by keeping traces from R_{ILIM}, C_{ITIMER}, and C_{SS} components to the device at an absolute minimum. SGMICRO advises maintaining ≤ 50pF parasitic capacitance on the ILIM node to guarantee operational stability. These traces must be physically segregated from all switching signal paths on the board to prevent electromagnetic coupling interference.

• Given the ILIM pin's bias current directly dictates the device's over-current protection behavior, its PCB routing must be physically segregated from any noisy switching signals to prevent parasitic coupling and ensure accurate protection response. Maintaining this isolation is imperative to avoid electromagnetic interference (EMI) that could distort the bias current, thereby compromising protection thresholds and system reliability.

• In the implementation of robust circuit protection, critical components such as TVS diodes, snubbers, and Schottky diodes must be positioned in immediate proximity to the protected device. Short trace routing is essential for minimizing parasitic inductance, a key factor in ensuring effective transient suppression. As recommended by SGMICRO, a protection Schottky diode should be employed to counteract negative voltage transients generated during the switching of inductive loads. The manufacturer further specifies that a ceramic decoupling capacitor (minimum 1μF) must be placed directly between VOUT and GND, with the component mounted adjacent to the VOUT pins. During PCB layout design, special attention should be given to reducing the loop area formed by the Schottky diode, bypass capacitor connections, VOUT pin, and IC's ground terminal to optimize electromagnetic compatibility.

LAYOUT GUIDELINES (continued)

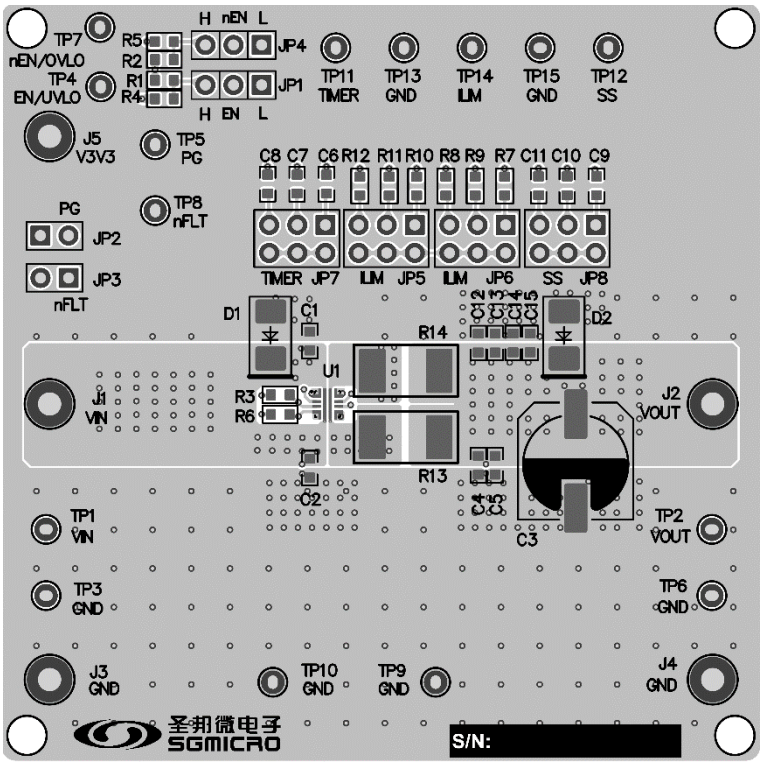


Figure 18. PCB Top Layer

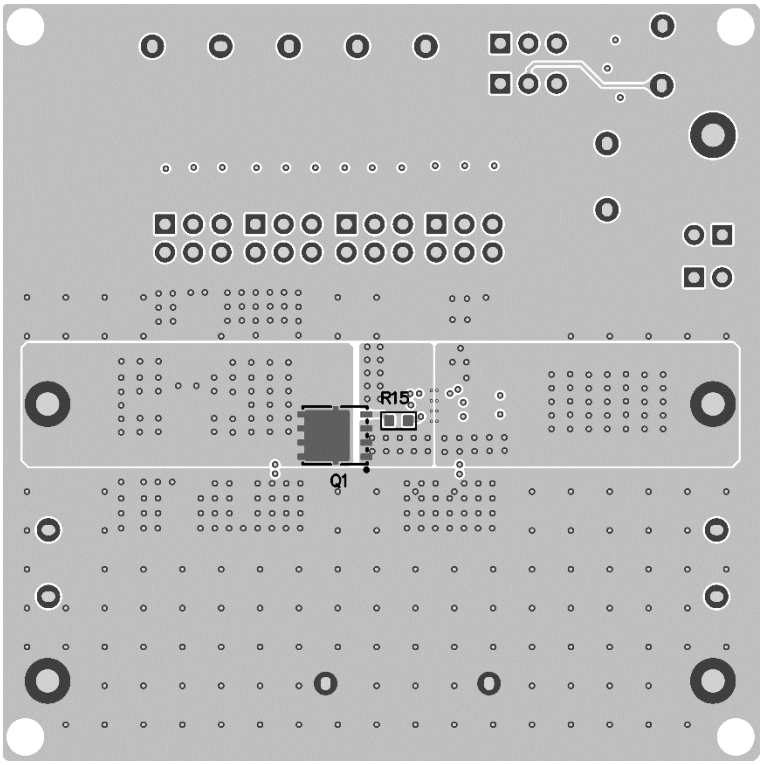


Figure 19. PCB Bottom Layer

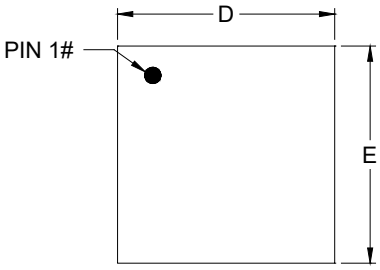
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

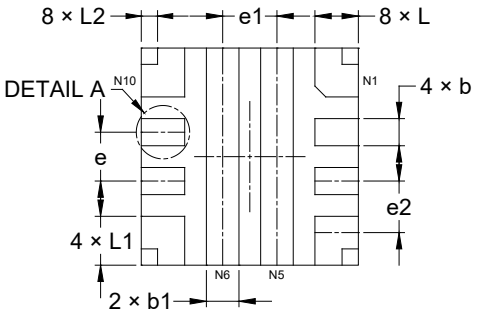
Changes from Original to REV.A (OCTOBER 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

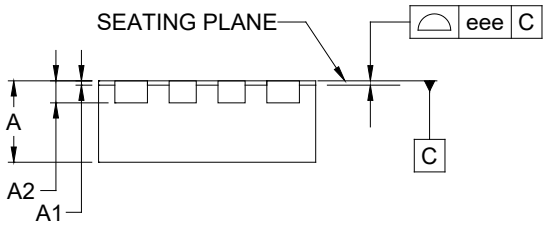
TQFN-2×2-10L



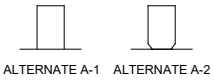
TOP VIEW



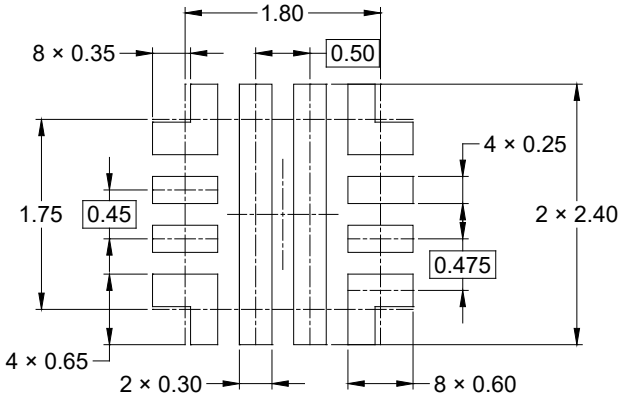
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



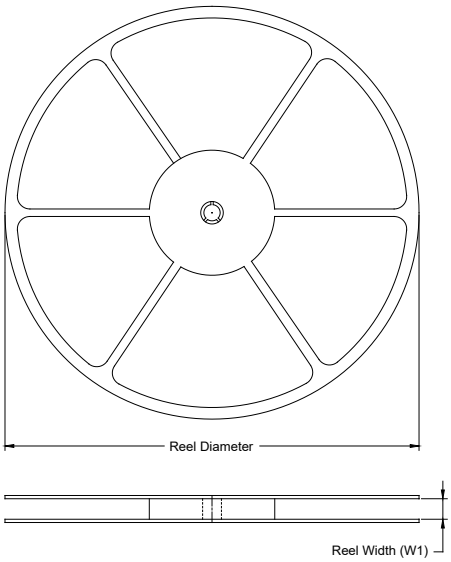
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.250	-	0.350
D	1.900	-	2.100
E	1.900	-	2.100
e	0.450 BSC		
e1	0.500 BSC		
e2	0.475 BSC		
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.150 REF		
eee	0.080		

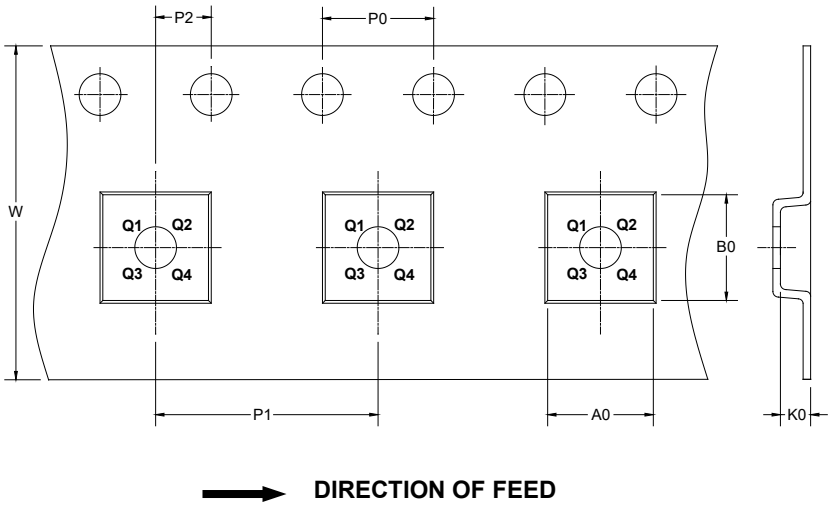
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



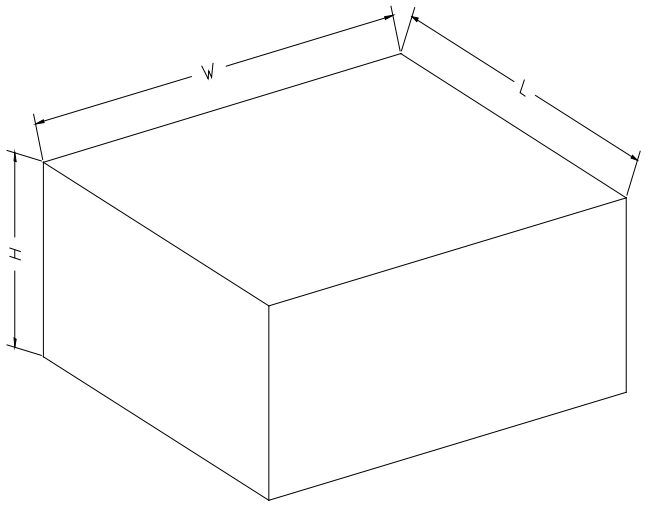
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002