SGM2082
1A, High Accuracy, Low Noise, Low Dropout Voltage Regulator

GENERAL DESCRIPTION

The SGM2082 is a high accuracy, low noise and low dropout linear regulator. It is capable of supplying 1A output current with typical dropout voltage of only 95mV. The operating input voltage range is from 1.4V to 6.5V. The adjustable output voltage range is from 0.8V to 5.2V.

Other features include an open-drain power-good (PG) output, logic-controlled shutdown mode and thermal shutdown protection. The SGM2082 has automatic discharge function to quickly discharge V_{OUT} in the disabled status.

The SGM2082 is available in a Green TDFN-2.5×2.5-10L package. It operates over an operating temperature range of -40℃ to +125℃.

APPLICATIONS

Instruments and Apparatuses
Precision Power Supply
Image Sensor
Consumer Electronics
Audio Player

FEATURES

- **Wide Input Voltage Range: 1.4V to 6.5V**
- **Adjustable Output from 0.8V to 5.2V**
- **1A Output Current**
- **Output Voltage Accuracy: ±0.7% at T_J = +25℃**
- **Low Output Noise: 4.9μV_{RMS} (10Hz to 100kHz)**
- **Low Dropout: 95mV (TYP) at 1A**
- **High PSRR:**
  - **76dB at 1kHz**
  - **47dB at 100kHz**
  - **44dB at 1MHz**
- **Current Limiting and Thermal Protection**
- **Excellent Load and Line Transient Responses**
- **With Output Automatic Discharge**
- **UVLO with Hysteresis**
- **Support Power-Good Indicator Function**
- **Stable with Small Case Size Ceramic Capacitors**
- **Adjustable Start-Up In-Rush Control with Selectable Soft-Start Charging Current**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-2.5×2.5-10L Package**

TYPICAL APPLICATION

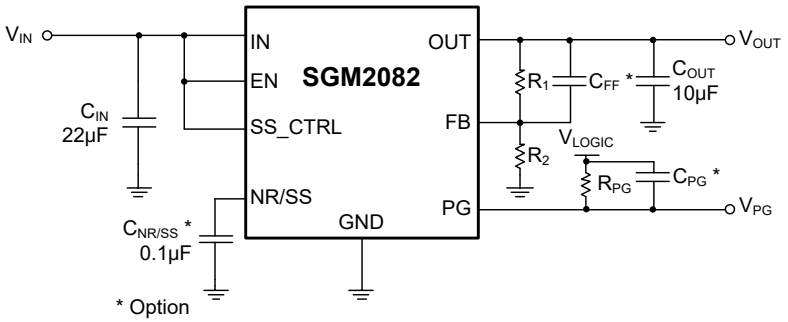


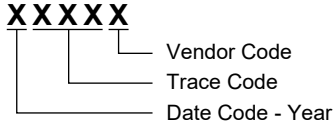
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2082	TDFN-2.5×2.5-10L	-40℃ to +125℃	SGM2082XTHP10G/TR	2082 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, PG, EN, SS_CTRL to GND ..... -0.3V to 7V
NR/SS, OUT to GND ..... -0.3V to MIN(V_{IN} + 0.3V, 6V)
FB to GND ..... -0.3V to 6V
PG Current (sink current into the device)..... 5mA
Package Thermal Resistance
TDFN-2.5×2.5-10L, θ_{JA} ..... 51.2℃/W
TDFN-2.5×2.5-10L, θ_{JB} ..... 23.5℃/W
TDFN-2.5×2.5-10L, $\theta_{JC(TOP)}$ ..... 56.3℃/W
TDFN-2.5×2.5-10L, $\theta_{JC(BOT)}$ ..... 4.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 1.4V to 6.5V
Enable Input Voltage Range ..... 0V to 6.5V
Output Voltage Range ..... 0.8V to 5.2V
Input Effective Capacitance, C_{IN} ..... 10μF (MIN)
Output Effective Capacitance, C_{OUT} ..... 3.3μF to 1000μF
Noise-Reduction Capacitor, $C_{NR/SS}$ ..... 1μF (MAX)
C_{FF} Effective Capacitance..... 100nF (MAX)
Power-Good Pull-Up Resistance ..... 10kΩ to 100kΩ
Operating Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

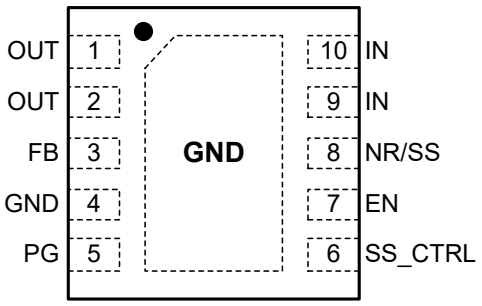
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM2082 (TOP VIEW)



TDFN-2.5×2.5-10L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	OUT	Regulator Output Pin. It is recommended to use a ceramic capacitor with minimum effective capacitance of 3.3μF to ensure stability. This ceramic capacitor should be placed as close as possible to OUT pin.
3	FB	Feedback Input Pin. Connect this pin to the midpoint of an external resistor divider to adjust the output voltage. Place the resistors as close as possible to this pin.
4	GND	Ground.
5	PG	Power-Good Indicator Output Pin. An open-drain, active-high output that indicates the status of V_{OUT}. When the output voltage reaches PG_{HTH} of the target, the PG pin goes into a high-impedance state.
6	SS_CTRL	Soft-Start Control Pin. This pin can be connected to IN pin or GND. Connect this pin to IN pin to provide the $C_{NR/SS}$ with a larger charging current for fast startup. To avoid output overshoot, this pin must be connected to GND when there is no $C_{NR/SS}$.
7	EN	Enable Pin. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. The EN pin must be connected to IN if the enable function is not used.
8	NR/SS	Noise-Reduction and Soft-Start Pin. Using an external capacitor $C_{NR/SS}$ to decouple this pin to GND can not only reduce output noise to very low level but also slow down the V_{OUT} rise like a soft-start behavior.
9, 10	IN	Input Supply Voltage Pin. It is recommended to use a 22μF or larger ceramic capacitor from IN pin to ground to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to IN pin.
Exposed Pad	GND	Exposed Pad. Connect it to GND internally. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAM

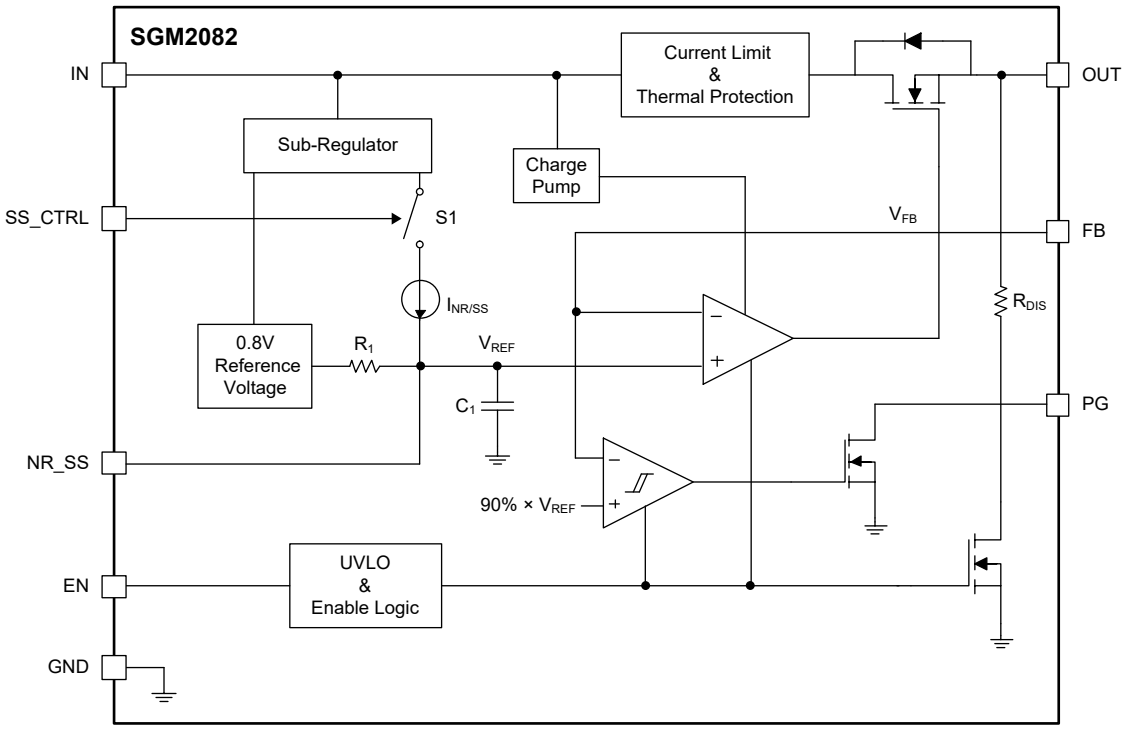


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

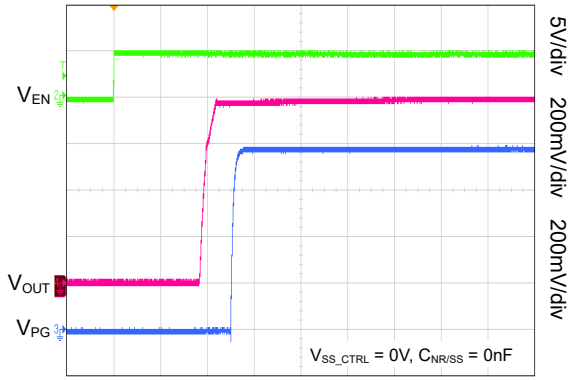
(V_{IN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{EN} = 1.4V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, V_{SS_CTRL} = 0V, and PG pin pulled up to V_{IN} with 100kΩ, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{IN}			1.4		6.5	V
Output Voltage Range	V_{OUT}			0.8		5.2	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = 1.4V to 6.5V, I_{OUT} = 5mA to 1A	T_J = +25℃	-0.7		+0.7	%
			T_J = -40℃ to +125℃	-1		+1	
Feedback Voltage	V_{FB}	V_{IN} = 1.4V to 6.5V, I_{OUT} = 5mA to 1A	T_J = +25℃	0.7944	0.8	0.8056	V
			T_J = -40℃ to +125℃	0.7920	0.8	0.8080	
FB Pin Leakage Current	I_{FB}	V_{IN} = 6.5V, V_{FB} = 0.9V			0.1	100	nA
Input Supply UVLO	V_{UVLO}	V_{IN} rising			1.26	1.39	V
Input Supply UVLO Hysteresis	V_{HYS}				150		mV
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = 1.4V to 6.5V, I_{OUT} = 5mA			0.005	0.12	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT} \times V_{OUT}}$	I_{OUT} = 5mA to 1A			0.025	0.4	%/A
Dropout Voltage	V_{DROP}	V_{FB} = 0V, I_{OUT} = 1A			95	220	mV
Output Current Limit	I_{LIMIT}	V_{IN} = 5.5V, $V_{OUT(NOM)}$ = 5V, V_{OUT} = 90% × $V_{OUT(NOM)}$		1.2	1.7		A
Short-Circuit Current Limit	I_{SHORT}	V_{OUT} = 0V			1.4		A
GND Pin Current	I_{GND}	V_{IN} = 6.5V, I_{OUT} = 0mA			1.9	3	mA
		V_{IN} = 1.4V, I_{OUT} = 1A				3	mA
Shutdown GND Pin Current	I_{SHDN}	V_{IN} = 6.5V, V_{EN} = 0.4V			1.2	10	μA
EN Pin High-Level Input Voltage	V_{IH}	V_{IN} = 1.4V to 6.5V		0.9		6.5	V
EN Pin Low-Level Input Voltage	V_{IL}	V_{IN} = 1.4V to 6.5V		0		0.4	V
EN Pin Current	I_{EN}	V_{IN} = 6.5V, V_{EN} = 0V to 6.5V		-200		200	nA
Output Discharge Resistance	R_{DIS}	V_{EN} = 0V			250		Ω
SS_CTRL Pin Current	I_{SS_CTRL}	V_{IN} = 6.5V, V_{SS_CTRL} = 0V to 6.5V		-200		200	nA
PG High Threshold	PG_{HTH}	V_{OUT} increasing		86	90.5	94	$\%V_{FB}$
PG Pin Hysteresis	PG_{LTH}	V_{OUT} decreasing			1.25		$\%V_{FB}$
PG Pin Low-Level Output Voltage	$V_{PG(LO)}$	V_{OUT} < PG_{LTH}, I_{PG} = -1mA (current into device)				0.4	V
PG Pin Leakage Current	$I_{PG(LKG)}$	V_{OUT} > PG_{HTH}, V_{PG} = 6.5V				1	μA
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = 0V, V_{IN} = 1.4V to 6.5V, V_{SS_CTRL} = 0V		4	6	8	μA
		$V_{NR/SS}$ = 0V, V_{IN} = 1.4V to 6.5V, V_{SS_CTRL} = V_{IN}		60	90	120	μA
Power Supply Rejection Ratio	PSRR	V_{IN} = 2.2V, $V_{OUT(NOM)}$ = 1.2V, I_{OUT} = 1A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, C_{OUT} = 22μF	f = 1kHz		76		dB
			f = 100kHz		47		
			f = 1MHz		44		
Output Voltage Noise	e_n	f = 10Hz to 100kHz, V_{IN} = 1.8V, $V_{OUT(NOM)}$ = 0.8V, I_{OUT} = 1A, $C_{NR/SS}$ = 10nF, C_{OUT} = 22μF			4.9		μV_{RMS}
Thermal Shutdown Temperature	T_{SHDN}	T_J rising			165		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}	Hysteresis			25		℃

TYPICAL PERFORMANCE CHARACTERISTICS

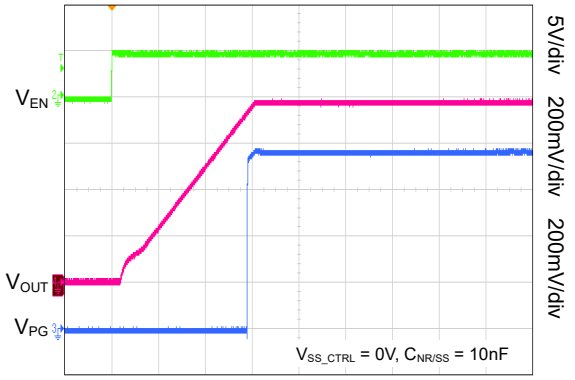
T_J = +25℃, V_{IN} = 1.4V, V_{EN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{SS_CTRL} = 0V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, unless otherwise noted.

Enable Turn-On Response



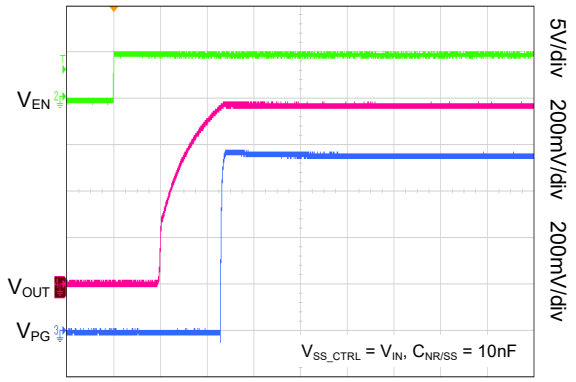
Time (50μs/div)

Enable Turn-On Response



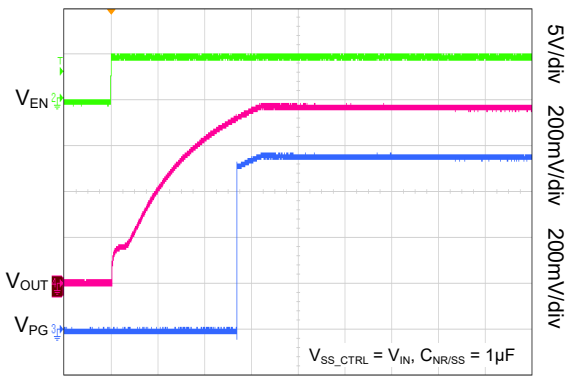
Time (500μs/div)

Enable Turn-On Response



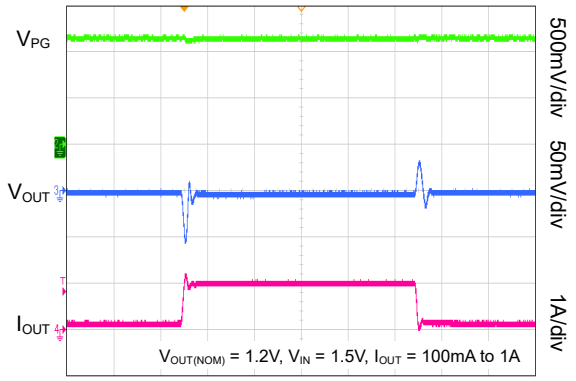
Time (100μs/div)

Enable Turn-On Response



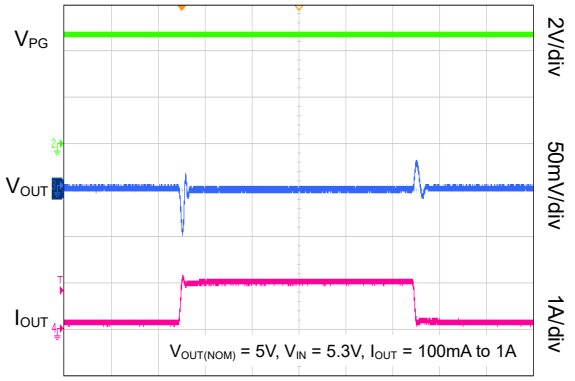
Time (5ms/div)

Load Transient Response



Time (20μs/div)

Load Transient Response

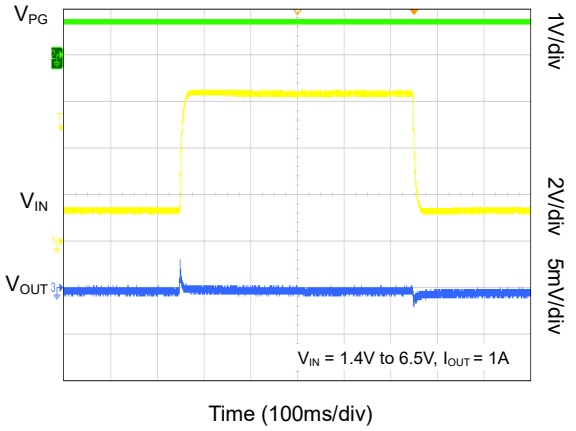


Time (20μs/div)

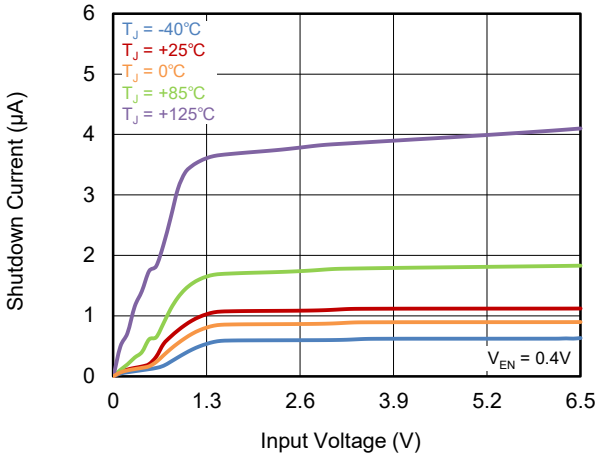
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 1.4V, V_{EN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{SS_CTRL} = 0V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, unless otherwise noted.

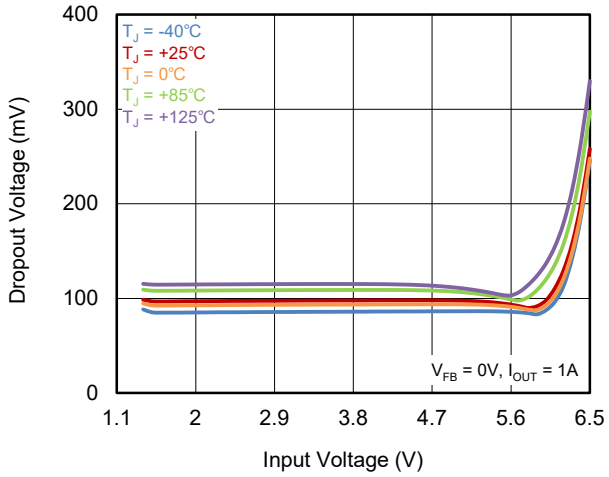
Line Transient Response



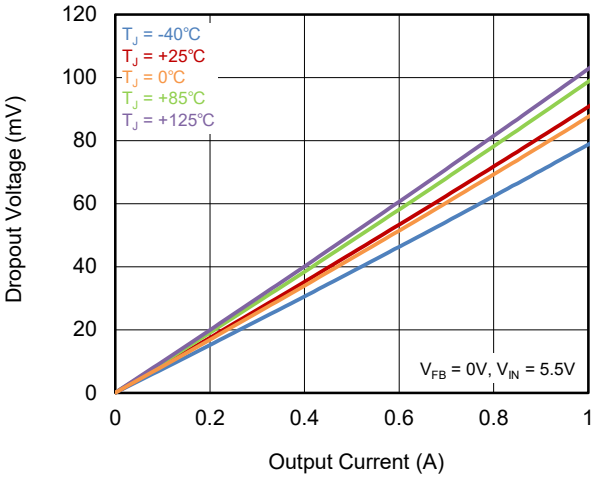
Shutdown Current vs. Input Voltage



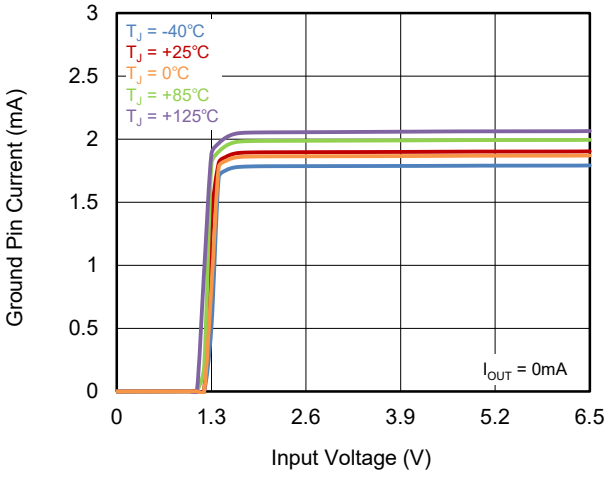
Dropout Voltage vs. Input Voltage



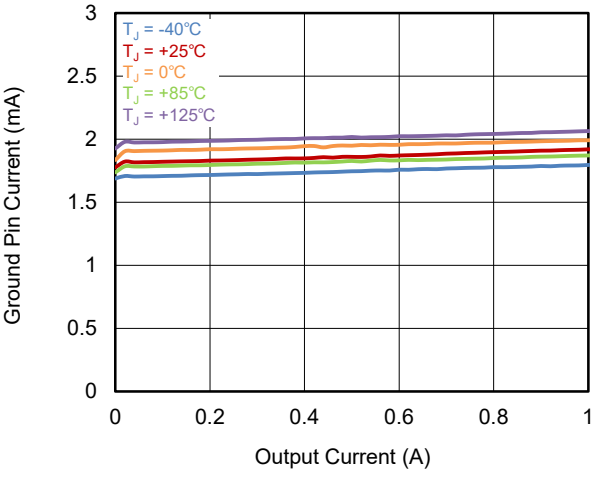
Dropout Voltage vs. Output Current



Ground Pin Current vs. Input Voltage



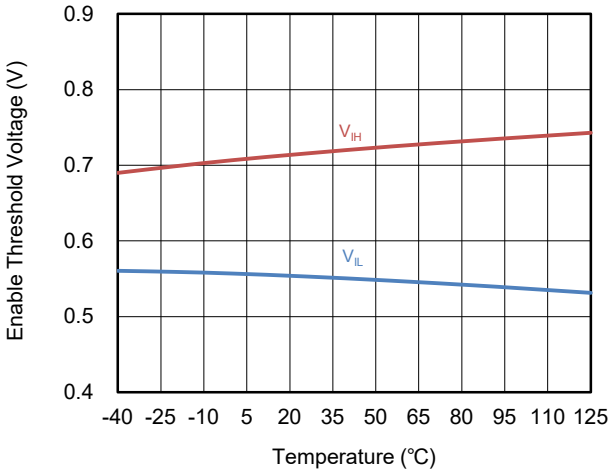
Ground Pin Current vs. Output Current



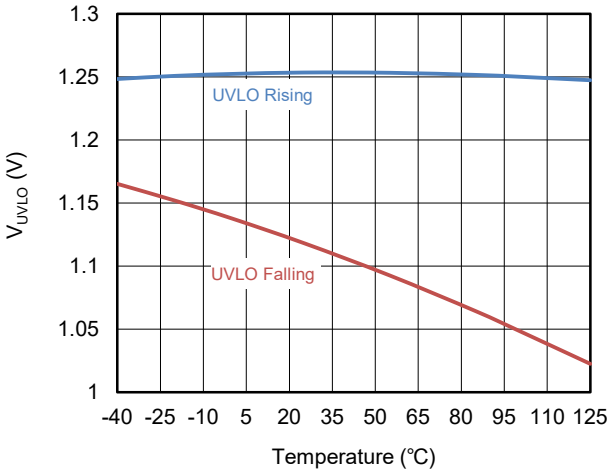
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 1.4V, V_{EN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{SS_CTRL} = 0V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, unless otherwise noted.

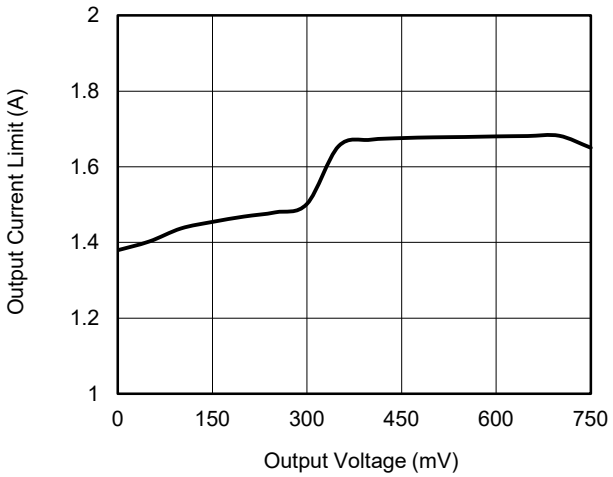
Enable Threshold Voltage vs. Temperature



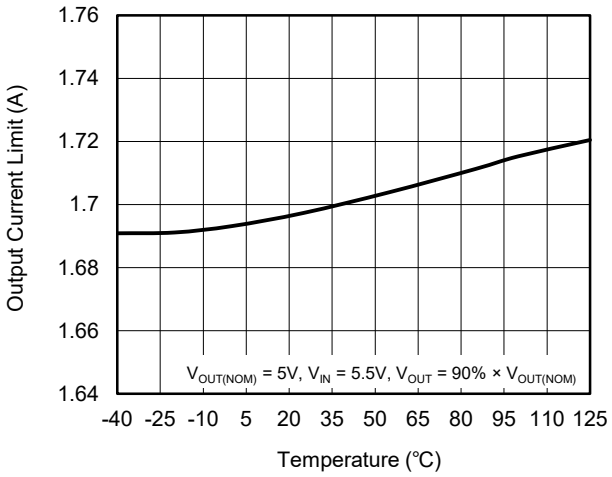
Input UVLO Threshold vs. Temperature



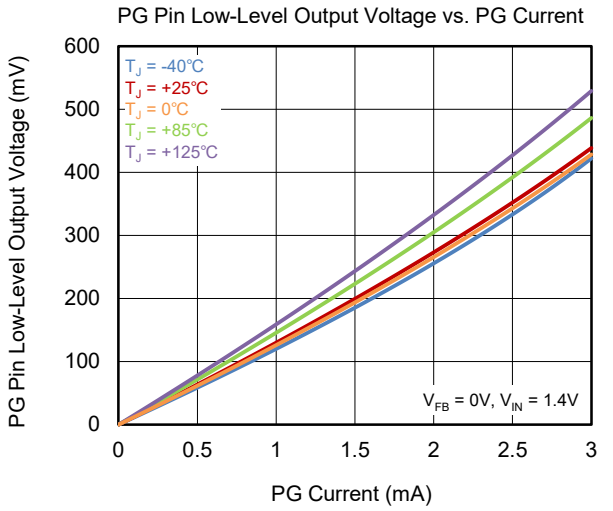
Output Current Limit vs. Output Voltage



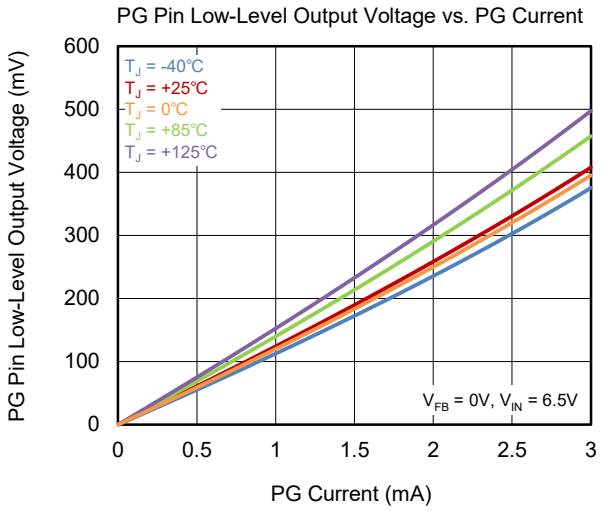
Output Current Limit vs. Temperature



PG Pin Low-Level Output Voltage vs. PG Current



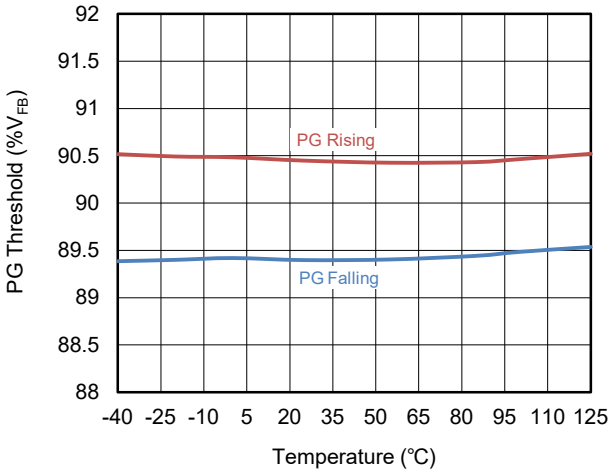
PG Pin Low-Level Output Voltage vs. PG Current



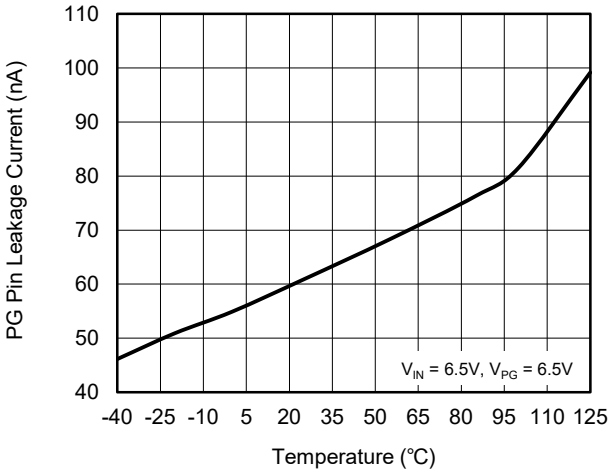
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 1.4V, V_{EN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{SS_CTRL} = 0V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, unless otherwise noted.

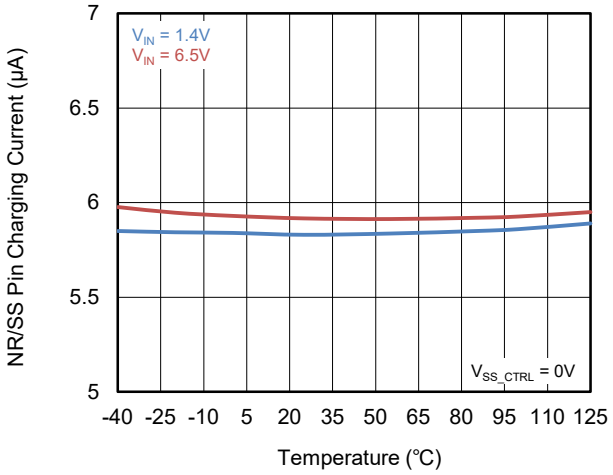
PG Threshold vs. Temperature



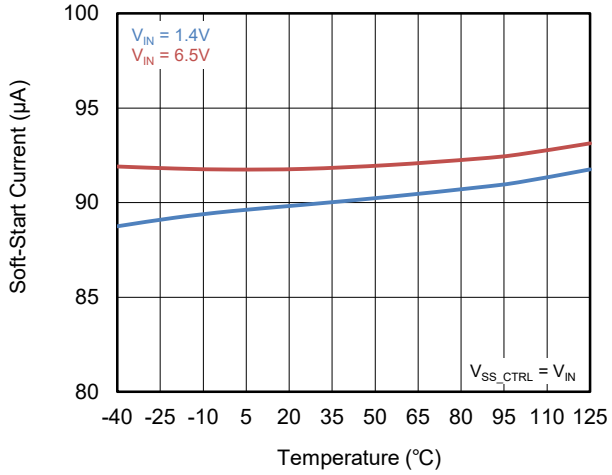
PG Pin Leakage Current vs. Temperature



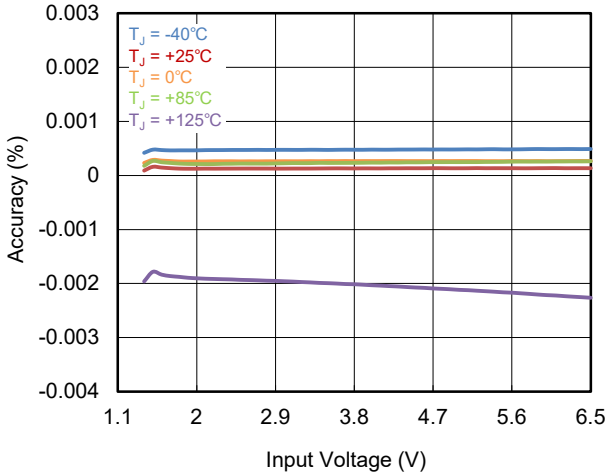
Soft-Start Current vs. Temperature



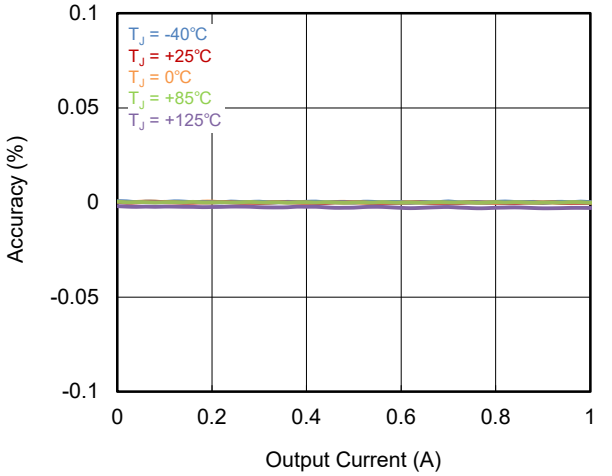
Soft-Start Current vs. Temperature



Output Voltage vs. Input Voltage



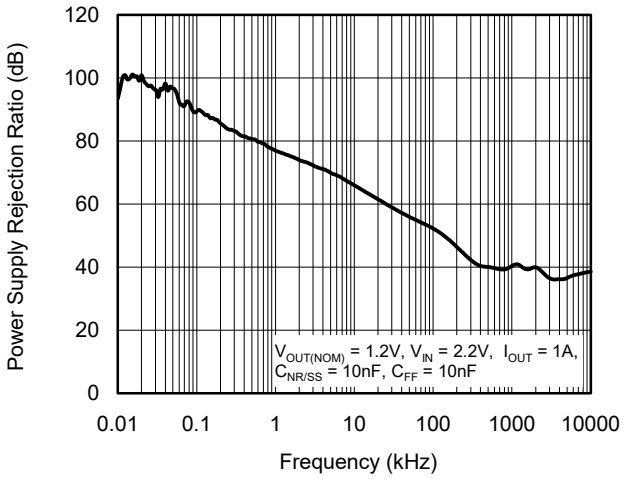
Output Voltage vs. Output Current



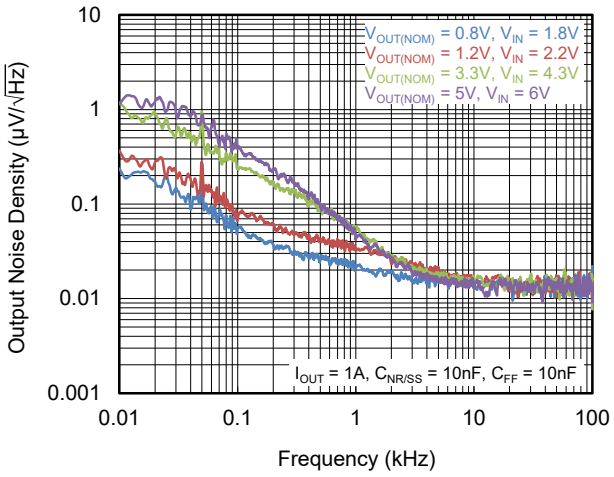
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 1.4V, V_{EN} = 1.4V, $V_{OUT(NOM)}$ = 0.8V, V_{SS_CTRL} = 0V, I_{OUT} = 5mA, C_{OUT} = 10μF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, unless otherwise noted.

Power Supply Rejection Ratio vs. Frequency



Output Noise Density vs. Frequency



APPLICATION INFORMATION

The SGM2082 is a high accuracy, low noise and low dropout linear regulator and provides 1A output current. These features make the device a reliable solution to solve many challenging problems in the generation of clean and accurate power supply. The high performance also makes the SGM2082 useful in a variety of applications. The SGM2082 provides protection functions for output overload and overheating.

The SGM2082 provides an EN pin as an external chip enable control to enable/disable the device. When the regulator is in shutdown state, the shutdown current consumes as low as 1.2μA (TYP).

Input Capacitor Selection (C_{IN})

The input decoupling capacitor should be placed as close as possible to the IN pin to ensure the device stability. 22μF or larger X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When V_{IN} is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings. For C_{OUT} with larger capacitance, it is recommended to choose the larger capacitance C_{IN}.

Output Capacitor Selection (C_{OUT})

One or more output capacitors are required to maintain the stability of the LDO, and the output capacitors should be placed as close as possible to the OUT pin. In addition, in order to obtain the best transient performance, it is recommended to use X7R and X5R ceramic capacitors as output capacitors. Ceramic capacitors have low equivalent series resistance (ESR), excellent temperature and DC bias characteristics. However, it cannot be ignored that the effective capacitance of ceramic capacitors is affected by temperature, DC bias and package size.

For example, Figure 3 shows the capacitance and DC bias and temperature characteristics of 0805, 10V, 10μF±10%, X7R capacitor. Therefore, it is necessary to evaluate whether the effective capacitance of the output capacitor can meet the stability requirements of the LDO in practical applications. In general, a capacitor in higher voltage rating and a larger package exhibits better stability, and the effective capacitance can be obtained from the manufacturer datasheet.

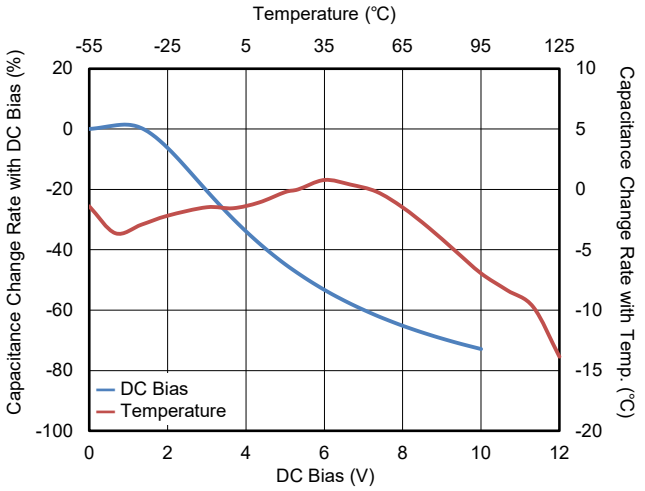


Figure 3. Capacitance vs. DC Bias and Temperature Characteristics

The SGM2082 requires a minimum effective capacitance of 3.3μF for C_{OUT} to ensure stability. Additionally, C_{OUT} with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The SGM2082 is designed for a programmable, monotonic soft-start time of output rising, it can be achieved via an external capacitor ($C_{NR/SS}$) on the NR/SS pin. Using an external $C_{NR/SS}$ is recommended for general application. It is not only for the in-rush current minimization but also helps reduce the noise component from internal reference. The soft start ramp time is determined by $I_{NR/SS}$ and $C_{NR/SS}$, and can be calculated with the equation:

$$t_{SS} = (0.8 \times C_{NR/SS}) / I_{NR/SS} \quad (1)$$

Enable Operation

The SGM2082 uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 0.4V, the device is in shutdown state. There is no current flowing from IN to OUT pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 250Ω (TYP) resistor and the PG output is pulled down.

When the EN pin voltage is higher than 0.9V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

APPLICATION INFORMATION (continued)

Adjustable Regulator

The output voltage of the SGM2082 can be adjusted from 0.8V to 5.2V. The FB pin will be connected to two external resistors as shown in Figure 4. The output voltage is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

where:

V_{OUT} is output voltage and V_{FB} is the internal voltage reference, V_{FB} = 0.8V.

One parallel capacitor (C_{FF}) with R_1 can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the output noise. Use R_2 ≤ 10kΩ to maintain a minimum load of 80μA.

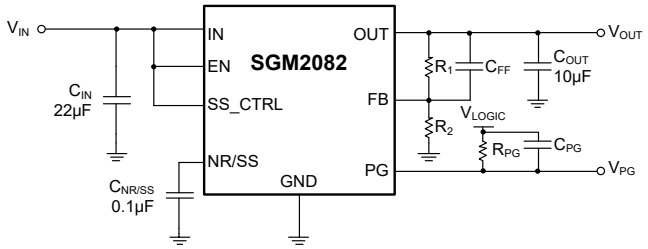


Figure 4. Adjustable Output Voltage Application

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before V_{IN} rises above the V_{UVLO} threshold. The UVLO circuit responds quickly to glitches on the IN pin and attempts to disable the output of the device if any of these rails collapses. The local input capacitance prevents severe brownouts in most applications. When the SGM2082 enters UVLO, the PG output is pulled down.

Power-Good Function

The SGM2082 features PG function for monitoring the feedback voltage, so as to reflect the state of the output voltage. When the output voltage is lower than PG_{LTH}, the PG pin open-drain engages and pulls the PG pin close to GND. When the output voltage is higher than PG_{HTH}, the PG pin is indicated as high impedance. Connecting the PG pin to an external power supply via a pull-up resistor enables any downstream device to receive a power-good valid logic signal for sequencing. The resistance range of the pull-up resistor is recommended to be between 10kΩ and 100kΩ.

When an external feed-forward capacitor (C_{FF}) is added in application, the total LDO startup time constant increases by approximately 3 × R_1 × C_{FF}.

If the Power-Good (PG) output time constant remains unchanged, the PG signal may not accurately indicate whether V_{OUT} has reached the expected voltage. To ensure a valid PG output, the following design configurations must be implemented to match the time constants.

Add a PG delay capacitor (C_{PG}) and connect C_{PG} in parallel with the PG pull-up resistor (R_{PG}) refer to Figure 4. Ensure the following condition is met:

$$3 \times R_{PG} \times C_{PG} \geq 3 \times R_1 \times C_{FF} \quad (3)$$

Figure 5 shows the differences in PG signals when C_{FF} and C_{PG} are added. In Figure 5, t_{REF} is the time that takes for the V_{FB} voltage to rise from 0V to 90.5% × V_{REF}, t_{CFF} is the startup time contributed by C_{FF}.

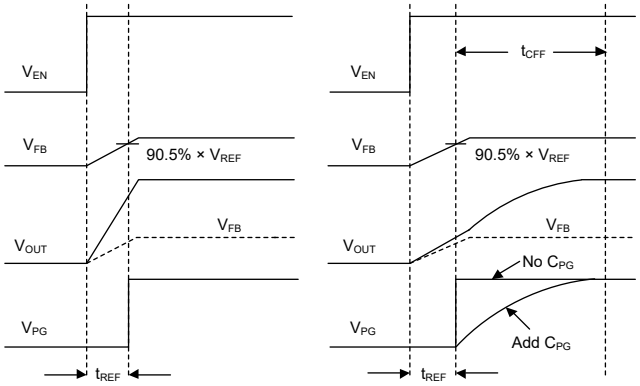


Figure 5. Typical Power-Good Timing Diagram

The PG output is pulled down when the SGM2082 is in one of the following states, including disabled, thermal shutdown, or UVLO.

APPLICATION INFORMATION (continued)

Reverse Current Protection

The power transistor has an inherent body diode. This body diode will be forward biased when V_{OUT} > (V_{IN} + 0.3V). When V_{OUT} > (V_{IN} + 0.3V), the reverse current flowing from the OUT pin to the IN pin will damage the SGM2082. If V_{OUT} > (V_{IN} + 0.3V) event would happen in system, one external Schottky diode will be added between OUT pin and IN pin in circuit design to protect the SGM2082.

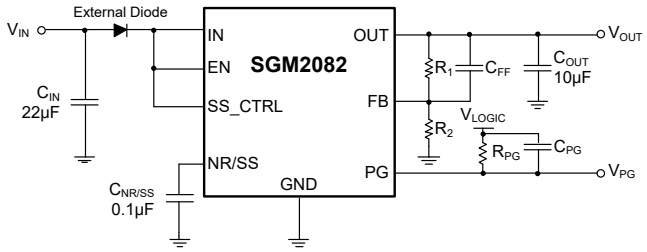


Figure 6. Reverse Protection Reference Design

Output Current Limit Protection

When overload events happen, the output current is internally limited to 1.7A (TYP). When the OUT pin is shorted to ground, the output current is internally limited to 1.4A (TYP).

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM2082 will be in shutdown state and it will remain in this state until the die temperature decreases to +140℃. When the device enters thermal shutdown, the PG output is pulled low.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM2082 can be calculated by the equation $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM2082 is affected by many factors, including the difference between junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (4)$$

REVISION HISTORY

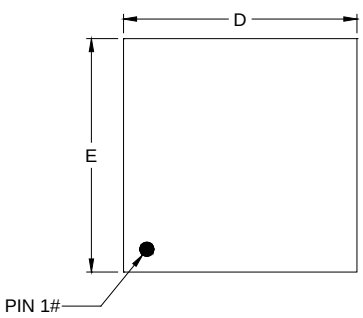
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2025 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	5

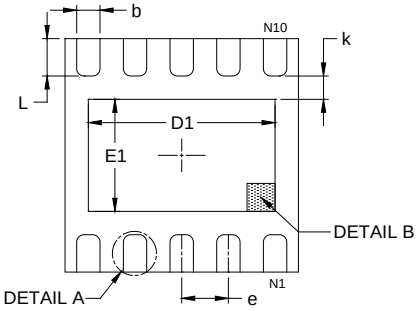
Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

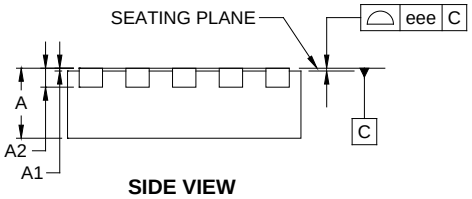
TDFN-2.5×2.5-10L



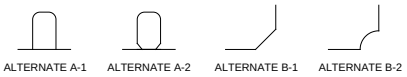
TOP VIEW



BOTTOM VIEW

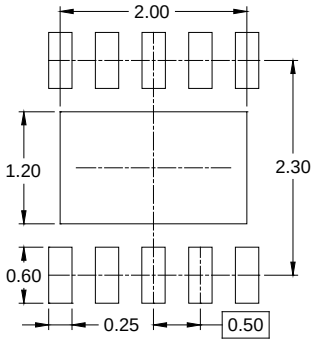


SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

DETAIL B
ALTERNATE PIN1 CONSTRUCTION



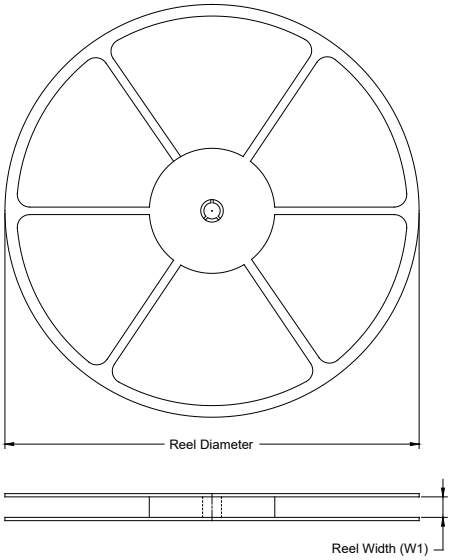
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	2.400	-	2.600
E	2.400	-	2.600
D1	1.900	-	2.100
E1	1.100	-	1.300
L	0.300	-	0.500
k	0.250 REF		
e	0.500 BSC		
eee	0.080		

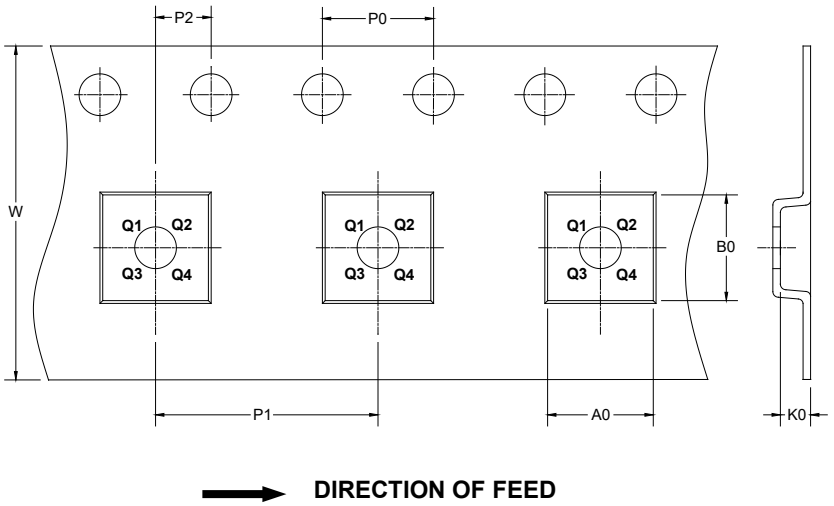
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



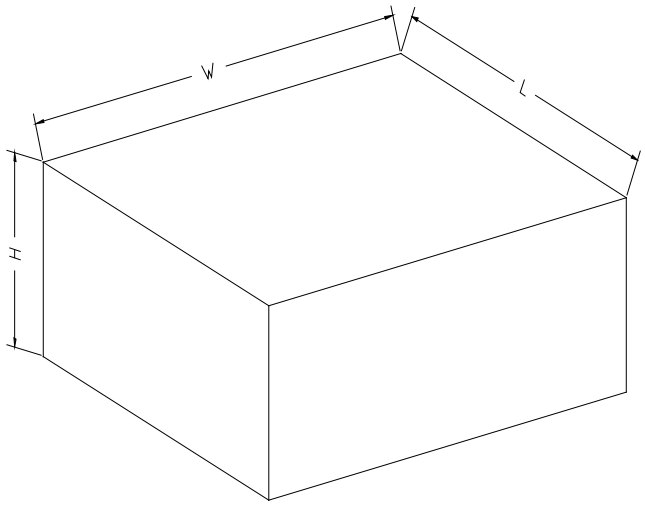
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2.5×2.5-10L	7"	12.4	2.75	2.75	0.85	4.0	4.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002