SGM61162
4.5V to 18V Input, 6A Output Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61162 is an adaptive constant on-time control (ACOT) synchronous Buck converter with a wide input voltage range of 4.5V to 18V. This device has 6A output current capability and operates at pseudo-fixed frequency. It is an easy-to-use device with power switches and internal compensation circuit, which are all integrated in a small 6-pin package, and supports low equivalent series resistance (ESR) output capacitors. A typical 2ms soft-start ramp is also included to minimize the inrush current.

Protection features include cycle-by-cycle current limit, hiccup mode short-circuit protection and thermal shutdown in case of excessive power dissipation.

The SGM61162A operates in pulse skip mode (PSM) at light load to boost light load efficiency, while the SGM61162B operates in forced pulse width modulation (FPWM) mode over the full load range to maintain constant frequency and reduce output voltage ripple.

The SGM61162 is available in a Green TSOT-23-6 package.

FEATURES

- **Wide 4.5V to 18V Input Voltage Range**
- **0.6V to 9V Output Voltage Range**
- **6A Continuous Output Current**
- **Integrated 32mΩ/20mΩ Power MOSFETs**
- **Shutdown Current: 2.8μA (TYP)**
- **2ms Internal Soft-Start Time**
- **Pseudo-Fixed 420kHz Switching Frequency**
- **Adaptive Constant On-Time Mode Control**
- **SGM61162A: PSM at Light Load Condition**
- **SGM61162B: FPWM at Light Load Condition**
- **Cycle-by-Cycle Over-Current Limit**
- **Thermal Shutdown with Auto Recovery**
- **Active Output Discharge**
- **Available in a Green TSOT-23-6 Package**

APPLICATIONS

Set-Top Boxes
Access Point Router
Monitor and Televisions
IP Cameras

SIMPLIFIED SCHEMATIC

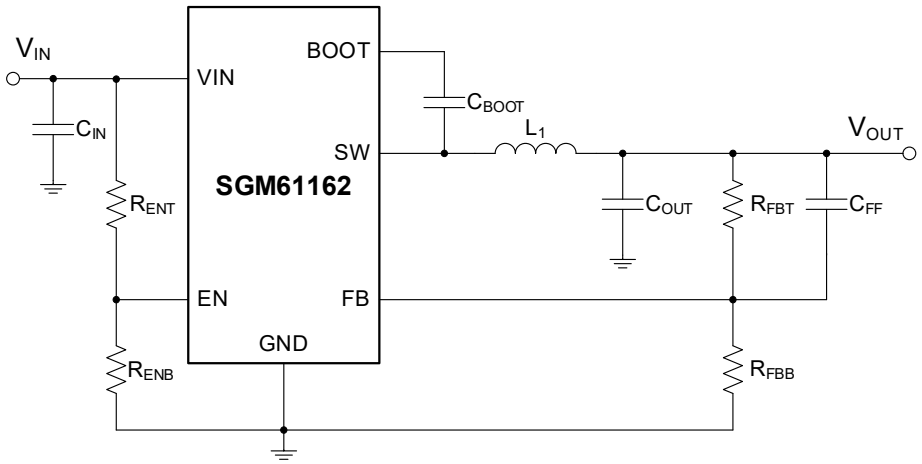


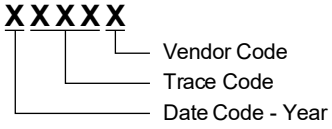
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61162A	TSOT-23-6	-40℃ to +125℃	SGM61162AXTN6G/TR	1O4 XXXXX	Tape and Reel, 3000
SGM61162B	TSOT-23-6	-40℃ to +125℃	SGM61162BXTN6G/TR	1SZ XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- VIN Pin ..... -0.3V to 19V
- EN Pin ..... -0.3V to 19V
- BOOT-SW Voltages ..... -0.3V to 6V
- SW Voltage ..... -0.3V to 19V
- SW Voltage (20ns Transient) ..... -3.5V to 21V
- FB Voltage ..... -0.3V to 5.5V

Package Thermal Resistance
- TSOT-23-6, θ_{JA} ..... 99.9℃/W
- TSOT-23-6, θ_{JB} ..... 21.8℃/W
- TSOT-23-6, θ_{JC} ..... 66.3℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 4.5V to 18V
Output Voltage Range, V_{OUT} ..... 0.6V to 9V
Output Current Range, I_{OUT} ..... 0A to 6A
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

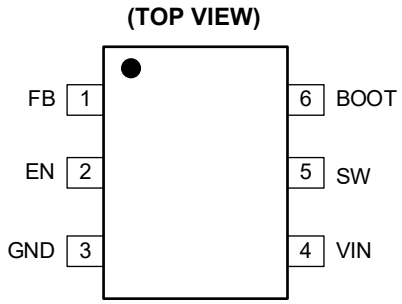
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	FB	I	Feedback Pin for Setting the Output Voltage. Tap an output feedback resistor divider to this pin.
2	EN	I	Active-High Enable Input. Pull up to a logic-high voltage (not higher than 18V) to enable the device, pull down to disable it. Input UVLO level can be programmed using a resistor divider from VIN. Do not leave it floating.
3	GND	G	Device Ground Reference Pin.
4	VIN	P	Supply Input. Connect VIN pin to a power source with 4.5V to 18V voltage range. Decouple VIN pin to GND as close as possible with a high frequency, low ESR ceramic capacitor (X5R or higher grade is recommended).
5	SW	P	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
6	BOOT	O	Bootstrap Pin. Bootstrap supply for high-side driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Input Voltage Range	V_{IN}		4.5		18	V
Under-Voltage Lockout Threshold	V_{IN_UVLO}	Rising threshold		4.15	4.50	V
		Falling threshold	3.45	3.8		
Input UVLO Hysteresis	V_{IN_HYS}	Hysteresis		0.35		V
Supply Current						
Operating Quiescent Current	I_Q	V_{IN} current, V_{EN} = 2V, V_{FB} = 1V, SGM61162A		170	240	μA
		V_{IN} current, V_{EN} = 2V, V_{FB} = 1V, SGM61162B		350		
Shutdown Supply Current	I_{SD}	V_{IN} current, V_{EN} = 0V		2.8	8	μA
Enable (EN Pin)						
EN Rising Threshold Voltage	V_{EN_H}		1.08	1.2	1.32	V
EN Falling Threshold Voltage	V_{EN_L}		0.9	1.0	1.1	V
EN Falling Hystersis Voltage	V_{EN_HYS}			0.2		V
Input Leakage Current at EN Pin	I_{EN}	V_{EN} = 2V		10		nA
Reference Voltage						
Reference Voltage	V_{REF}	T_J = +25℃	592	604	616	mV
		T_J = -40℃ to +125℃	589	604	619	
FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
Output Discharge Resistance	R_{DIS}	V_{EN} = 0.9V		60		Ω
MOSFET						
High-side Switch On-Resistance	R_{DSON_HS}			32	56	mΩ
Low-side Switch On-Resistance	R_{DSON_LS}			20	38	mΩ
Switching Node (SW Pin)						
Minimum On Time (1)	t_{ON_MIN}			65		ns
Minimum Off Time (1)	t_{OFF_MIN}			120		ns
Soft-Start						
Soft-Start Time (1)	t_{SS}	Internal soft-start time		2		ms
Frequency						
Switching Frequency	f_{SW}	V_{OUT} = 3.3V, continuous conduction mode		420		kHz
Current Limit						
Valley Inductor Current Limit	I_{LS_LIMIT}	Initial	5.8	6.7		A
Zero Cross Current	I_{LS_ZC}	SGM61162A only		200		mA
Negative Current Limit	I_{LS_NEG}	SGM61162B only		-3.5		A
Output Under-Voltage						
Output UVP Threshold	V_{UVP}	Hiccup detect threshold, percentage of V_{REF}		33		%
Output UVP Delay (1)	t_{UVP_DLY}			100		μs
Hiccup Time before Restart (1)	t_{HICCUP_RE}			10		ms
Thermal Shutdown						
Thermal Shutdown Threshold (1)	T_{SD}			155		℃
Thermal Shutdown Hysteresis (1)	T_{HYS}			20		℃

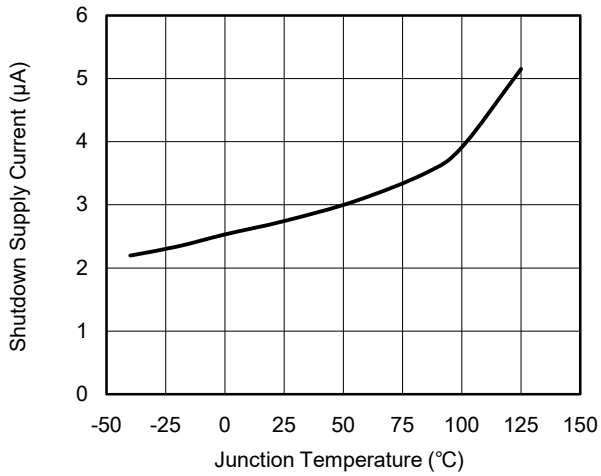
NOTE:

1. Guaranteed by design, not tested in production.

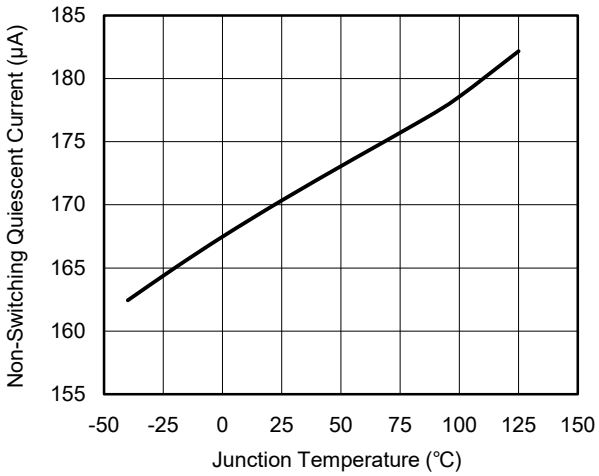
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

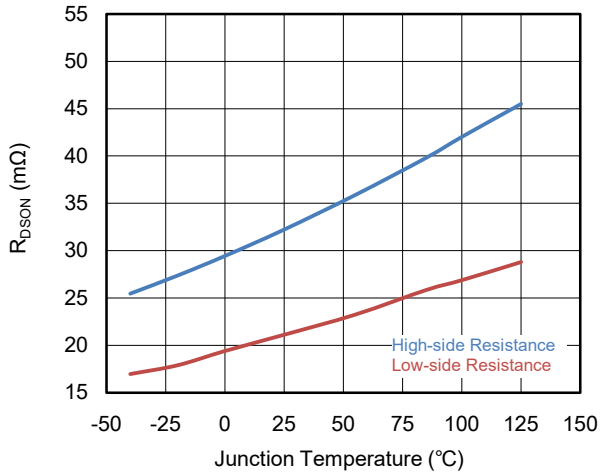
Shutdown Supply Current vs. Temperature



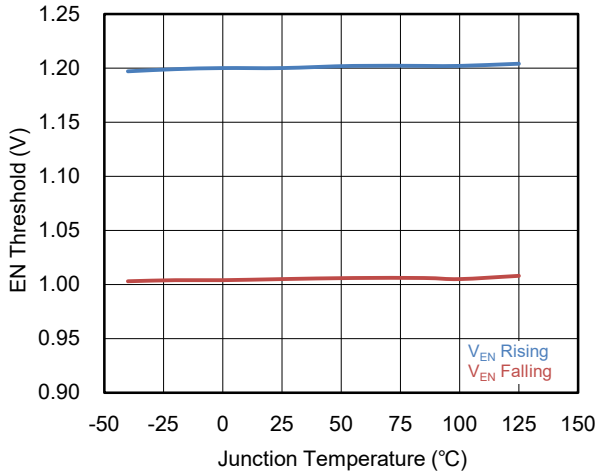
Non-Switching Quiescent Current vs. Temperature



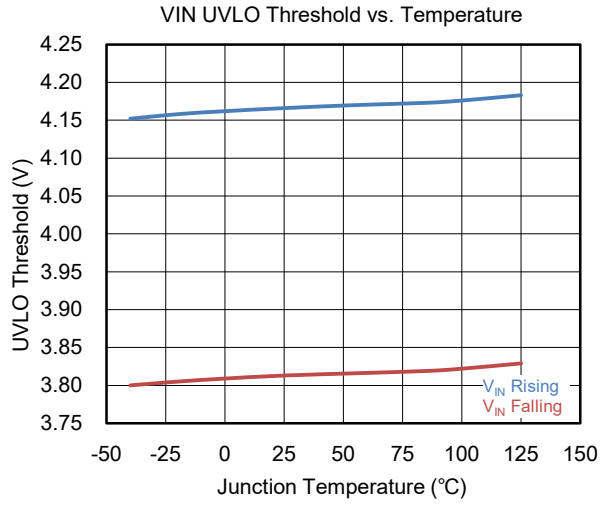
On-Resistance vs. Temperature



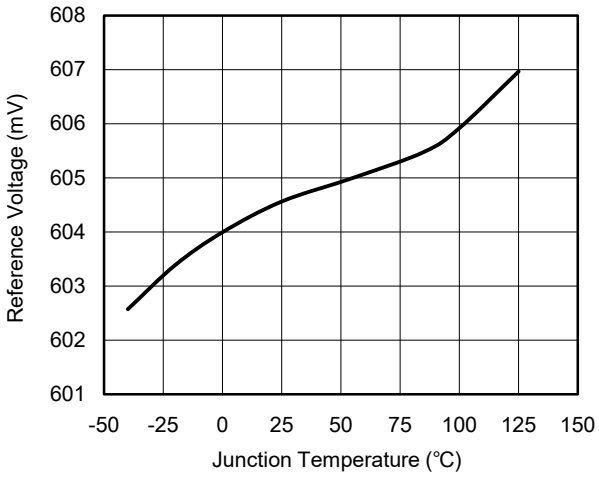
EN Threshold vs. Temperature



VIN UVLO Threshold vs. Temperature



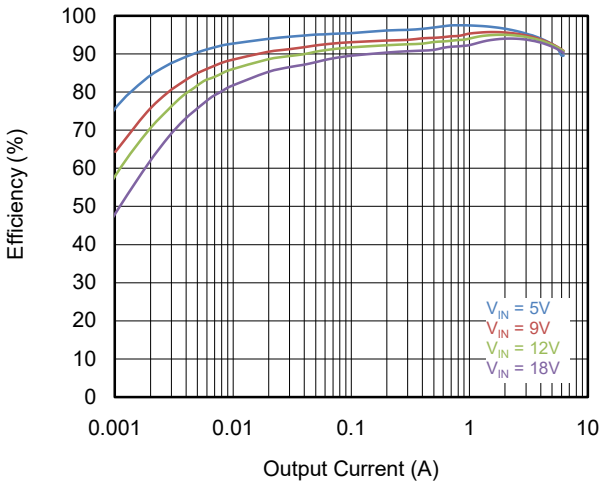
Reference Voltage vs. Temperature



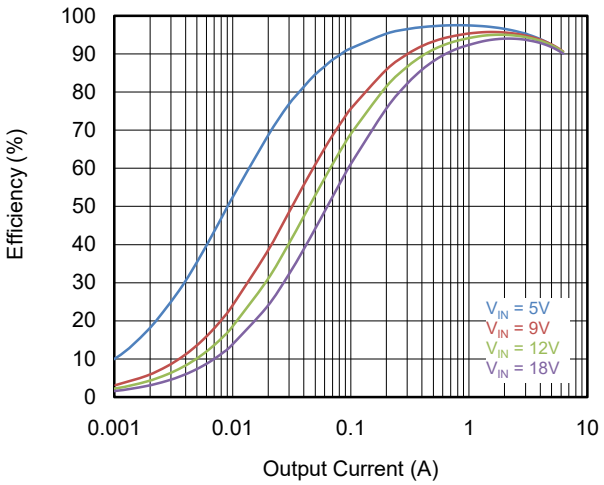
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

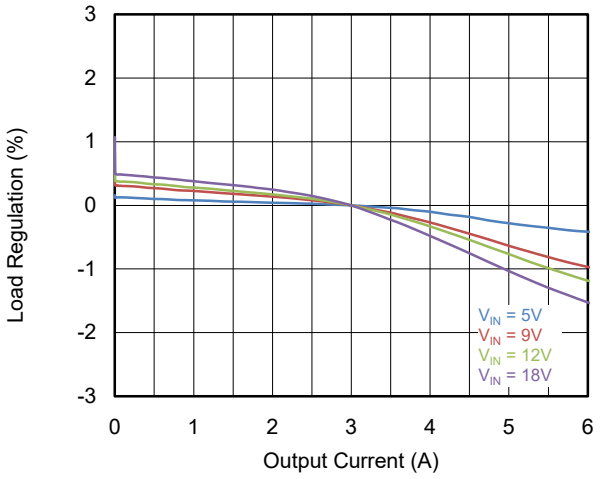
Efficiency vs. Output Current (SGM61162A)



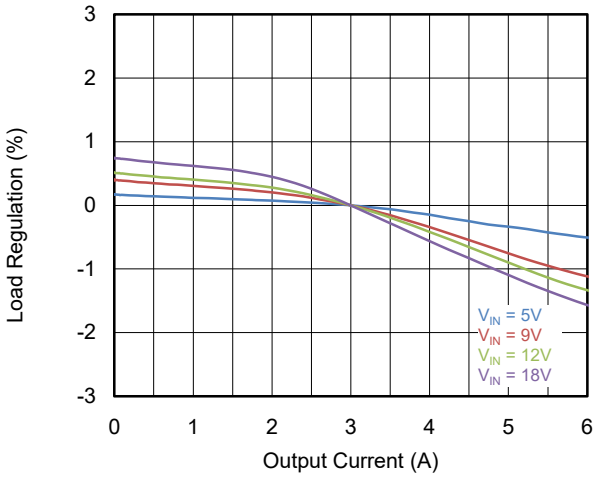
Efficiency vs. Output Current (SGM61162B)



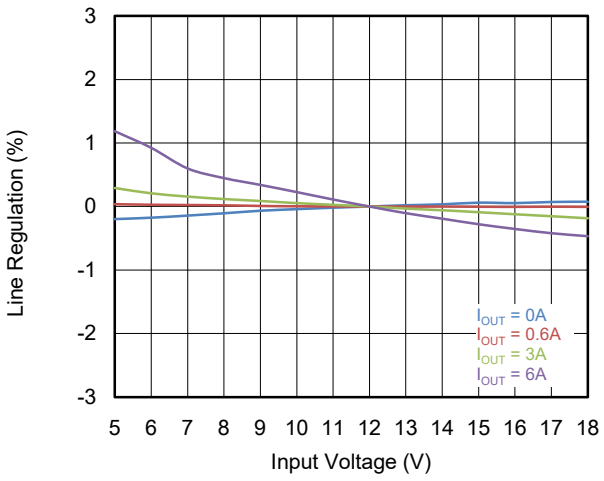
Load Regulation (SGM61162A)



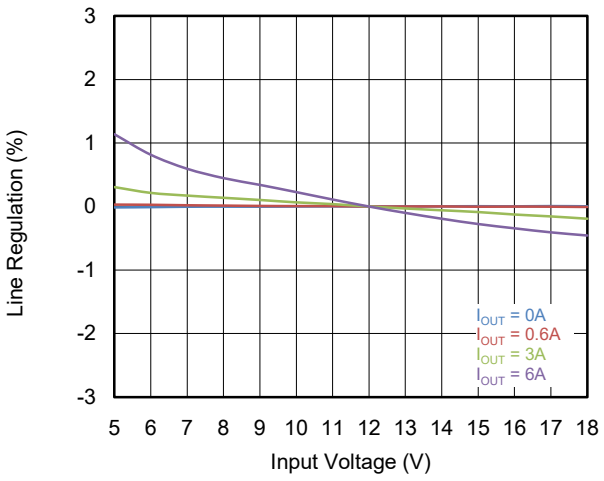
Load Regulation (SGM61162B)



Line Regulation (SGM61162A)



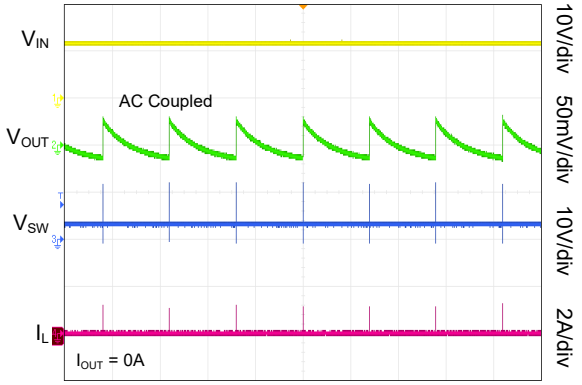
Line Regulation (SGM61162B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

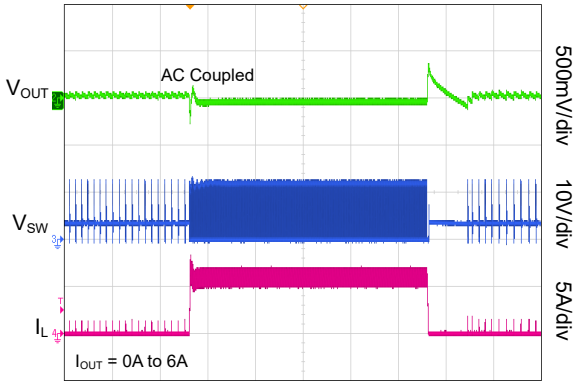
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

Output Voltage Ripple (SGM61162A)



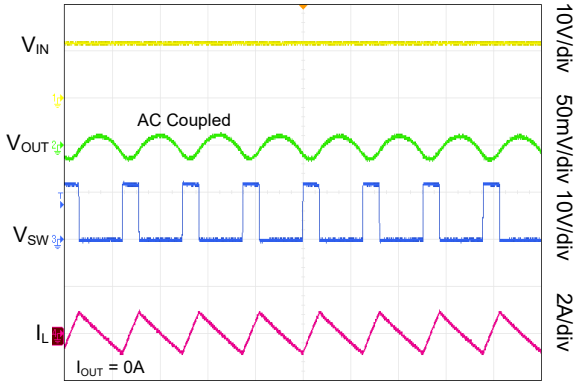
Time (20ms/div)

Load Transient (SGM61162A)



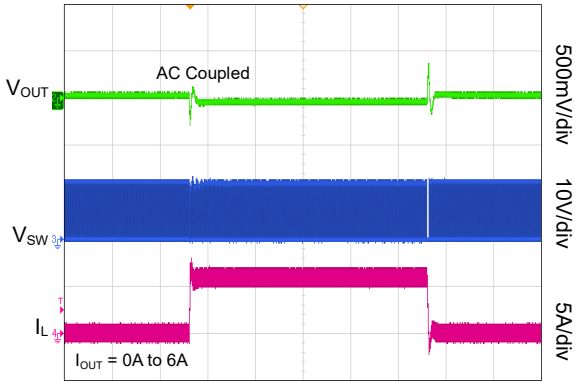
Time (200μs/div)

Output Voltage Ripple (SGM61162B)



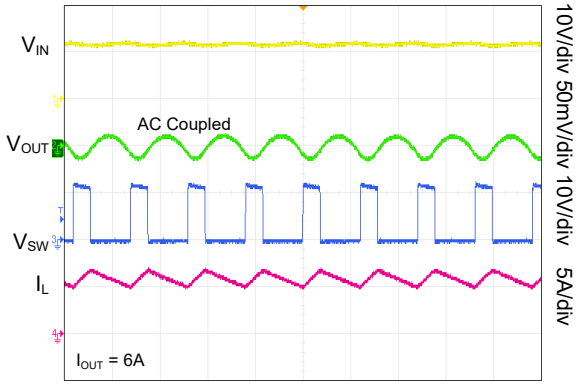
Time (2μs/div)

Load Transient (SGM61162B)



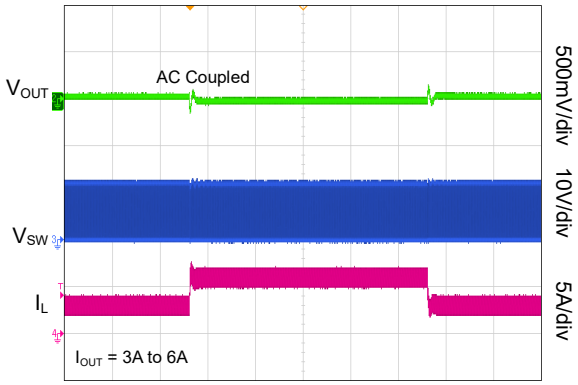
Time (200μs/div)

Output Voltage Ripple



Time (2μs/div)

Load Transient

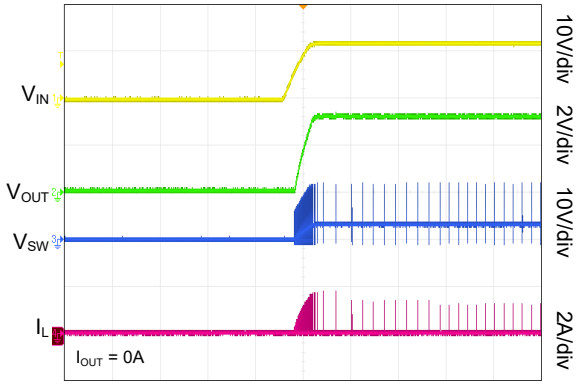


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

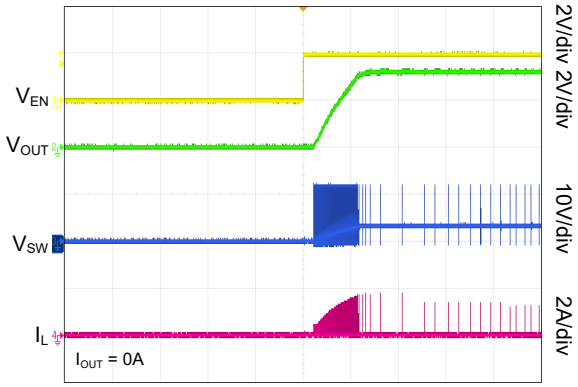
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

VIN Startup (SGM61162A)



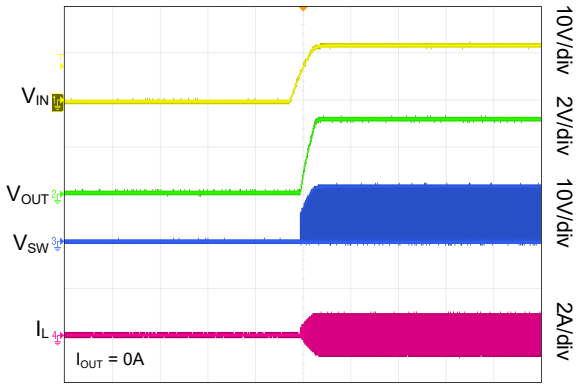
Time (5ms/div)

EN Startup (SGM61162A)



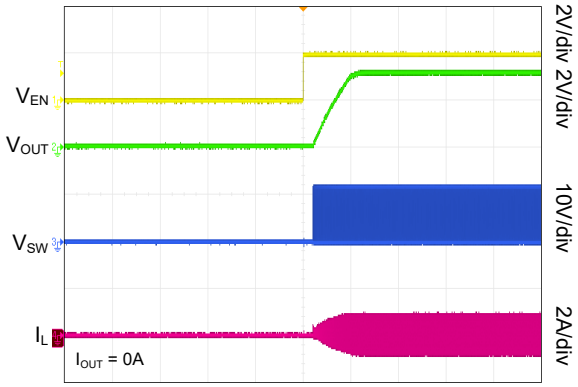
Time (2ms/div)

VIN Startup (SGM61162B)



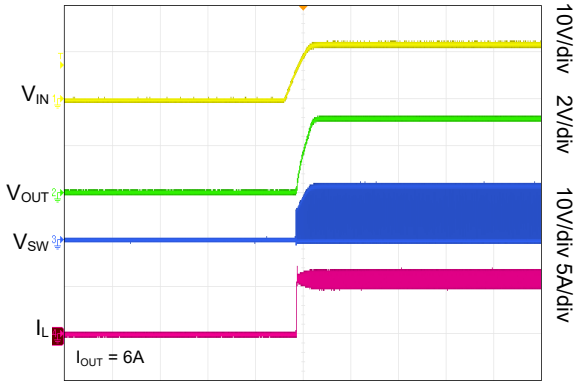
Time (5ms/div)

EN Startup (SGM61162B)



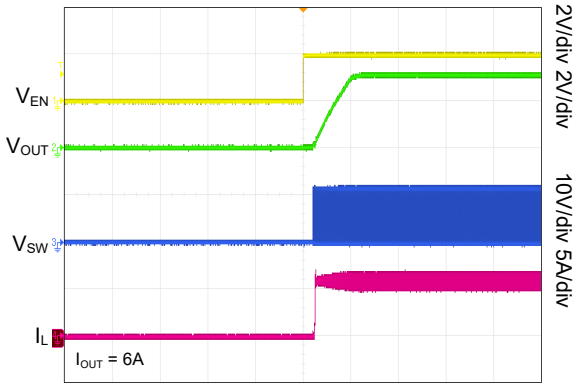
Time (2ms/div)

VIN Startup



Time (5ms/div)

EN Startup

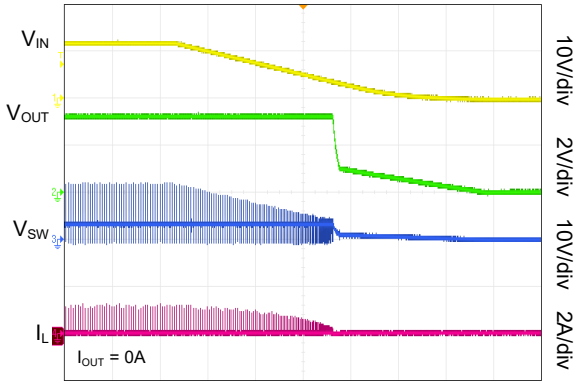


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

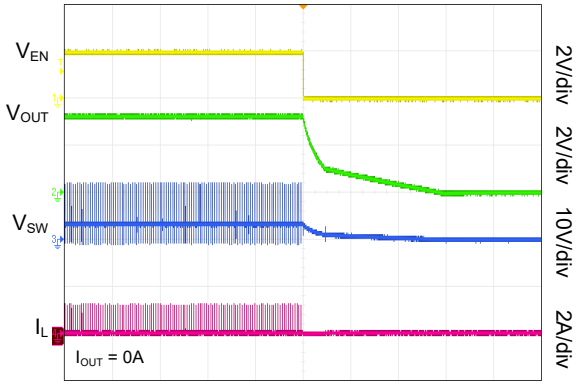
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

VIN Shutdown (SGM61162A)



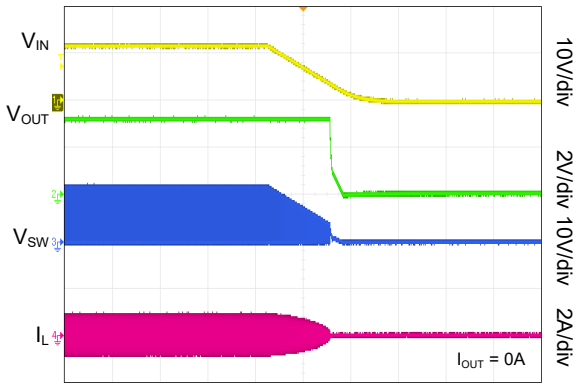
Time (20ms/div)

EN Shutdown (SGM61162A)



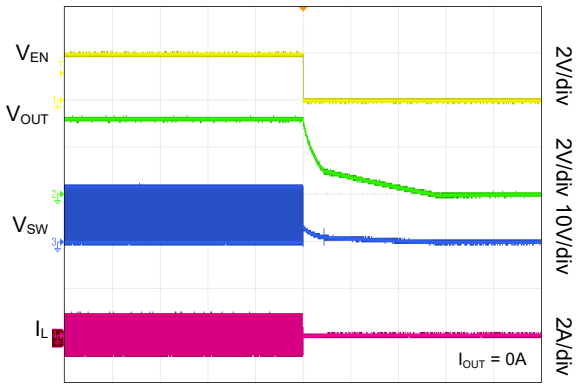
Time (5ms/div)

VIN Shutdown (SGM61162B)



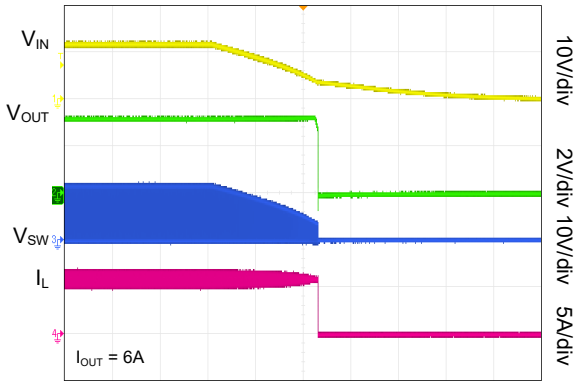
Time (50ms/div)

EN Shutdown (SGM61162B)



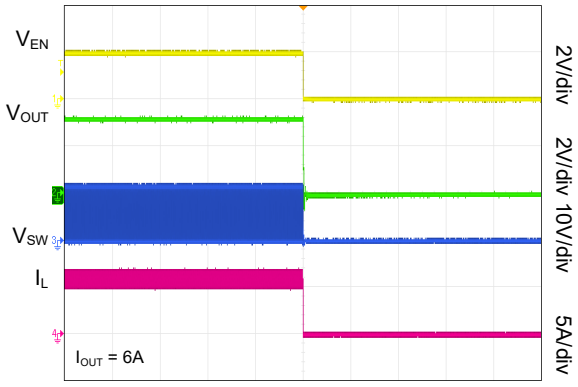
Time (5ms/div)

VIN Shutdown



Time (10ms/div)

EN Shutdown

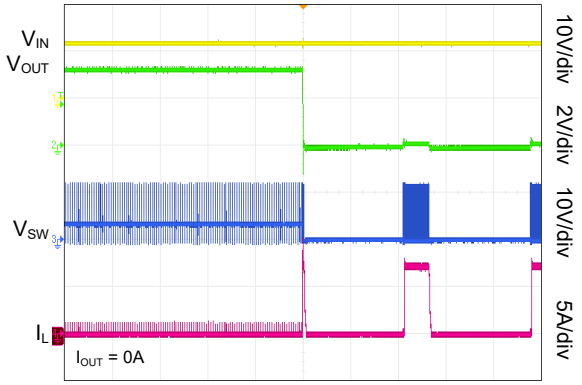


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

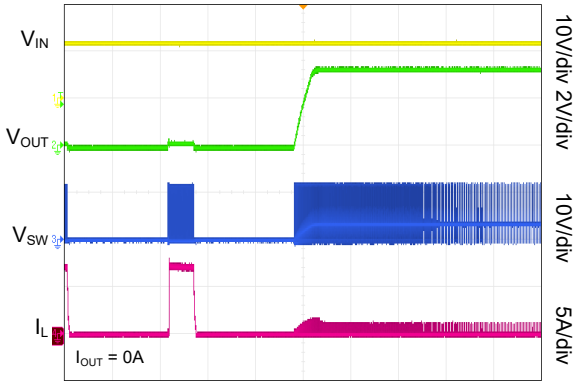
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 3.3μH and C_{OUT} = 22μF × 2, unless otherwise noted.

Short-Circuit Entry (SGM61162A)



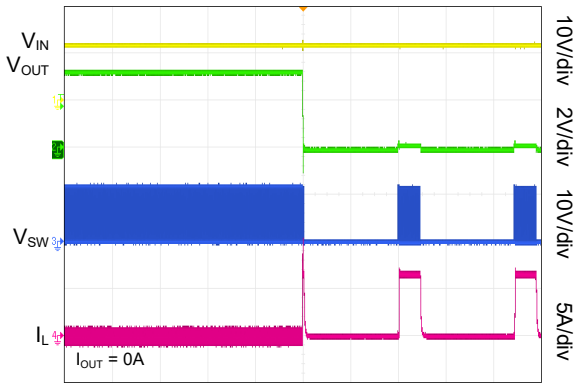
Time (5ms/div)

Short-Circuit Recovery (SGM61162A)



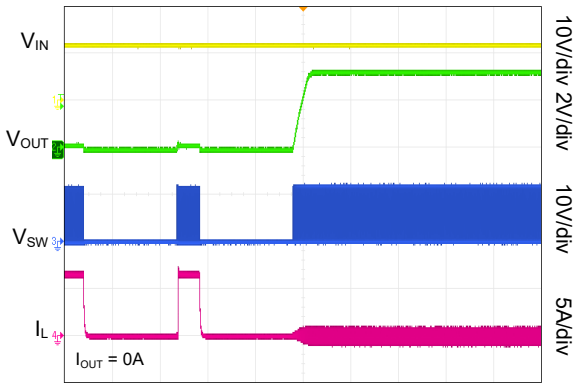
Time (5ms/div)

Short-Circuit Entry (SGM61162B)



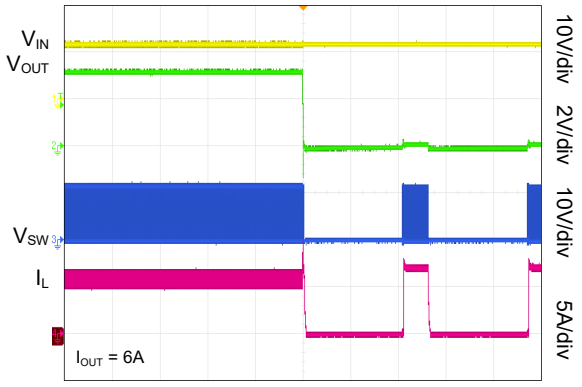
Time (5ms/div)

Short-Circuit Recovery (SGM61162B)



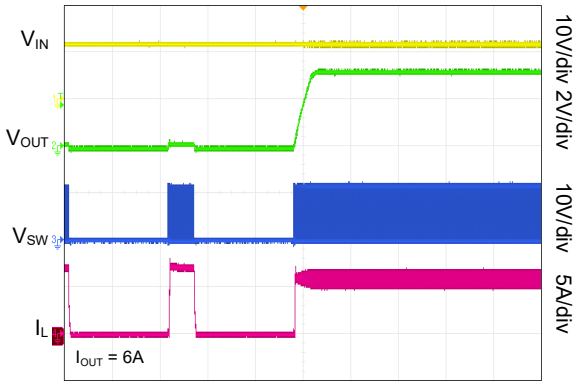
Time (5ms/div)

Short-Circuit Entry



Time (5ms/div)

Short-Circuit Recovery



Time (5ms/div)

FUNCTIONAL BLOCK DIAGRAM

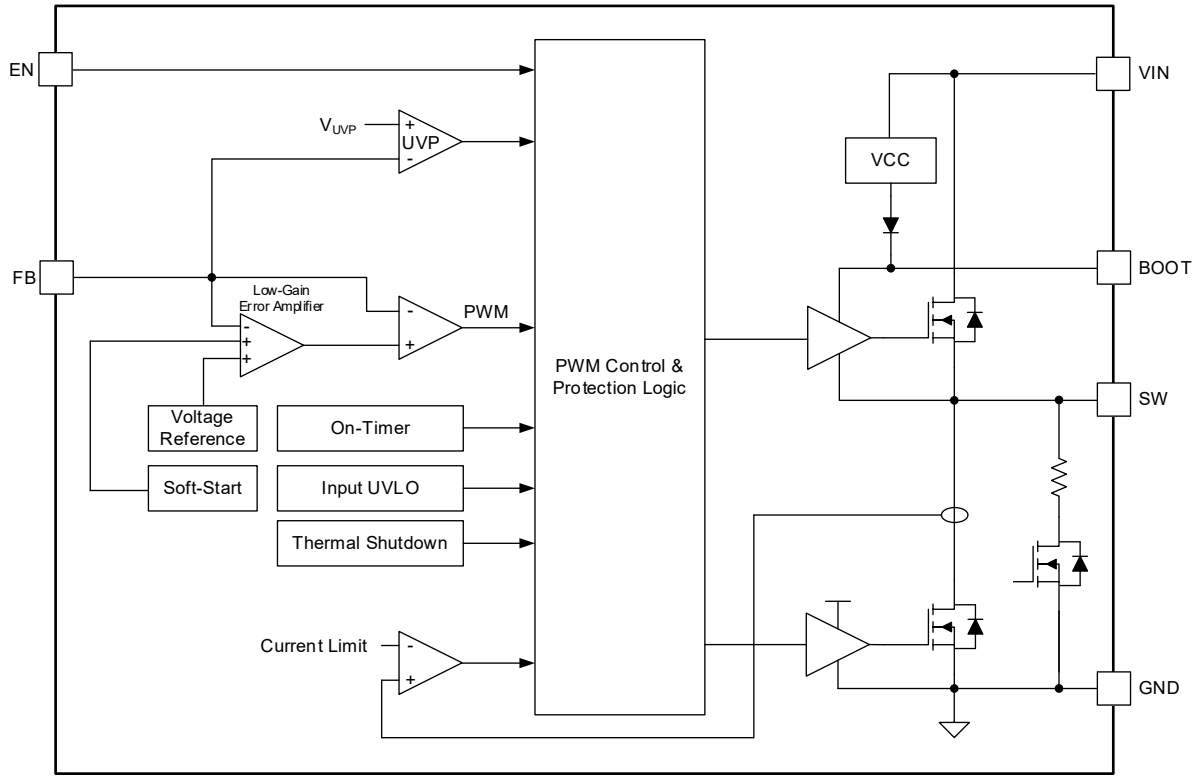


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61162 is a 18V, 6A synchronous Buck converter with over-current, short-circuit and thermal shutdown protection with auto recovery. Figure 2 shows the simplified block diagram of the SGM61162. The two integrated MOSFET switches of the power stage (32mΩ high-side and 20mΩ low-side) can provide up to 6A of continuous current with high efficiency.

The device is powered up when V_{IN} exceeds the UVLO threshold (4.15V TYP). At light load condition, the SGM61162A enters in pulse skip mode (PSM) to improve efficiency, while the SGM61162B works in forced pulse width modulation (FPWM) mode to achieve low output ripple and good regulation. At no load and with no switching, the typical operating current of SGM61162A is 170μA (TYP) and when the device is disabled by EN pin, it is only 2.8μA (TYP). The internal ripple injection minimizes the BOM cost and simplifies the design. The inrush current is also limited by an internal 2ms soft-start ramp.

DETAILED DESCRIPTION (continued)

Adaptive Constant On-Time Control

In conventional voltage mode control (VMC) or current mode control (CMC) converters, a fixed frequency clock timing signal generates a saw-tooth ramp that is compared with the compensation network output to adjust the PWM duty cycle (on-time) as control variable and regulate the output voltage and/or current feedback(s) to govern the control variable and keep the output regulated with fast reaction to load or V_{IN} variations. The existence of the compensator in VMC or CMC converter inherently introduces some delay in the loop response.

Unlike VMC or CMC, the adaptive constant on-time (ACOT) control is a hysteretic mode control without clock signal. Each switching cycle is started with a relative constant on-time pulse when an internal comparator senses that the output voltage drops below the desired output voltage. Output voltage is sensed by the feedback (FB) pin through an output resistor divider and is compared to the internal reference voltage (V_{REF}) with a low gain error amplifier. The amplifier output is sent to a comparator and when the feedback voltage (V_{FB}) falls below amplifier output, the comparator triggers the on-time control logic that turns on the high-side switch. ACOT control is able to dynamically adjust the on-time duration based on the input voltage and output voltage so that it can achieve relative constant frequency during steady state operation, which minimizes the EMI interference at some sensitive bands of certain frequencies in the system. An internal ramp is added to reference voltage to simulate output ripple, so it supports low ESR output capacitors applications.

Enable

The voltage on the EN pin provides the precision enable and disable of SGM61162. The device will be enabled if the EN pin voltage exceeds the enable threshold of 1.2V and V_{IN} exceeds its UVLO rising threshold. The device will be disabled if the EN voltage is externally pulled low or the V_{IN} pin voltage falls below its UVLO falling threshold. The EN pin cannot be left floating and can be connected to V_{IN} to enable the device.

An external input UVLO adjustment circuit is recommended in Figure 3. The EN input can be driven by an external logic signal to facilitate system sequencing and protection. If V_{EN} < 1V (TYP), the device will shut down. Only if V_{EN} > 1.2V (TYP), the device will start operation. It is crucial to note that the voltage supplied to the EN pin should never exceed V_{IN} + 0.3V.

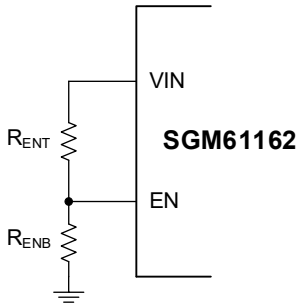


Figure 3. System UVLO by Enable Divider

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations.

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 1 and Figure 1 to calculate the output voltage. Lower divider resistor values increase loss and reduce light-load efficiency. Consider larger resistors to improve efficiency at light-load, and start with 100kΩ for the top resistor (R_{FBT}). Note that if R_{FBT} is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{FB} \times \left[\frac{R_{FBT}}{R_{FBB}} + 1 \right] \quad (1)$$

DETAILED DESCRIPTION (continued)

Internal Voltage Reference and Soft-Start

The SGM61162 device has an internal 0.604V reference (V_{REF}) to program the output at the desired level. When the converter starts, an internal ramp voltage begins to rise from near 0V to slightly above 0.604V with a ramp time of 2ms. The lower of V_{REF} and this ramp is used as reference for the error amplifier. Therefore, the ramp provides a soft-start for the output during startup. The soft-start is needed to avoid high inrush current caused by rapid increase of output voltage across output capacitors and the load.

Operation with Pulse Skip Mode (SGM61162A)

When SGM61162A operates in discontinuous conduction mode (DCM) with light load, it goes into the pulse skip mode in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load.

The details are explained in Figure 4 that shows the timings of the ACOT control in DCM. Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero, both high-side and low-side MOSFETs are turned off (if $V_{FB} > V_{REF\_EA}$). They will not turn on again until the V_{FB} falls below V_{REF} and triggers a new on-time pulse. During this off-time period, all non-essential circuits are shut down to minimize losses and the load is supplied by the output capacitor stored energy. The control circuitry wakes up when the new on-pulse is triggered.

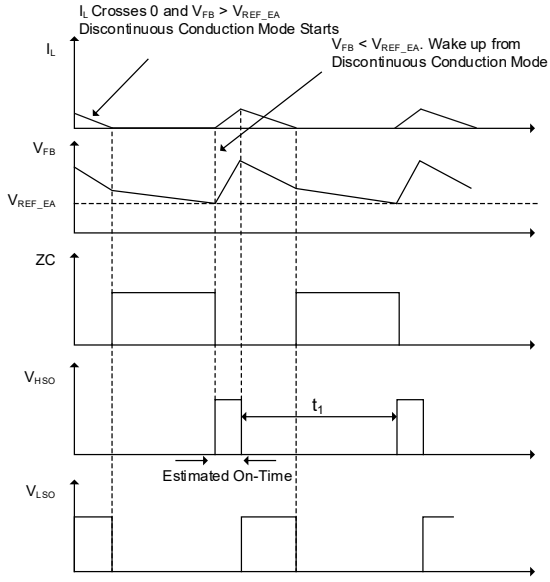


Figure 4. Pulse Skip Mode (DCM)

Light-Load Operation with Continuous Current Mode (SGM61162B)

SGM61162B is locked in forced pulse width modulation mode from full load to no load. Negative inductor currents are allowed at light load to keep continuous inductor current operation. It is a tradeoff that sacrifices light-load efficiency for keeping switching frequency relatively fixed, lower output ripple, and better output regulation. To avoid fatal negative current in the LS switch, this current is limited at -3.5A (TYP).

Over-Current and Short-Circuit Protection

The SGM61162 supports overload mode. When the output current continues overload while the system power-up, the SGM61162 exports the maximize power and limits the maximum valley current of the low-side MOSFET switch. The device keeps in cycle-by-cycle limit to obtain the system power request. The SGM61162 does not shut down until the device heats and then goes to thermal shutdown. As the load increases continuously, the output voltage decreases. If SS is ready and the FB voltage drops to 33% of V_{REF}, hiccup current-protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 10ms typically before the SGM61162 tries to start again. If over-current or a short-circuit fault condition still exists, the hiccup mode will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating.

Output Discharge Control

When EN is low, the SGM61162 utilizes an internal MOSFET connected between the SW pin and the GND pin to discharge the output capacitor stored energy, while ensuring that both the high-side and low-side MOSFETs remain in the OFF state. The typical discharge resistance is 60Ω.

Thermal Shutdown

If the junction temperature exceeds +155℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

APPLICATION INFORMATION

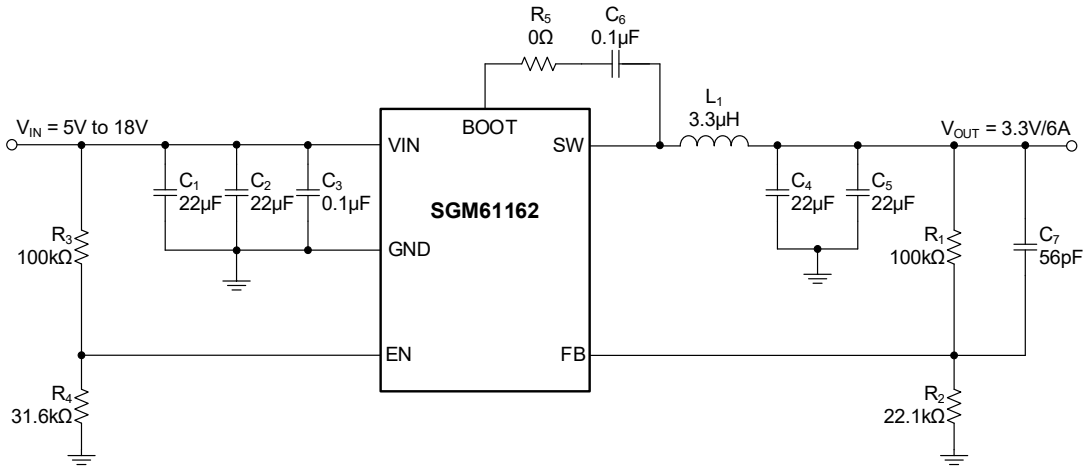


Figure 5. A Reference Design for 3.3V/6A Application

The design method and component selection for the SGM61162 Buck converter is explained in this section. Schematic of a basic design is shown in Figure 5. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L_1 and C_{OUT}) along with C_{FF} and divider resistor values are provided in Table 1 to simplify component selection.

Table 1. Recommended Component Values

V_{OUT} (V)	L_1 (μH)	C_4 + C_5 (μF)	R_1 (kΩ)	R_2 (kΩ)	C_7 (pF)
0.9	1.2	44	49.9	100	56
3.3	3.3	44	100	22.1	56
5	4.7	44	147	20	56

Design Requirements

A typical application circuit for the SGM61162 as a Buck converter is shown in Figure 5. It is used for converting a 5V to 18V supply voltage to a lower voltage level supply voltage (3.3V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 5V to 18V
Input Ripple Voltage	360mV, 3% of V_{IN_TYP}
Output Voltage	3.3V
Output Voltage Ripple	66mV, 2% of V_{OUT}
Output Current Rating	6A
Transient Response, 3A to 6A Load Step	165mV, 5% of V_{OUT}
Operation Frequency	420kHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61162. In some applications, additional bulk capacitance may also be required for the V_{IN} input, for example, when the SGM61162 is more than 5cm away from the input source. The V_{IN} capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 2 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 6A, yields an RMS input ripple current of 3A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (2)$$

APPLICATION INFORMATION (continued)

For this design, a ceramic capacitor with at least 25V voltage rating is required to support the maximum input voltage. So, two 22μF/25V capacitors are selected for V_{IN} to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 3. In this example, the total effective capacitance of the 2 × 22μF/25V capacitor is around 10μF at 12V input, and the input voltage ripple is 285mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (3)$$

It is recommended placing an additional small size 0.1μF ceramic capacitor right beside V_{IN} and GND pins for high frequency filtering.

Inductor Selection

Equation 4 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 30% ripple is selected (K_{IND} = 0.3).

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (4)$$

In this example, the calculated inductance will be 3.57μH with K_{IND} = 0.3, for compact application scenario a 3.3μH is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 5, 6 and 7 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (5)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (6)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Additionally, the capacitors store energy to assist in maintaining output voltage regulation during load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage, temperature (℃) and its parasitic parameters (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (8)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant. The type of output capacitors will determine which terms of Equation 8 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the capacitive term.

To reduce the voltage ripple, either inductance or the total capacitance is increased. For electrolytic output capacitors, the value of capacitance is relatively high, and compared with ESR and ESL terms, the third term in Equation 8 can be ignored.

Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors.

APPLICATION INFORMATION (continued)

The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended using quality capacitors with the ESR or the total impedance clearly documented in the datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The design of the output capacitor typically satisfies the typical ±1% ripple requirement. The appropriate output capacitor value can be selected through calculations based on the capacitor ripple and ESR ripple. However, in scenarios involving low voltage and high current, it is crucial to consider the overshoot and undershoot of the output voltage during load transient. Additionally, with the same output capacitor, the ACOT control response is faster than voltage mode control or current mode control. Therefore, the design of the output capacitor must always take into account the load transient response. Equation 9 and Equation 10 calculate the minimum capacitor required to keep the output voltage overshoot or undershoot to a desired value.

$$C_{OUT} > \frac{L \times I_{STEP}^2}{2 \times V_{UNDER} \times D \times (V_{IN} - V_{OUT})} \quad (9)$$

$$C_{OUT} > \frac{L \times I_{STEP}^2}{2 \times V_{OVER} \times V_{OUT}} \quad (10)$$

where

V_{OVER} is the output overshoot during load transient from full load to half load.

V_{UNDER} is the output undershoot during load transient from half load to full load.

I_{STEP} is the magnitude of the load step change.

In this case according to Table 1, 2 × 22μF/10V X7R ceramic capacitors can meet the above conditions.

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X5R or X7R) with 10V or higher voltage rating for the bootstrap capacitor (C_6).

VIN UVLO Setting

The input UVLO can be programmed by using an external voltage divider on the EN pin of the SGM61162. In this design, R_3 is connected between VIN pin and EN pin, and R_4 is connected between EN pin and GND (see Figure 5). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above V_{UV_H}. When the regulator is working, it will not stop switching (disabled) until the input falls below V_{UV_L}. The enable rising threshold voltage V_{EN_H} is 1.2V (TYP) and enable hysteresis voltage V_{EN_HYS} is 0.2V (TYP). Given V_{UV_H} as 5.0V, select R_3 to be 100kΩ to minimize input current from the supply, then R_4 and V_{UV_L} can be calculated by following equations.

$$V_{UV\_H} = V_{EN\_H} \times \frac{R_3 + R_4}{R_4} \quad (11)$$

$$V_{UV\_L} = (V_{EN\_H} - V_{EN\_HYS}) \times \frac{R_3 + R_4}{R_4} \quad (12)$$

By Equation 11, R_4 is calculated to be 31.58kΩ, and a standard value of 31.6kΩ is selected. Based on the value of R_3 and R_4, V_{UV_L} can be calculated to be 4.16V according to Equation 12.

Output Voltage Setting

Use an external resistor divider (R_1 and R_2) to set the output voltage using Equation 13:

$$R_2 = \frac{R_1 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (13)$$

where V_{REF} = 0.604V is the internal reference. For example, by choosing R_1 = 100kΩ, the R_2 value for 3.3V output will be calculated as 22.4kΩ, so the nearest resistance of 22.1kΩ is selected.

Feed-Forward Capacitor Selection

The SGM61162 contains an internal compensation circuit, an internal ramp is added to reference voltage to simulate output ripple. For ultra-low output capacitance ESR (ceramic capacitor) applications, it is recommended adding a 56pF feed-forward capacitor (C_7) to provide a low-impedance path for output voltage ripple and ensure minimal phase shift of the voltage ripple at the feedback node while maintaining acceptable transient response.

APPLICATION INFORMATION (continued)

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R, X7R or better dielectric) placed as close as possible to VIN pin.
- Use short, wide and direct traces for high-current connections (VIN, SW and GND).
- Keep the BOOT-SW voltage path as short as possible.
- Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

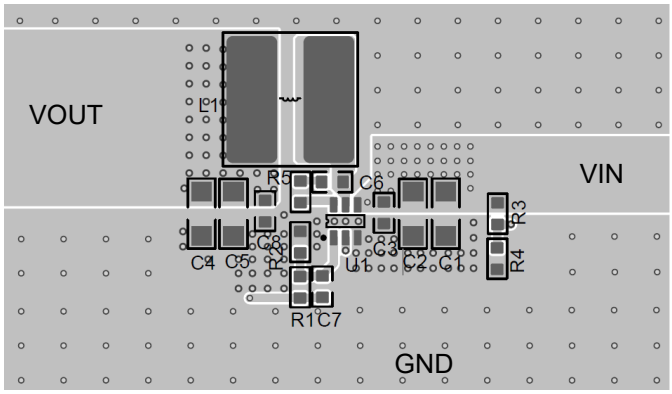


Figure 6. PCB Top Layer

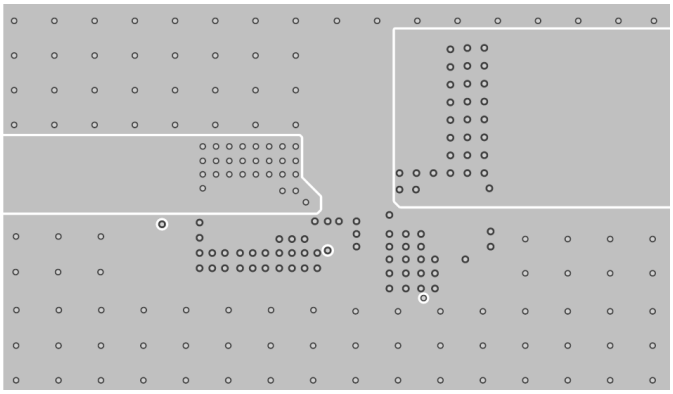


Figure 7. PCB Bottom Layer

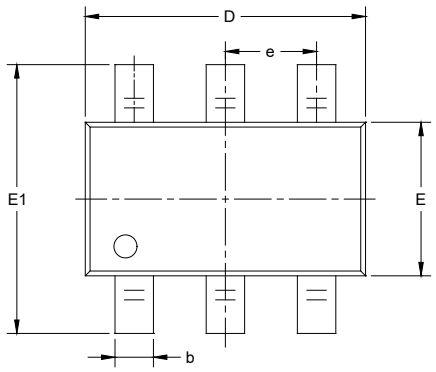
REVISION HISTORY

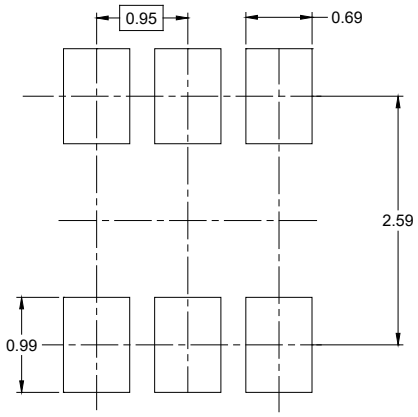
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2025)	Page
Changed from product preview to production data	All

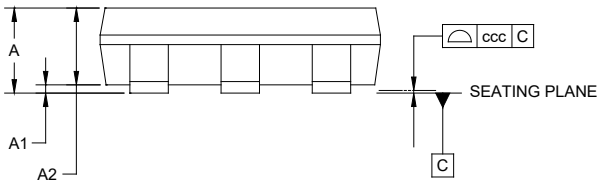
PACKAGE OUTLINE DIMENSIONS

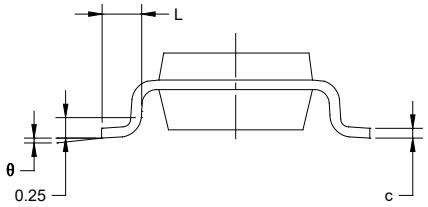
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



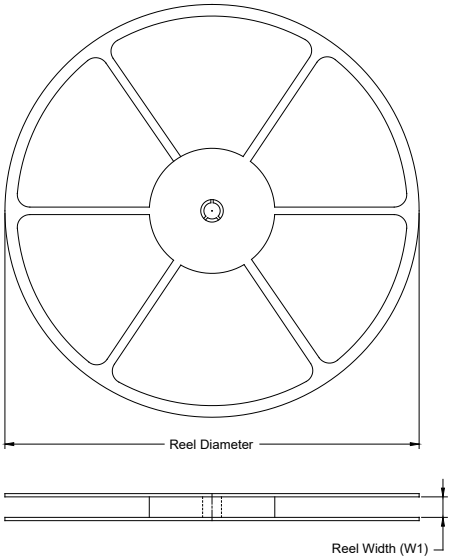


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.300	-	0.500
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

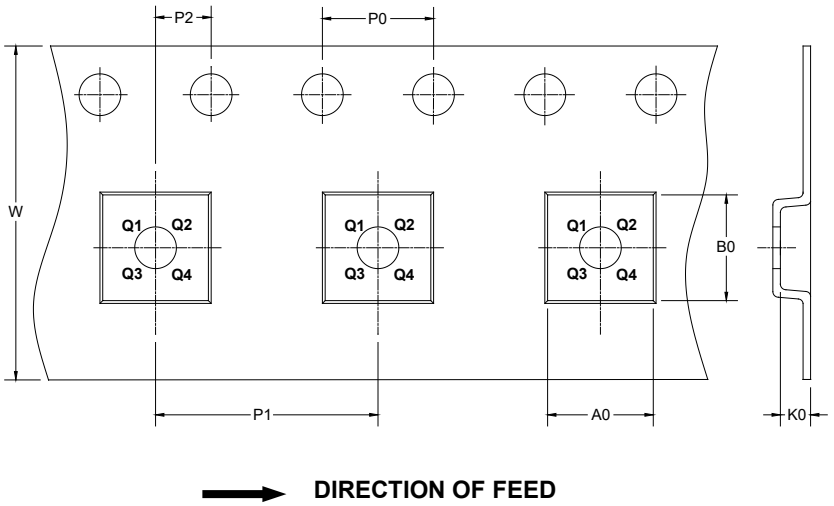
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

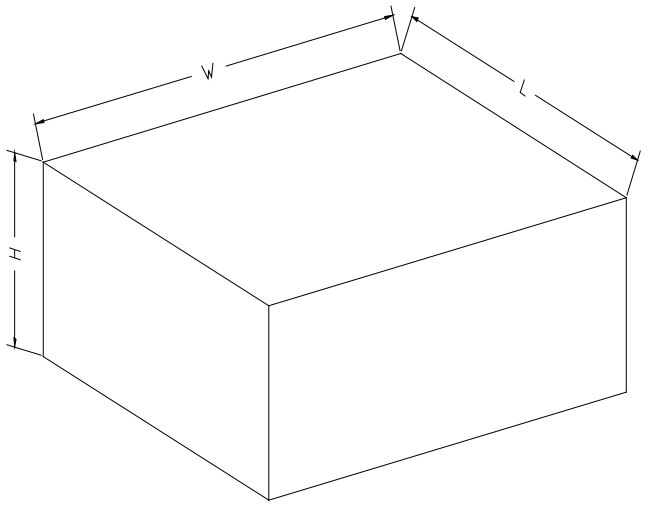
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002