SGM70430
Low Dropout Linear Voltage Regulator with Watchdog and Reset

GENERAL DESCRIPTION

The SGM70430 is a low dropout linear regulator with 3.3V and 5V fixed output and low quiescent current. It can support up to 300mA output current (500mA peak). This device adopts output voltage supervision, watchdog timer, user-programmable delay for both reset and watchdog function, and enable function. It also has over-temperature protection and over-current protection. Additionally, it can withstand transient voltages with maximum magnitude within 45V.

The SGM70430 maintains rapid response and excellent stability with only a 1μF ceramic capacitor at the output, even under a very low VCC voltage (down to 3V).

The SGM70430 is available in a Green SSOP-14 (Exposed Pad) package.

FEATURES

- **Up to 300mA Output Current (500mA Peak)**
- **Input Voltage Range from 3V to 28V**
- **Output Voltage with ±2% Accuracy**
- **Fixed Output:**
  - **SGM70430-3.3: 3.3V**
  - **SGM70430-5.0: 5.0V**
- **High Accuracy Output Voltage Tolerance**
- **Suitable for Micropower Control Applications: Enable, Watchdog and nRESET**
- **Stable with 1μF Ceramic Output Capacitor**
- **Ultra Low Current Consumption: 23μA (TYP)**
- **Very Low Dropout Voltage: 110mV (TYP) at 100mA**
- **Output Voltage Supervision by Reset Circuit:**
  - **Programmable Under-Voltage Reset Threshold: 2.5V (MIN)**
  - **Programmable Delay Time**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SSOP-14 (Exposed Pad) Package**

APPLICATIONS

General ECUs
Telematics Systems
ADAS Cameras and Radar Systems
Navigation Systems
Body Control Modules

TYPICAL APPLICATION

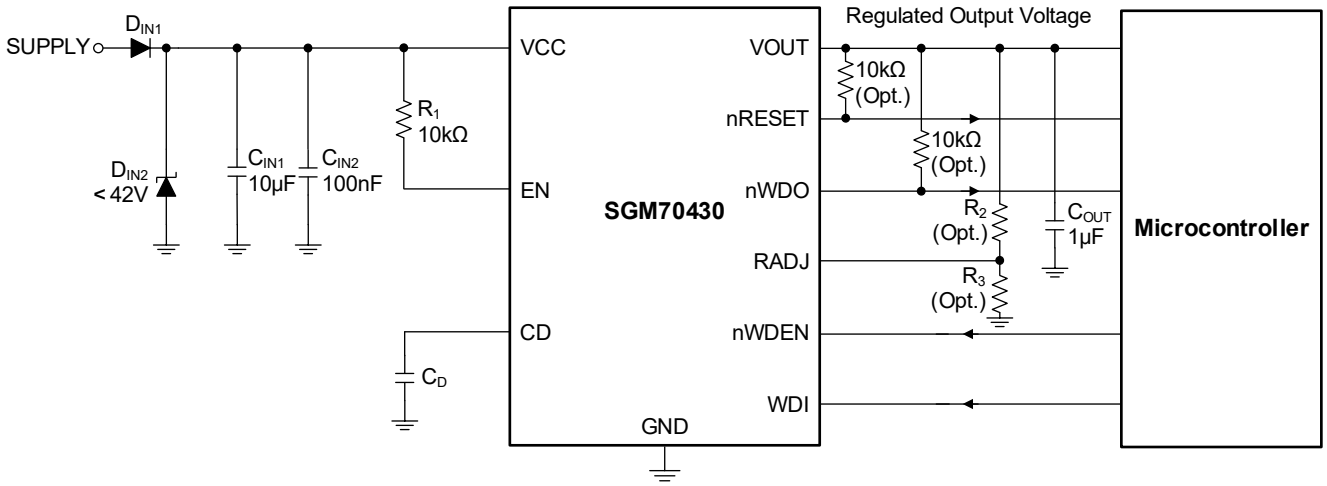


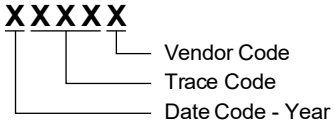
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM70430-3.3	SSOP-14 (Exposed Pad)	-40℃ to +125℃	SGM70430-3.3XPSS14G/TR	XXXXX 2T6	Tape and Reel, 3000
SGM70430-5.0	SSOP-14 (Exposed Pad)	-40℃ to +125℃	SGM70430-5.0XPSS14G/TR	XXXXX 2T7	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Rating

Input Voltage, V_{CC} ..... -0.3V to 45V
Enable Voltage, V_{EN} ..... -0.3V to 45V
Output Voltage, V_{OUT} ..... -0.3V to 7V
nRESET Output Voltage, V_{RESET} ..... -0.3V to 7V
CD Voltage, V_{CD} ..... -0.3V to 7V
Reset Threshold Voltage, V_{RADJ} ..... -0.3V to 7V
Watchdog Input, V_{WDI} ..... -0.3V to 7V
Watchdog Output, V_{nWDO} ..... -0.3V to 7V
Watchdog Enable Input, V_{nWDEN} ..... -0.3V to 7V
Package Thermal Resistance
SSOP-14 (Exposed Pad), θ_{JA} ..... 41.9℃/W
SSOP-14 (Exposed Pad), θ_{JB} ..... 21.8℃/W
SSOP-14 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 53.3℃/W
SSOP-14 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 12.4℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{CC} .....V_{OUT_NOM} + V_{DR} to 28V
Extended Input Voltage Range, V_{CC_EXT} .....3V to 28V (1)
Enable Voltage Range, V_{EN} .....0V to 28V
Output Capacitance for Stable Operation, C_{OUT} .....
.....1μF to 10μF (2) (3)
ESR of Output Capacitor, ESR_{COUT} ..... 20Ω (MAX) (3) (4)
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

NOTES:

1. When V_{CC_EXT} is smaller than V_{OUT_NOM}, V_{OUT} follows the V_{CC} voltage, see Voltage Regulator.
2. Capacitance range smaller than 30%.
3. Guaranteed by design.
4. Relevant ESR value at f = 10kHz.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

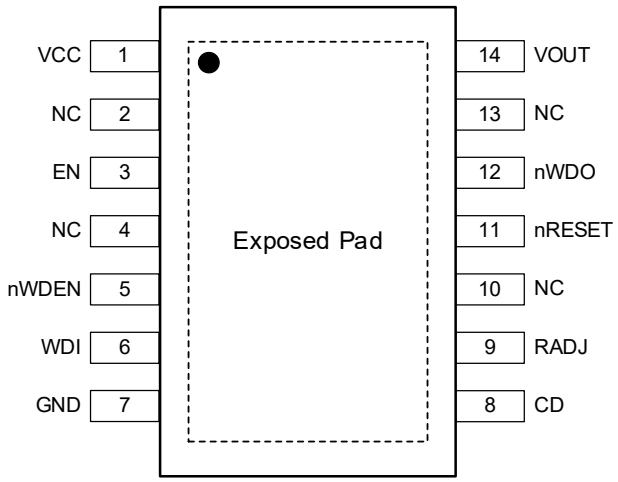
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SSOP-14 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VCC	Supply Voltage. A ceramic capacitor is advised to be placed at this pin.
2, 4, 10, 13	NC	Not Connected. Leave this pin open or connect it to GND.
3	EN	Enable Input. A built-in resistor is placed between the EN pin and GND.
5	nWDEN	Watchdog Enable Input. A built-in resistor is placed between the nWDEN pin and GND.
6	WDI	Watchdog Input. A positive edge at the WDI pin triggers the watchdog and clears the watchdog timer. A built-in resistor is placed between the WDI pin and GND.
7	GND	Ground.
8	CD	Delay Input. A capacitor at this pin is determined to set both the reset timing and the watchdog timing. Once this pin is unconnected, please pull down the nWDEN pin and disable the watchdog function. Watchdog trigger time can be derived from the delay capacitor by: $t_{WDI\_TR} = C_D/10nF \times t_{WDI\_TR\_10nF}$.
9	RADJ	Reset Threshold Adjustment. To utilize the default reset threshold, connect this pin to GND. For a customized reset threshold, tie this pin to an external resistor ladder. If the reset function is deselected, this pin should be connected directly to the VOUT pin.
11	nRESET	Reset Output. It is weakly pulled up to VOUT.
12	nWDO	Watchdog Output. It is weakly pulled up to VOUT.
14	VOUT	Regulator Output. A ceramic capacitor is advised to be placed as close as possible to this pin.
Exposed Pad	Exposed Pad	Exposed Pad. Connect it to GND.

ELECTRICAL CHARACTERISTICS

Voltage Regulator Electrical Characteristics

(V_{CC} = 13.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Accuracy	V_{OUT}	50μA ≤ I_{OUT} ≤ 300mA, V_{OUT_NOM} + V_{DR} ≤ V_{CC} ≤ 28V	SGM70430-3.3	3.23	3.3	3.37	V
			SGM70430-5.0	4.9	5.0	5.1	
Output Voltage Startup Slew Rate	dV_{OUT}/dt	$d\Delta V_{CC}/\Delta t$ = 50V/ms, C_{OUT} = 1μF, 0.1 × V_{OUT_NOM} ≤ V_{OUT} ≤ 0.9 × V_{OUT_NOM}		7		70	V/ms
Load Regulation Steady State	dV_{OUT_LOAD}	I_{OUT} = 0.05mA to 300mA, V_{CC} = 6.5V		-16		16	mV
Line Regulation Steady State	dV_{OUT_LINE}	V_{CC} = 8V to 32V, I_{OUT} = 5mA		-16		16	mV
Power Supply Ripple Rejection	PSRR	f_{RIPPLE} = 100Hz, V_{RIPPLE} = 0.5V_{PP}, I_{OUT} = 10mA (1)			70		dB
Dropout Voltage V_{DR} = V_{CC} - V_{OUT}	V_{DR}	I_{OUT} = 100mA	SGM70430-3.3		110	725	mV
			SGM70430-5.0		110	300	
		I_{OUT} = 250mA	SGM70430-3.3		300	840	mV
			SGM70430-5.0		300	1110	
Output Current Limitation	I_{OUT_MAX}	V_{OUT} ≤ V_{OUT_NOM} - 1V		301	580	800	mA
Over-Temperature Shutdown Threshold	T_{J_SD}	T_J increasing (1)			175		℃
Over-Temperature Shutdown Threshold Hysteresis (1)	T_{J_SDH}				20		℃

Current Consumption Electrical Characteristics

(V_{CC} = 13.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption I_q = I_{CC}	I_{q_OFF}	V_{EN} = 0V, T_A ≤ +125℃			2	μA
		V_{EN} = 0.4V, T_A ≤ +125℃			2	
Current Consumption I_q = I_{CC} - I_{OUT}	I_q	I_{OUT} = 50μA, T_A = +25℃, watchdog disabled		23	34	μA
		I_{OUT} = 50μA, T_A ≤ +125℃, watchdog disabled		40	55	
		I_{OUT} = 50μA, T_A = +25℃, watchdog enabled		23	34	
		I_{OUT} = 50μA, T_A ≤ +125℃, watchdog enabled (1)		40	55	

Enable Electrical Characteristics

(V_{CC} = 13.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable High Input Voltage	V_{EN_H}	V_{OUT} settled	2			V
Enable Low Input Voltage	V_{EN_L}	V_{OUT} ≤ 0.1V			0.8	V
Enable Threshold Hysteresis (1)	V_{EN_HY}		90			mV
Enable High Input Current	I_{EN_H}	V_{EN} = 3.3V			1	μA
		V_{EN} = 18V			6	
Enable Internal Pull-Down Resistor	R_{EN}		3	10	20	MΩ

NOTE:

1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

Reset Electrical Characteristics

(V_{CC} = 13.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Under-Voltage Reset Comparator Default Values (Pin RADJ = GND)							
Output Under-Voltage Reset Lower Switching Threshold	V_{RT_LOW}	V_{EN} ≥ 2.0V, V_{OUT} decreasing, RADJ connected to GND, V_{RT_LOW} ≤ V_{CC} ≤ 28V	SGM70430-3.3	2.97	3.03	3.10	V
			SGM70430-5.0	4.50	4.60	4.70	
Output Under-Voltage Reset Upper Switching Threshold	V_{RT_HIGH}	V_{EN} ≥ 2.0V, V_{OUT} increasing, RADJ connected to GND, V_{RT_HIGH} ≤ V_{CC} ≤ 28V	SGM70430-3.3	3.03	3.10	3.17	V
			SGM70430-5.0	4.60	4.70	4.80	
Output Under-Voltage Reset Switching Hysteresis	V_{RT_HY}	V_I within operating range, RADJ connected to GND, V_{EN} ≥ 2.0V	SGM70430-3.3	30	70	130	mV
			SGM70430-5.0	40	100	180	
Reset Threshold Adjustment							
Reset Adjust Switching Threshold	V_{RADJ_TH}			0.87	0.92	0.97	V
Reset Adjustment Range (1)	V_{RT_RANGE}	SGM70430-3.3		2.5		2.9	V
		SGM70430-5.0		2.5		4.4	
Reset Output nRESET							
Reset Output Low Voltage	V_{RESET_LOW}	1V ≤ V_{OUT} ≤ V_{RT}, R_{RESET_EXT} ≥ 6.2kΩ			0.03	0.4	V
Reset Output, External Pull-Up Resistor to VOUT	R_{RESET_EXT}	1V ≤ V_{OUT} ≤ V_{RT}, V_{RESET} ≤ 0.4V		6.2			kΩ
Reset Output, Internal Pull-Up Resistor	R_{RESET_INT}	Internally connected to VOUT		10	20	30	kΩ
Reset Delay Timing							
Upper Delay Switching Threshold	V_{DR_HIGH}				0.92		V
Lower Delay Switching Threshold	V_{DR_LOW}				0.59		V
Delay Capacitor Charge Current	I_{DELAY_CH}	V_{DELAY} = 1.2V			1.53		μA
Delay Capacitor Reset Discharge Current	I_{DR_DSCH}	V_{DELAY} = 1.2V			50		mA
Power-On Reset Delay Time	$t_{CD\_PWRON\_10nF}$	Calculated value, C_D = 10nF, C_D discharged to 0V (2)		4.5	6.5	8.5	ms
Internal Reset Reaction Time	t_{RR_INT}	C_D = 0nF, V_{OUT} = 4V, V_{nWDEN_HIGH} ≤ V_{nWDEN}			10		μs
Delay Capacitor Discharge Time	$t_{RR\_D\_10nF}$	C_D = 10nF (2)			0.2		μs
Total Reset Reaction Time	$t_{RR\_TOTAL\_10nF}$	Calculated value: $t_{RR\_D\_10nF}$ + t_{RR_INT}, C_D = 10nF			10		μs
Reset Blanking Time (3)	t_{RR_BLANK}				4		μs

NOTES:

1. If the reset switching threshold is modified, then the related parameters V_{RT_HIGH}, V_{RT_HY} are changed directly proportional.
2. For programming a different delay and reset reaction time.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)

Watchdog Electrical Characteristics

(V_{CC} = 13.5V, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Watchdog Enable, nWDEN						
Watchdog Enable Low Signal Valid	V_{nWDEN_LOW}				0.8	V
Watchdog Enable High Signal Valid	V_{nWDEN_HIGH}		2			V
Watchdog Enable High Level Input Current	I_{nWDEN_HIGH}	V_{nWDEN} = 3.3V			4	μA
WDI Blanking Time after Watchdog Enable High	$t_{blanking\_nWDEN}$	C_D = 10nF, $V_{nWDEN} \geq V_{nWDEN\_HIGH}$		1.4		ms
Watchdog Enable Internal Pull-down Resistor	R_{nWDEN}		0.4	1.3	2.5	MΩ
Watchdog Input, WDI						
Watchdog Input Low Signal Valid	V_{WDI_LOW}				0.8	V
Watchdog Input High Signal Valid	V_{WDI_HIGH}		2			V
Watchdog Input Low Signal Pulse Length (1)	t_{WDI_PL}	$V_{WDI} \leq V_{WDI\_LOW}$	1			μs
Watchdog Input High Signal Pulse Length	t_{WDI_PH}	$V_{WDI} \geq V_{WDI\_HIGH}$	1			μs
Watchdog Input High Level Input Current	I_{WDI_H}	V_{WDI} = 3.3V			4	μA
Watchdog Input Signal Slew Rate	$\Delta V_{WDI}/\Delta t$	$V_{WDI\_LOW} \leq V_{WDI} \leq V_{WDI\_HIGH}$	1			V/μs
Watchdog Input Internal Pull-down Resistor	R_{WDI}		0.4	1.3	2.5	MΩ
Watchdog Output, nWDO						
Watchdog Output Low Voltage	V_{nWDO_LOW}	$V_{OUT} \geq$ 2.5V, $R_{nWDO} \geq$ 6.2kΩ		0.03	0.4	V
Watchdog Output External Pull-up Resistor	R_{nWDO_EXT}	$V_{OUT} \geq$ 2.5V, $V_{nWDO} \leq$ 0.4V	6.2			kΩ
Watchdog Output Internal Pull-up Resistor	R_{nWDO_INT}		10	20	30	kΩ
Watchdog Timing						
Delay Capacitor Charge Current	I_{CD}	V_{CD} = 1.2V		1.53		μA
Delay Capacitor Deactivation Charge Current	$I_{DW\_CH\_DEACT}$	V_{CD} = 1.2V		1.53		μA
Delay Capacitor Watchdog Discharge Current	I_{DW_DISCH}	V_{CD} = 1.2V		0.5		μA
Upper Watchdog Timing Threshold	V_{DW_HIGH}			1.44		V
Lower Watchdog Timing Threshold	V_{DW_LOW}			0.89		V
Upper Delay Watchdog Deactivated Hold Voltage	V_{DW_CD}	$V_{nWDEN} \geq V_{nWDEN\_HIGH}$		1.54		V
Watchdog Trigger Time	$t_{WDI\_TR\_10nF}$	Calculated value, C_D = 10nF	7	11	15	ms
Watchdog Output Low Time	$t_{WD\_LO\_10nF}$	Calculated value, C_D = 10nF	2.5	3.5	5.5	ms
Watchdog Period	$t_{WD\_P\_10nF}$	Calculated value, $t_{WDI\_TR\_10nF} + t_{WD\_LO\_10nF}$, C_D = 10nF	9.5	14.5	20.5	ms

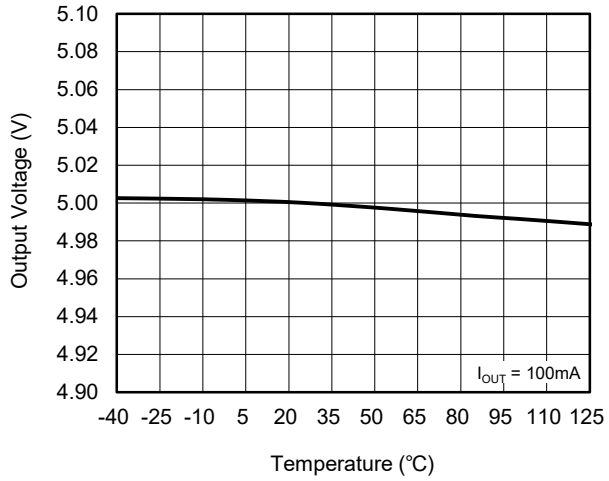
NOTE:

1. Guaranteed by design.

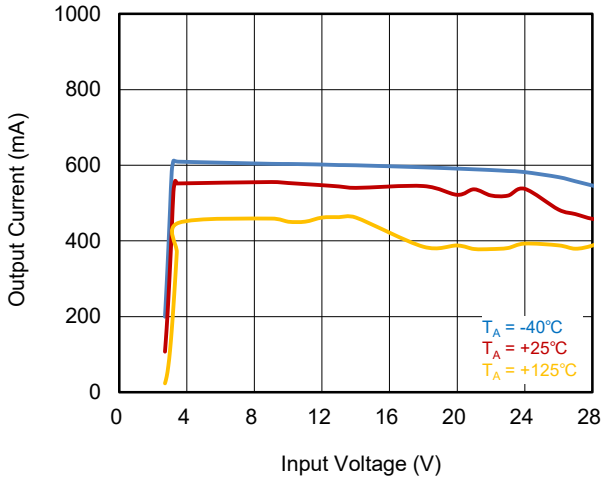
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

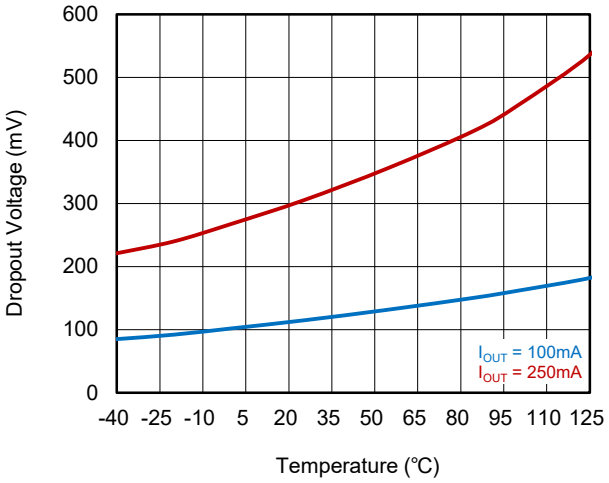
Output Voltage vs. Temperature



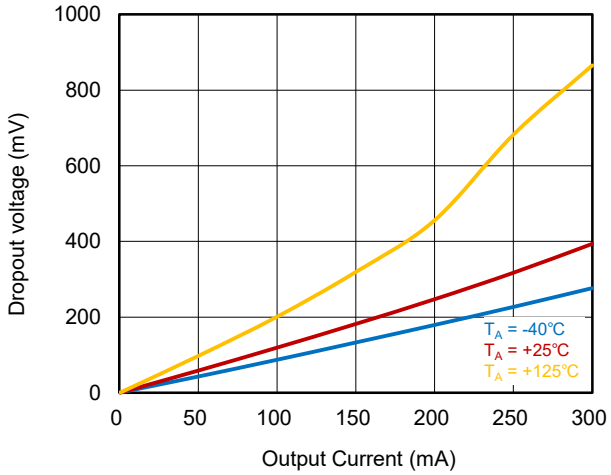
Output Current vs. Input Voltage



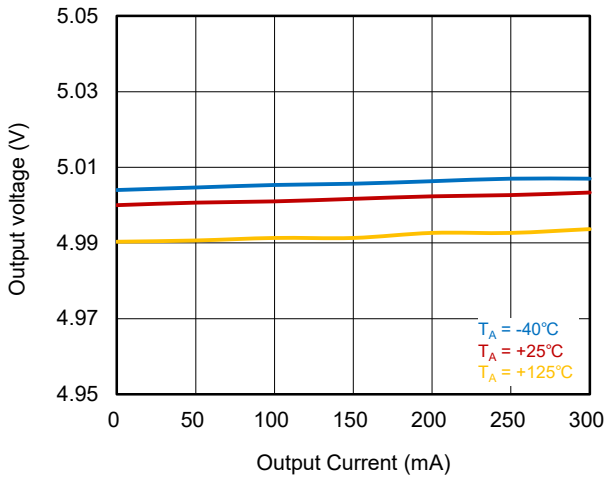
Dropout Voltage vs. Temperature



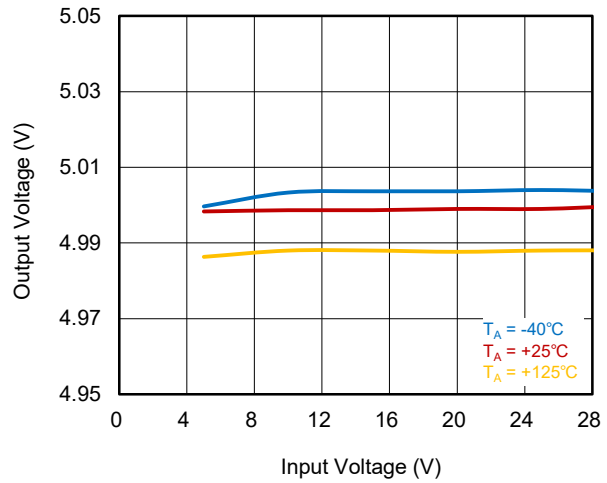
Dropout Voltage vs. Output Current



Output Voltage vs. Output Current



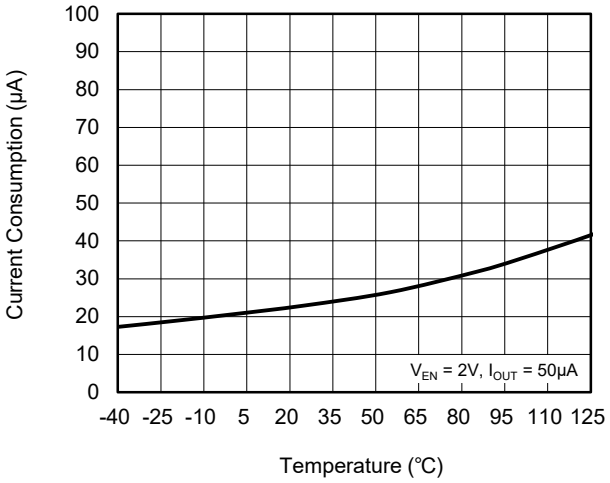
Output Voltage vs. Input Voltage



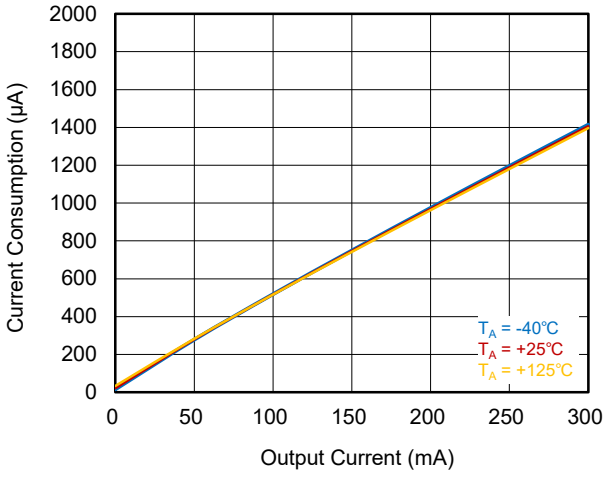
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

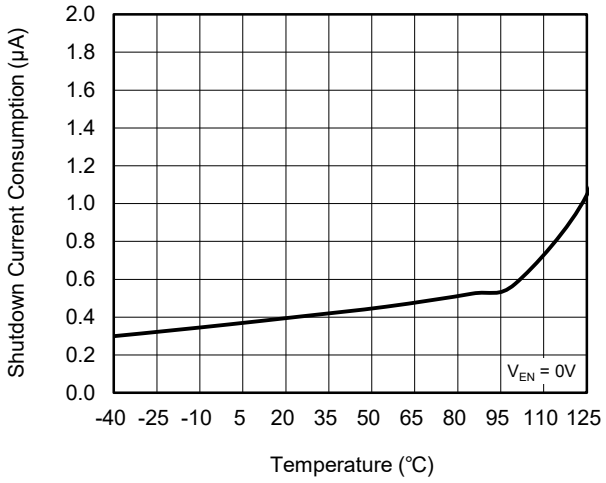
Current Consumption vs. Temperature



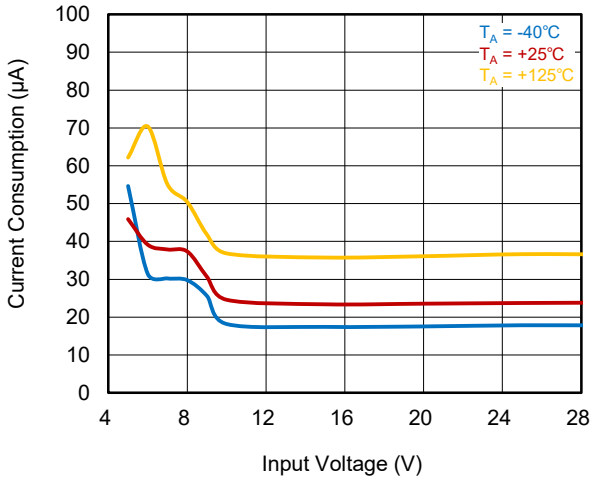
Current Consumption vs. Output Current



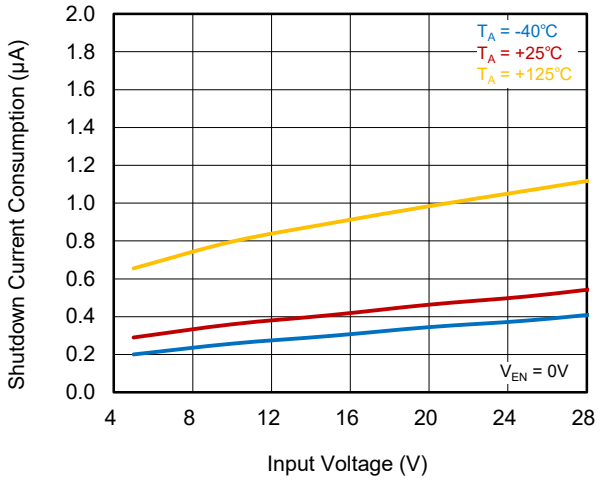
Shutdown Current Consumption vs. Temperature



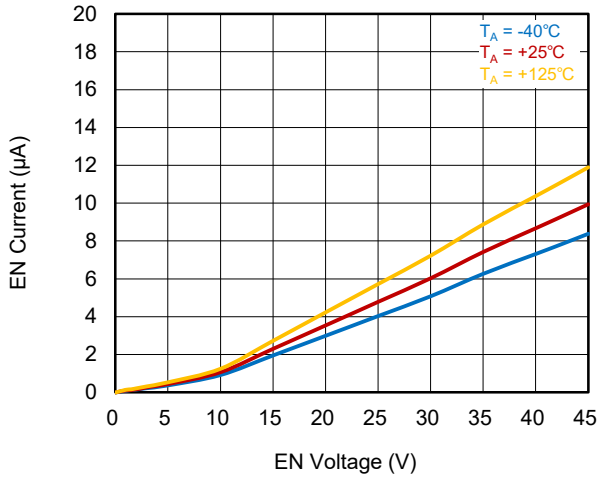
Current Consumption vs. Input Voltage



Shutdown Current Consumption vs. Input Voltage



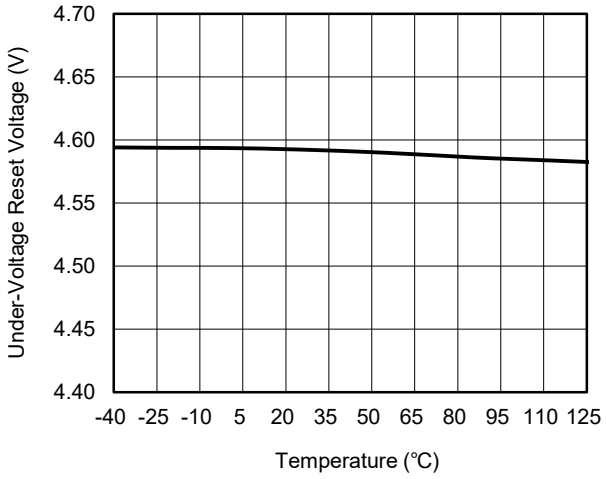
EN Current vs. EN Voltage



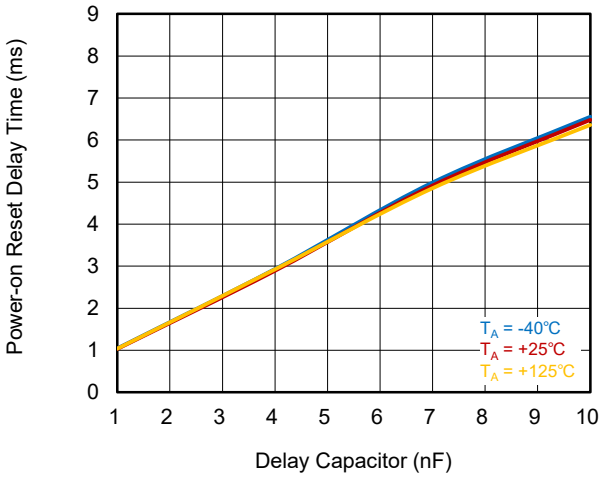
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

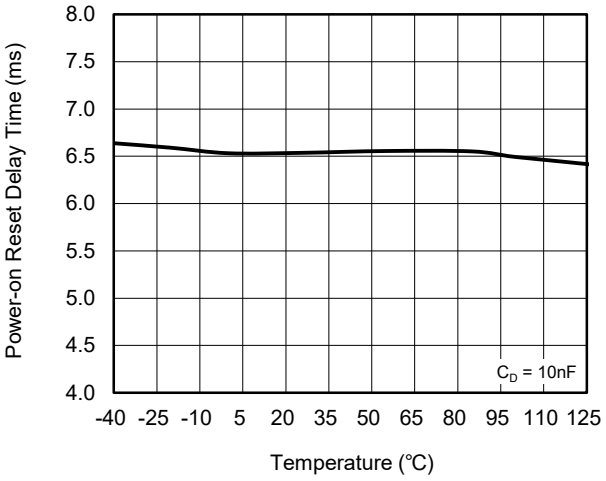
Under-Voltage Reset Voltage vs. Temperature



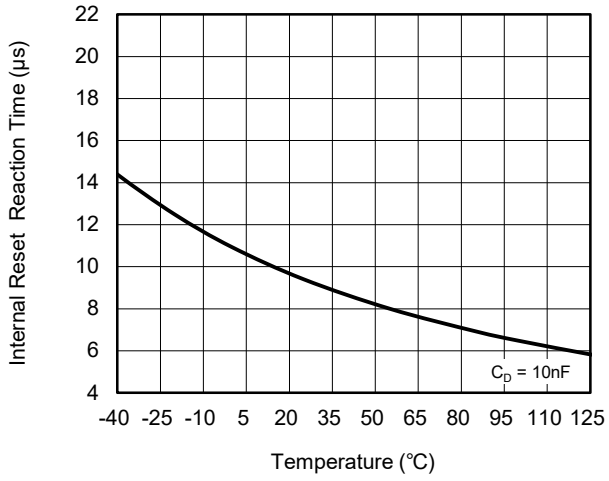
Power-on Reset Delay Time vs. Delay Capacitor



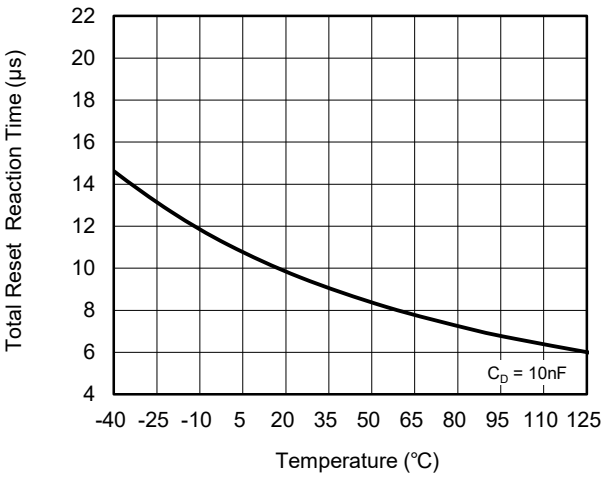
Power-on Reset Delay Time vs. Temperature



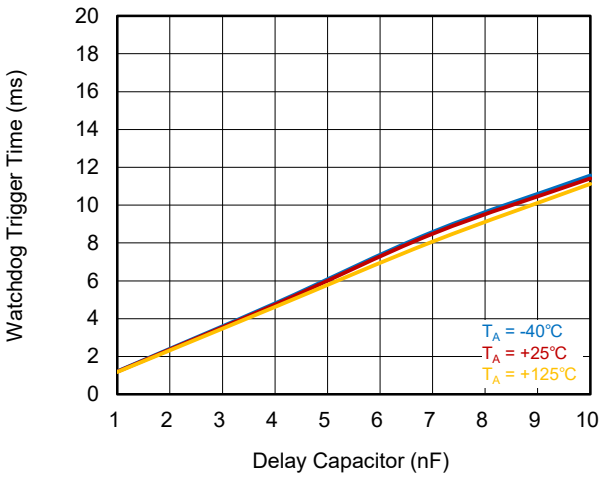
Internal Reset Reaction Time vs. Temperature



Total Reset Reaction Time vs. Temperature



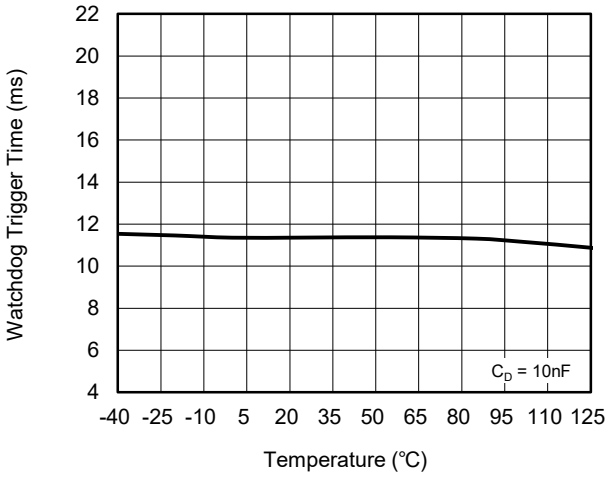
Watchdog Trigger Time vs. Delay Capacitor



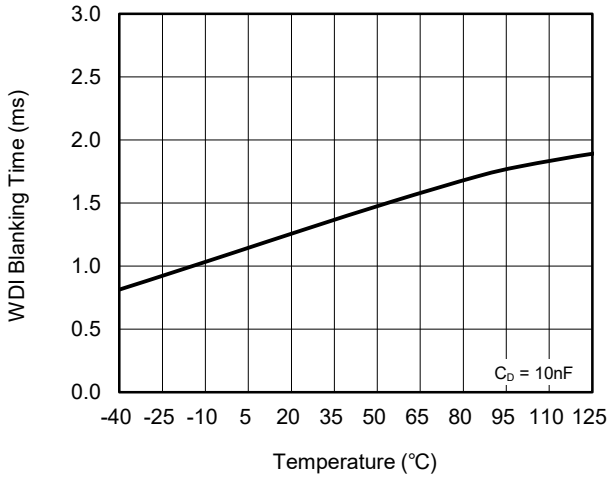
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

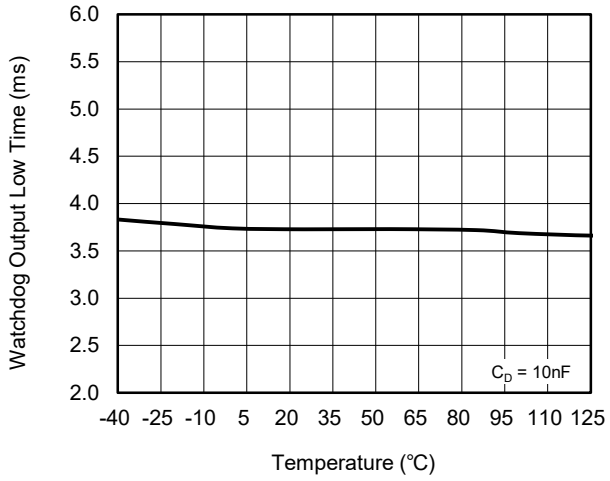
Watchdog Trigger Time vs. Temperature



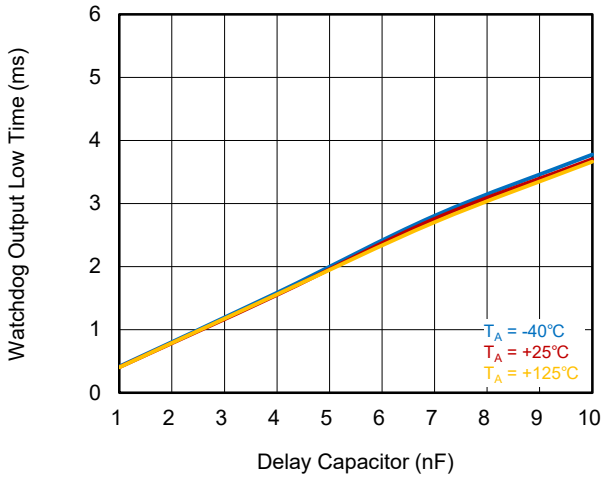
WDI Blanking Time vs. Temperature



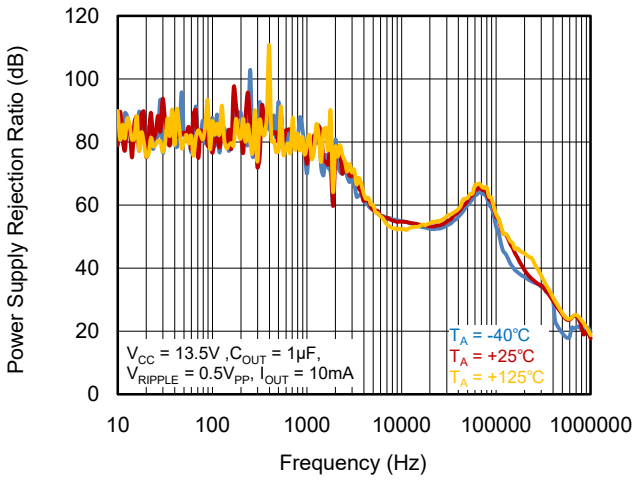
Watchdog Output Low Time vs. Temperature



Watchdog Output Low Time vs. Delay Capacitor



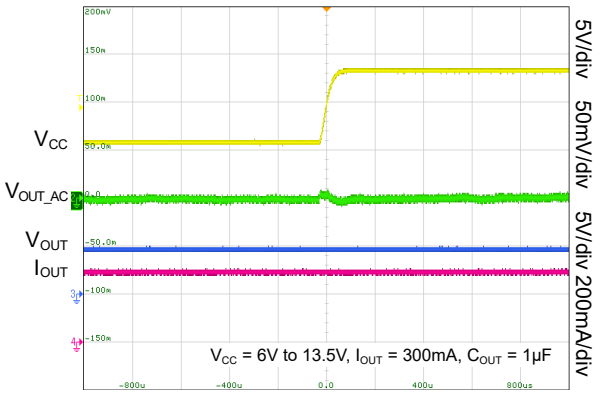
Power Supply Rejection Ratio vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

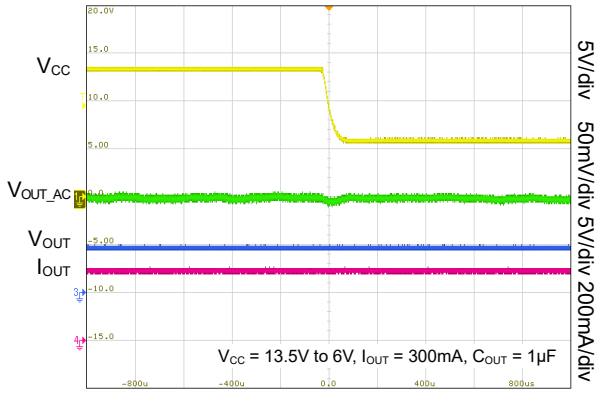
T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

Line Transient



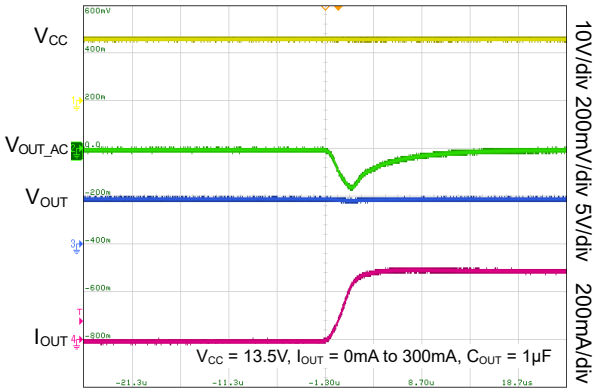
Time (200μs/div)

Line Transient



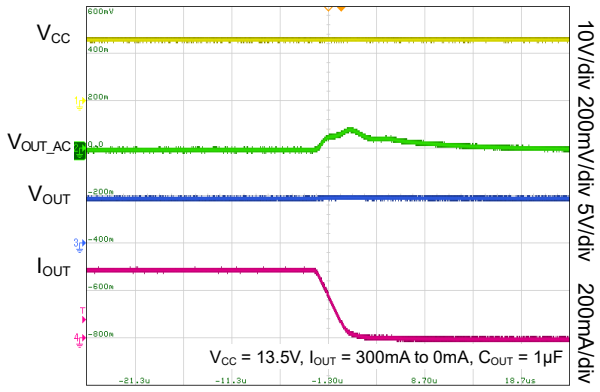
Time (200μs/div)

Load Transient



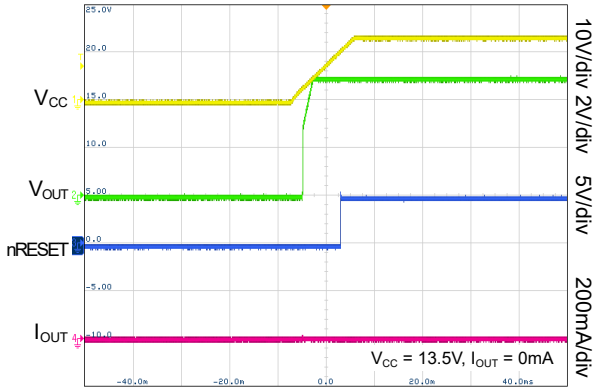
Time (5μs/div)

Load Transient



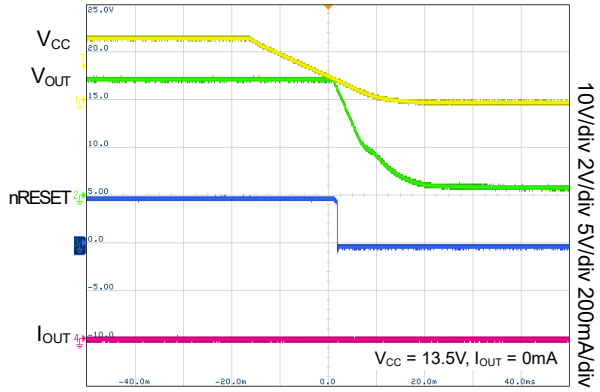
Time (5μs/div)

V_{CC} Power-on



Time (10ms/div)

V_{CC} Power-off

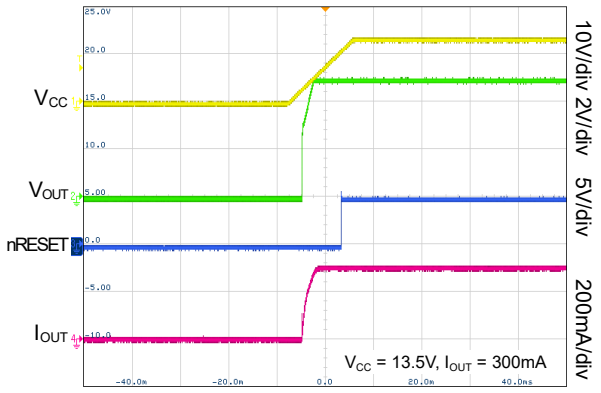


Time (10ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

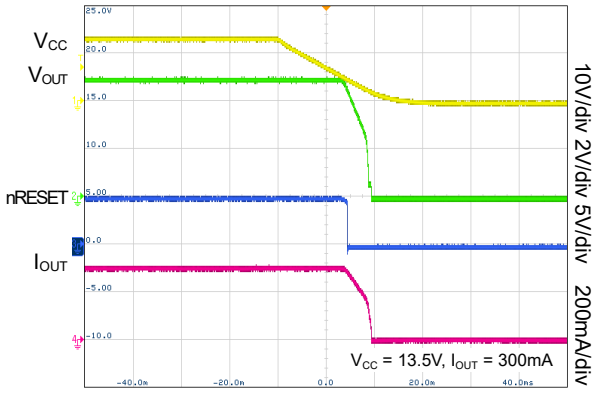
T_A = -40℃ to +125℃, V_{CC} = 13.5V, unless otherwise noted.

V_{CC} Power-on



Time (10ms/div)

V_{CC} Power-off



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

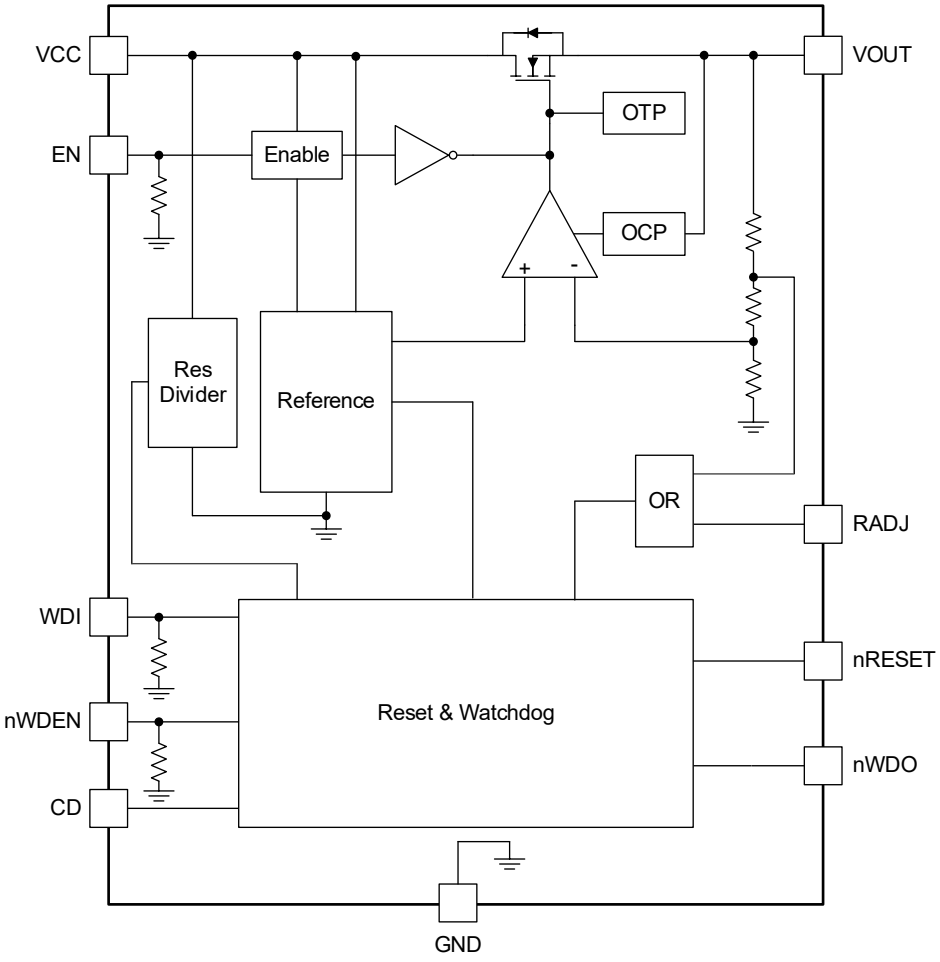


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM70430 is a high precision a low dropout linear regulator with enable, watchdog, reset and user-programmable delay functions. It has low quiescent current 23μA (TYP) at 50μA load and low dropout voltage of 115mV at 100mA load. It also has over-temperature protection and over-current protection. Additionally, it can still work properly under extremely high transient voltage up to 45V.

Voltage Regulator

There is a resistor network inside the SGM70430 to divide the output voltage V_{OUT}. The stability of the regulation loop is governed by the characteristics of the output capacitance, the magnitude of the load current (I_{OUT}), the device junction temperature (T_J), and the underlying internal circuit architecture.

Output Capacitor

System stability depends on the correct choice of the output capacitor. The selected C_{OUT} must comply with the specified limits for both capacitance and ESR. Its value should be determined by the application requirements to provide adequate charge buffering during output load current transients.

Input Capacitors, Reverse Polarity Protection Diode

An input C_{IN} is advised to improve immunity to supply disturbances. The use of a reverse-polarity protection diode with parallel capacitors helps limit input voltage spikes and high-frequency interference. The capacitors should be positioned close to the IC terminals for best performance.

Smooth Ramp-Up

A controlled ramp-up function is implemented to limit output voltage over-shoot during startup. This reduces startup over-shoot and is largely independent of load conditions and output capacitor values.

Output Current Limitation

Under short-circuit or overload conditions, the load current may rise beyond the rated value. The device then activates output current limiting, causing the output voltage to drop accordingly.

Over-Temperature Shutdown

An over-temperature shutdown function protects the device from damage under fault conditions, such as a sustained output short-circuit. When the thermal limit is reached, the device is turned off and automatically restarts after cooling, resulting in a cyclic behavior of the output voltage. Operation with junction temperatures above +150℃ exceeds the maximum ratings and may significantly shorten device lifetime.

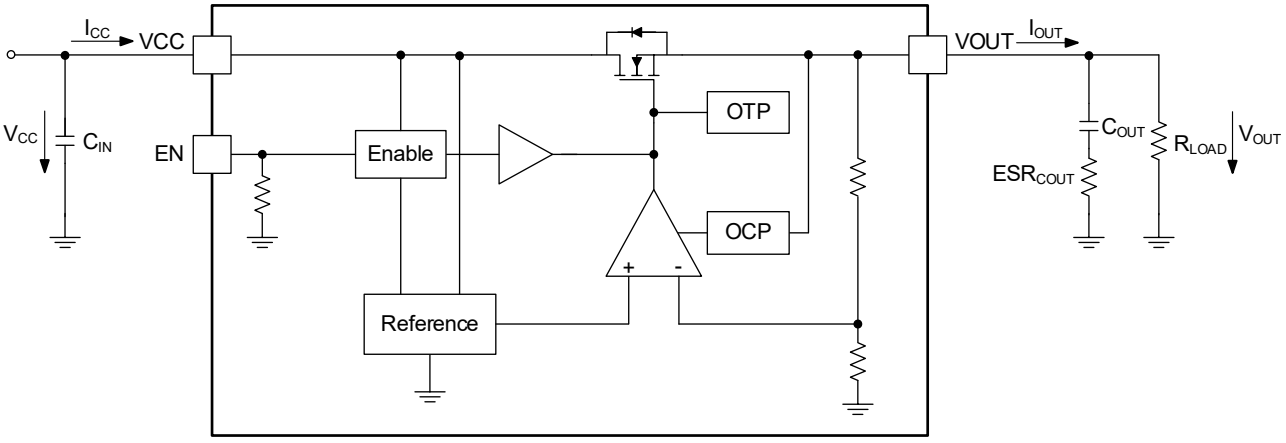


Figure 3. Functional Block Diagram Voltage Regulator Circuit

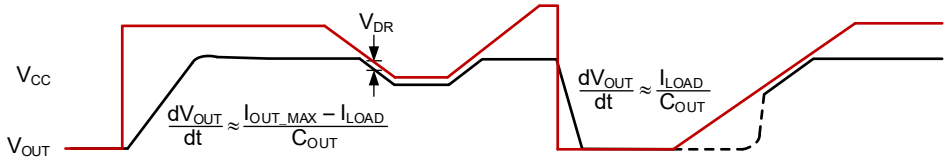


Figure 4. Output Voltage versus Input Voltage

DETAILED DESCRIPTION (continued)

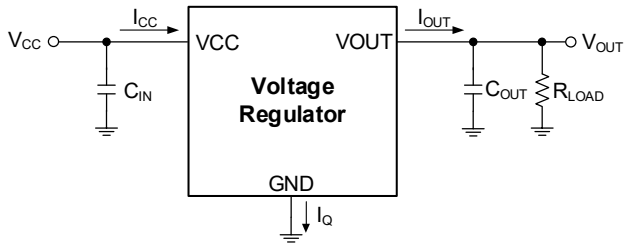


Figure 5. Parameter Definition

Enable

The device is controlled through the EN input. A high level, such as the battery voltage, enables operation, while a low level, such as GND, disables the device. To prevent unintended switching with slowly changing EN signals, an internal hysteresis is implemented.

Reset

The reset function supervises the regulated output voltage V_{OUT} and enables the system or microcontroller to respond to an impending power loss. Selected reset parameters can be configured to match application requirements, as described in the following sections.

Output Under-Voltage Reset Event

When V_{OUT} falls below the output under-voltage reset threshold V_{RT_LOW}, an under-voltage condition is detected and the nRESET output is asserted low. This signal can be used to reset a microcontroller powered by V_{OUT}.

Reset Reaction Time

When the regulator output falls below the under-voltage reset threshold V_{RT_LOW}, the delay capacitor C_D begins to discharge with the current I_{DR_DSCH}. Once the delay voltage V_{CD} reaches the lower delay threshold V_{DR_LOW}, the nRESET output is driven low. The interval between V_{OUT} crossing V_{RT_LOW} and nRESET being asserted low defines the total reset reaction time t_{RR_TOTAL}.

The total reset reaction time t_{RR_TOTAL} equals the delay capacitor discharge time (t_{RR_CD}) plus the device internal response time (t_{RR_INT}).

$$t_{RR\_TOTAL} = t_{RR\_INT} + t_{RR\_CD} \quad (1)$$

where

t_{RR_TOTAL}: Total reset reaction time

t_{RR_INT}: Internal reset reaction time

t_{RR_CD}: Delay capacitor discharge time. For C_D = 10nF see value specified in delay capacitor discharge time.

When the output voltage drop duration is shorter than the reset blanking time t_{RR_BLANK}, the delay capacitor is not discharged and the nRESET output remains inactive. This blanking function avoids unintended microcontroller resets resulting from short output voltage glitches.

Power-On Reset Delay Time

Prior to regulator startup or following an under-voltage reset, the delay capacitor CD is fully discharged. When the regulator output rises above the upper under-voltage reset threshold V_{RT_HIGH}, CD begins charging with the current I_{D_CH}. When the delay voltage V_{CD} rises to the upper threshold V_{DR_HIGH}, the nRESET output is deasserted.

The time elapsed from V_{OUT} exceeding V_{RT_HIGH} to nRESET going high is defined as the power-on reset delay, $t_{D\_PWR\text{-}ON}$. This delay allows sufficient time for microcontroller initialization and is programmable via the external delay capacitor CD connected to the CD pin.

For applications requiring a power-on reset delay different from the value specified for C_D = 10nF, the required capacitor value can be calculated based on the equations provided in the Reset Delay Timing section.

$$C_D = 10nF \times t_{CD\_PWRON}/t_{CD\_PWRON\_10nF} \quad (2)$$

where

t_{CD_PWRON}: Power-on reset delay time as required by the system

$t_{CD\_PWRON\_10nF}$: Power-on reset delay time

C_D: Delay capacitor required

This equation applies when C_D is 1nF or greater. For accurate timing results, the tolerance of the delay capacitor should also be taken into account.

Reset Output (nRESET)

The nRESET output uses an open-drain structure with an internal pull-up resistor. When a lower-impedance nRESET signal is needed, an external pull-up to VOUT may be applied. The minimum external resistor value is limited by the nRESET sink current capability and is provided in the Electrical Characteristics. The timing relationship between VOUT thresholds and nRESET outputs is illustrated in Figure 6.

Reset Output (nRESET) Low for $V_{OUT} \geq 1V$

During an under-voltage reset event, the device holds the nRESET output low as long as V_{OUT} remains at or above 1V, even when the input voltage V_{CC} is 0V. This behavior is supported by powering the reset circuitry from the output capacitor.

DETAILED DESCRIPTION (continued)

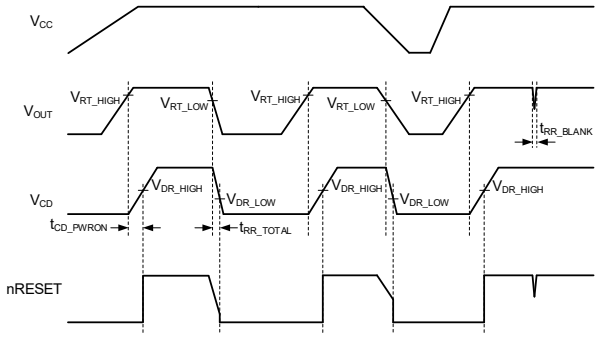


Figure 6. Timing Diagram Reset

Reset Adjust Function

The under-voltage reset threshold can be adapted to application requirements by using an external resistor divider (R_{ADJ_1}, R_{ADJ_2}) connected to the RADJ pin. For the default threshold setting, the RADJ pin should be tied to GND.

When selecting the resistor values, the additional current through the divider must be taken into account. With the divider connected, the adjusted lower under-voltage reset threshold $V_{RT\_LOW\_NEW}$ can be calculated as shown below, assuming the reset adjust pin current I_{RADJ} is negligible. See Figure 7.

$$V_{RT\_LOW\_NEW} = V_{RADJ\_TH} \times (R_{ADJ\_1} + R_{ADJ\_2})/R_{ADJ\_2} \quad (3)$$

where

$V_{RT\_LOW\_NEW}$: Desired reset switching threshold.

R_{ADJ_1}, R_{ADJ_2}: Resistors of the external voltage divider.

V_{RADJ_TH}: Reset adjust switching threshold.

Watchdog

The watchdog supervises the microcontroller to identify timing-related faults. If a required rising edge on the WDI input is not detected within the programmed interval, the watchdog output is asserted low. The watchdog timing is set by an external delay capacitor C_D. Details on valid WDI signal behavior are provided in the following sections.

The watchdog output nWDO is independent of the reset output nRESET and may be used as an interrupt source for the microcontroller. If desired, the nWDO and nRESET pins can be connected together to form a wired-OR configuration with an active-low output. See Figure 8.

Watchdog Inhibit Input (nWDEN)

The watchdog function is controlled by the nWDEN inhibit input. Driving nWDEN high disables the watchdog, during which the capacitor connected to the CD pin is charged to the watchdog hold voltage V_{DW_CD}. The nWDEN input signal must remain within the limits specified in the Watchdog Electrical Characteristics.

Watchdog Output (nWDO)

The nWDO output is implemented as an open-drain output with an internal pull-up resistor. If lower output impedance is required, an external pull-up resistor may be connected to VOUT. Because the nWDO sink current is limited, the minimum permitted value of the external pull-up resistor R_{nWDO_EXT} is defined in the Watchdog Electrical Characteristics.

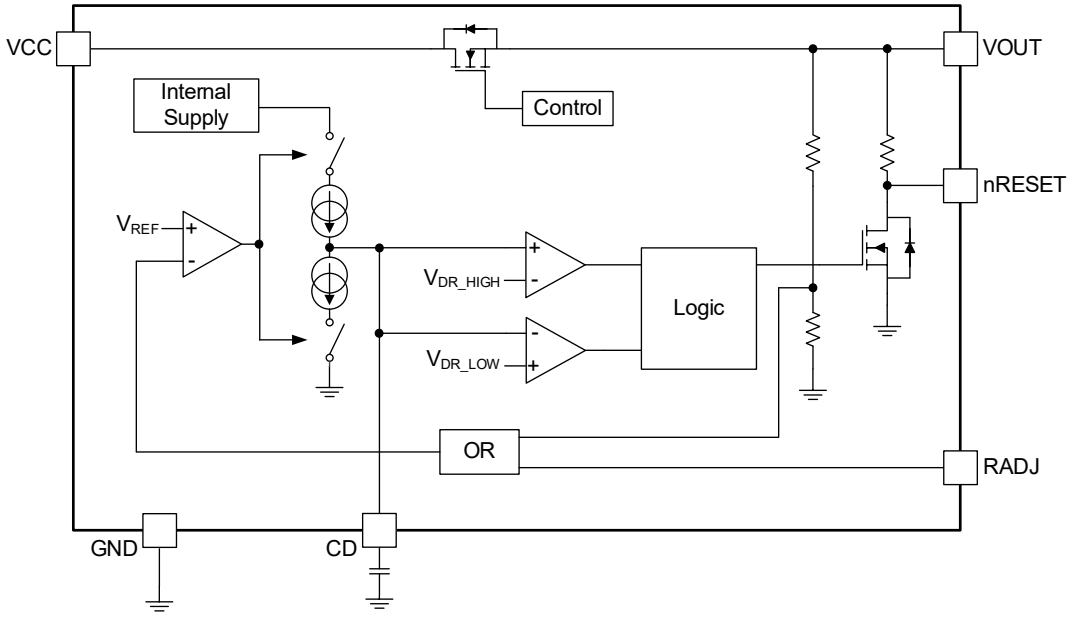


Figure 7. Functional Block Diagram Reset

DETAILED DESCRIPTION (continued)

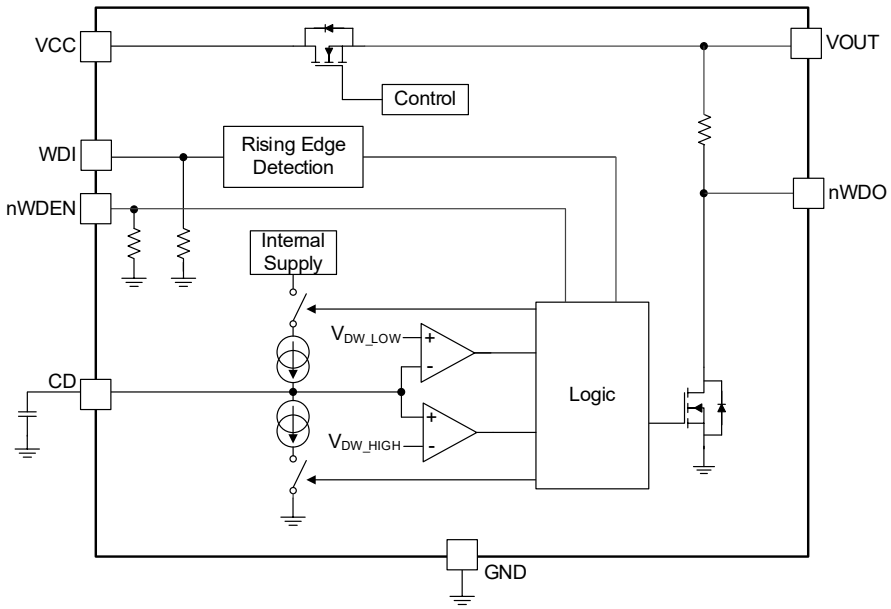


Figure 8. Functional Block Diagram Watchdog Circuit

Watchdog Input (WDI)

A rising edge on the WDI input services the watchdog. Due to the integrated high-pass filtering, the signal amplitude and transition slope at the WDI pin must meet the specifications listed under Watchdog Input (WDI). The applied test pulse is illustrated in Figure 9.

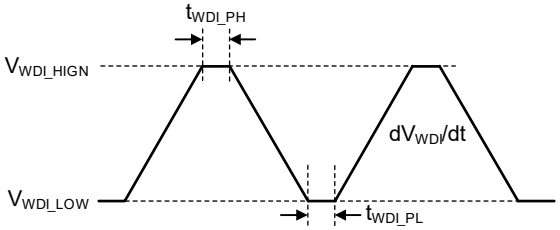


Figure 9. Test Pulses Watchdog Input WDI

Watchdog Timing

When the watchdog is active and no rising edge is detected on the WDI input, the delay capacitor C_D repeatedly charges and discharges between the thresholds V_{DW_LOW} and V_{DW_HIGH}. Each time the capacitor voltage V_{CD} reaches V_{DW_LOW} during discharge, the nWDO output is asserted low for the duration t_{WD_LO}. This cyclic behavior continues with a watchdog period of t_{WD_P}.

If a rising edge on WDI is detected while C_D is discharging, a new charging cycle is initiated. To avoid asserting nWDO low, the WDI rising edge must occur within the watchdog trigger window t_{WDI_TR}.

For applications requiring a watchdog trigger time different from the value specified for C_D = 10nF, the corresponding capacitor value can be calculated using the equations provided in the Watchdog Timing section.

$$C_D = 10nF \times t_{WDI\_TR}/t_{WDI\_TR\_10nF} \quad (4)$$

The watchdog output low time t_{WD_LO} and the watchdog period t_{WD_P} equate to:

$$t_{WD\_LO} = t_{WD\_LO\_10nF} \times C_D/10nF \quad (5)$$

$$t_{WD\_P} = t_{WDI\_TR} + t_{WD\_LO} \quad (6)$$

The formula applies for $C_D \geq 1nF$. For precise timing calculations consider the delay capacitor's tolerance.

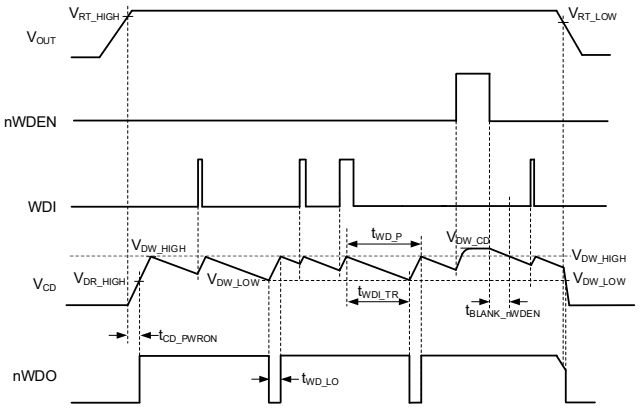


Figure 10. Timing Diagram Watchdog

APPLICATION INFORMATION

Application Diagram

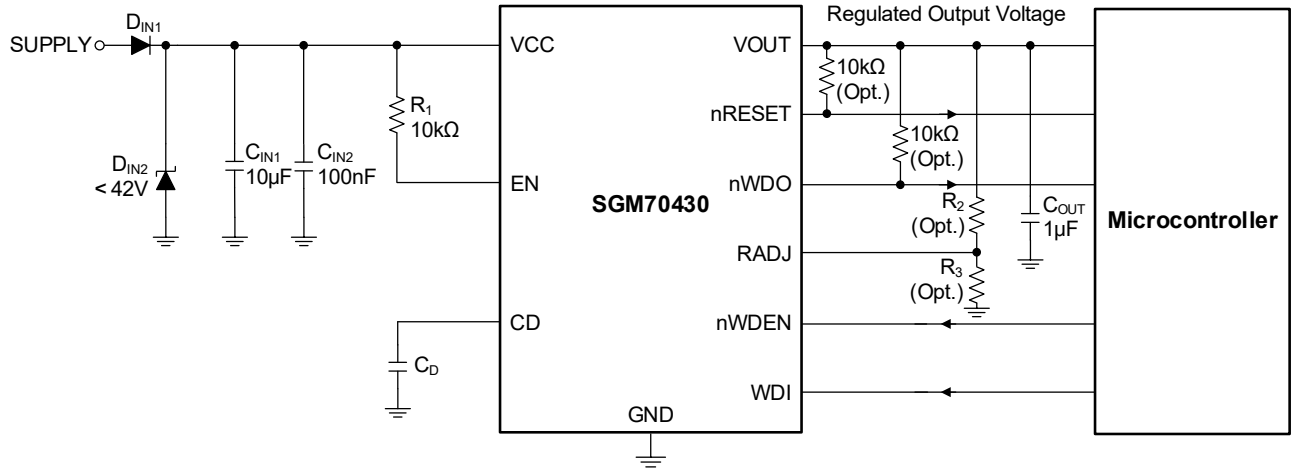


Figure 11. Application Diagram

Selection of External Components

Input Pin

Figure 11 illustrates a typical input configuration for a linear voltage regulator. A ceramic input capacitor with a value between 100nF and 470nF is recommended to attenuate high-frequency line disturbances, such as ISO pulses 3a and 3b, and should be placed as close as possible to the regulator input pin.

To buffer high-energy transients, such as ISO pulse 2a, an aluminum electrolytic capacitor in the range of 10μF to 470μF is suggested at the input. This capacitor should also be located near the input pin on the PCB.

An over-voltage suppressor diode may be added to clamp input voltages that exceed the regulator's maximum rating and to protect the device from over-voltage stress.

While these external input components are not required for basic regulator operation, their use is recommended in environments subject to significant supply disturbances.

Output Pin

An output capacitor is required to ensure stable operation of the linear voltage regulator, with the applicable specifications defined in the functional operating range. The device is optimized for use with very low-ESR capacitors; ceramic capacitors with X5R or X7R dielectric types.

For optimal performance, the output capacitor should be placed as close as possible to the output and GND pins, preferably on the same PCB side as the regulator. Under fast input voltage or load current transients, the capacitor value must be appropriately selected and validated in the target application to maintain output stability.

Thermal Shutdown

When the die temperature exceeds the threshold value of thermal shutdown, the SGM70430 will be in shutdown state and it will remain in this state until the die temperature decreases to +155℃.

Power Dissipation (P_D)

Power dissipation (P_D) of the SGM70430 can be calculated by the equation $P_D = (V_{CC} - V_{OUT}) \times I_{OUT}$. The maximum allowable power dissipation ($P_{D(MAX)}$) of the SGM70430 is affected by many factors, including the difference between maximum junction temperature and ambient temperature ($T_{J(MAX)} - T_A$), package thermal resistance from the junction to the ambient environment (θ_{JA}), the rate of ambient airflow and PCB layout. $P_{D(MAX)}$ can be approximated by the following equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad (7)$$

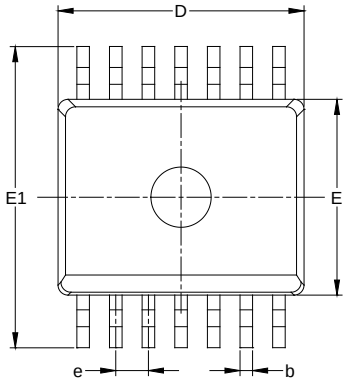
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

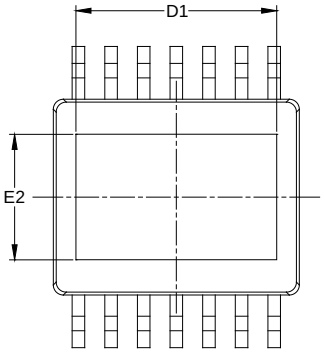
Changes from Original to REV.A (AUGUST 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

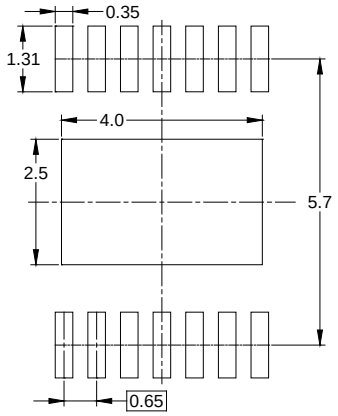
SSOP-14 (Exposed Pad)



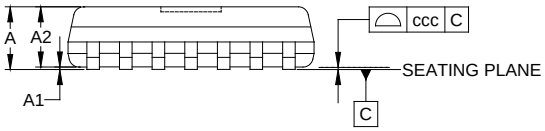
TOP VIEW

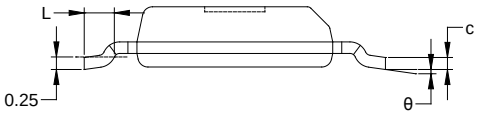


BOTTOM VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



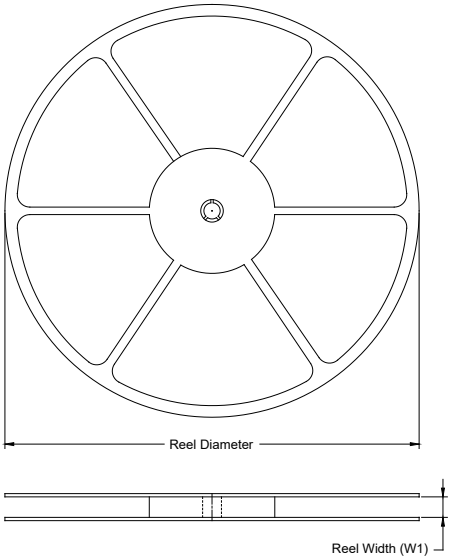


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.400
A1	0.000	-	0.100
A2		1.200 REF	
b	0.200	-	0.300
c	0.190	-	0.280
D	4.800	-	5.000
D1	3.800	-	4.200
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.100	-	2.700
e		0.650 BSC	
L	0.400	-	0.850
θ	0°	-	8°
ccc		0.100	

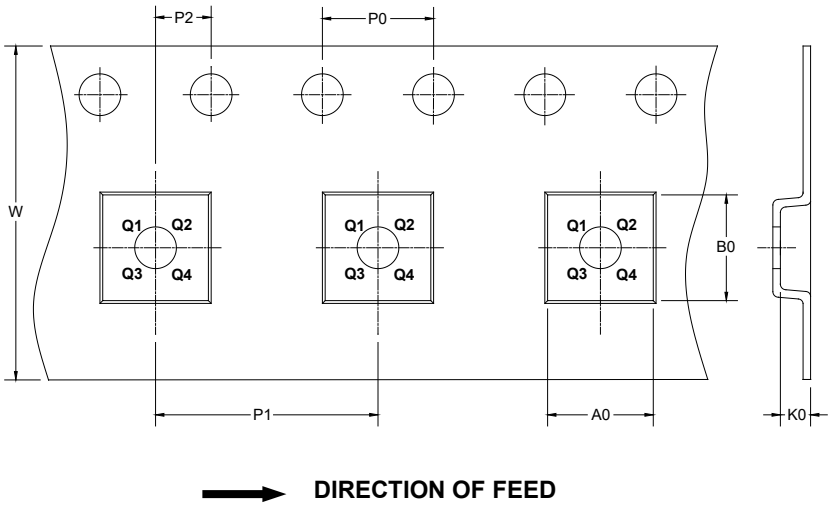
NOTES:
1. This drawing is subject to change without notice.
2. This dimension does not include mold flash, protrusions or gate burrs.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



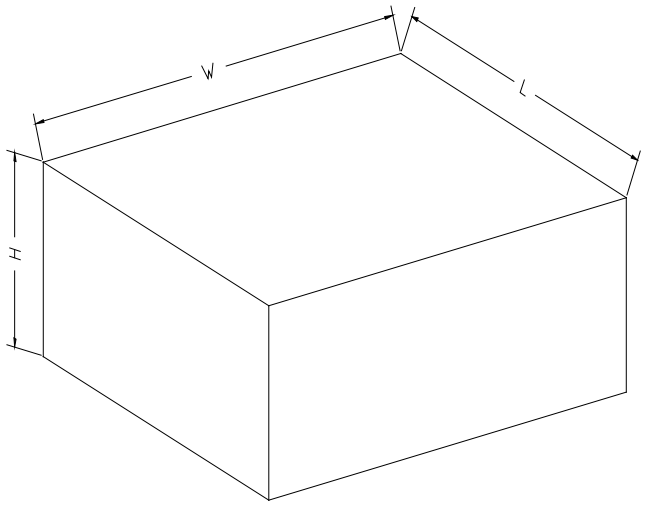
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-14 (Exposed Pad)	13"	12.4	6.50	5.25	1.70	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002