SGM61010A
High Efficiency, 1.5MHz, 1A Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61010A is a high efficiency synchronous Buck DC/DC converter with 1A output current capability and adjustable output voltage. The input supply voltage is in the range of 2.5V to 5.5V.

This device operates with a quasi-fixed 1.5MHz pulse width modulation (PWM) mode for moderate or heavy loads. But at light loads, pulse skip modulation is used for power-save mode (PSM). The PSM operating quiescent current is very low, typically 53μA, which is well suitable for battery powered applications to prolong battery life. Despite such low quiescent current, the transient response to large load variations is excellent. The device shutdown current is 0.05μA (TYP).

The SGM61010A provides an adjustable output voltage by an external resistor divider. The device is capable for low dropout operation with 100% duty cycle. Additional features include an internal soft-start function to limit inrush current, over-current and thermal shutdown protections, an enable input (EN), and input under-voltage lockout (UVLO) protection.

The SGM61010A is available in a Green SOT-23-5 package.

FEATURES

- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Low R_{DSON} for Internal Switches: 230mΩ/150mΩ**
- **Power-Save Mode for Light Load Efficiency**
- **53μA Low Quiescent Current**
- **100% Duty Cycle for Low Dropout Operation**
- **1.5MHz PWM Switching Frequency**
- **Output Discharge Function**
- **Internal Soft-Start Limits the Inrush Current**
- **Over-Current Protection**
- **Thermal Shutdown Protection**
- **Input Under-Voltage Lockout (UVLO) Protection**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Battery Powered Application
General Purpose POL Supply
Set-Top Box
Network Video Camera
Wireless Router
Hard Disk Driver

TYPICAL APPLICATION

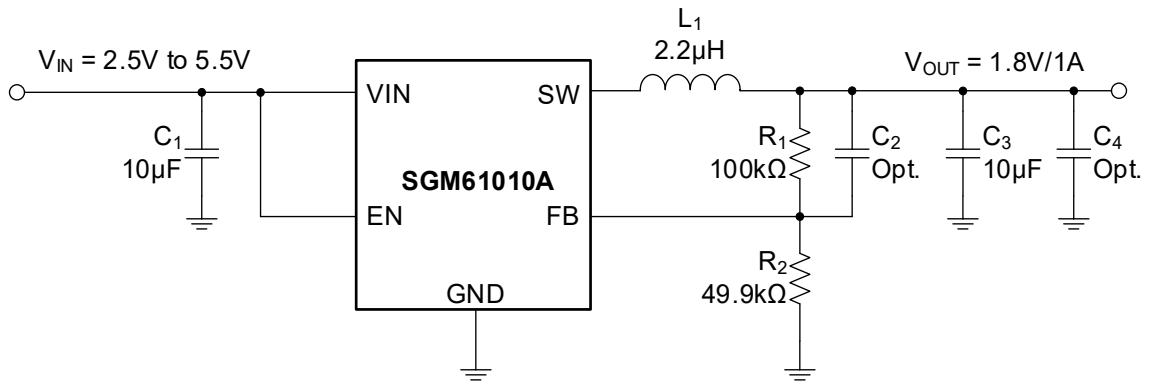


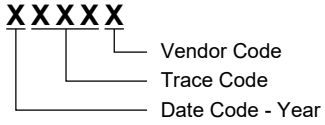
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61010A	SOT-23-5	-40℃ to +125℃	SGM61010AXN5G/TR	23H XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (1)
VIN, EN ..... -0.3V to 6V
SW (DC) ..... -0.3V to V_{IN} + 0.3V
SW (AC, less than 10ns) (2) ..... -2V to 9V
FB ..... -0.3V to 5.5V
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 159.2℃/W
SOT-23-5, θ_{JB} ..... 40℃/W
SOT-23-5, θ_{JC} ..... 77.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (3) (4)
HBM ..... ±1500V
CDM ..... ±1000V

NOTES:

1. All voltage values are with respect to the ground terminal.

2. While switching.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.5V to 5.5V
Output Voltage Range, V_{OUT} ..... 0.6V to V_{IN}
Output Current Range, I_{OUT} ..... 0A to 1A
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

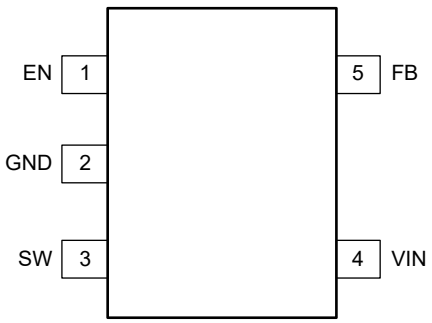
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM61010A (TOP VIEW)



SOT-23-5

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN	DI	Active High Enable Input. Apply a logic low to shut down the device or pull EN up to VIN to enable it. Do not leave EN floating.
2	GND	P	Ground Pin.
3	SW	P	Switching Node Output Pin. Connect to the filter inductor.
4	VIN	P	Power Supply Input. Decouple VIN with at least 10μF ceramic capacitor, close to the device.
5	FB	AI	Feedback Input. Use a resistor divider to feedback the output voltage to this pin and set the output voltage.

NOTE: DI = digital input, AI = analog input, O = output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 5.5V, T_J = -40℃ to +125℃, typical values are at V_{IN} = 5.0V and T_J = +25℃, unless otherwise noted.)

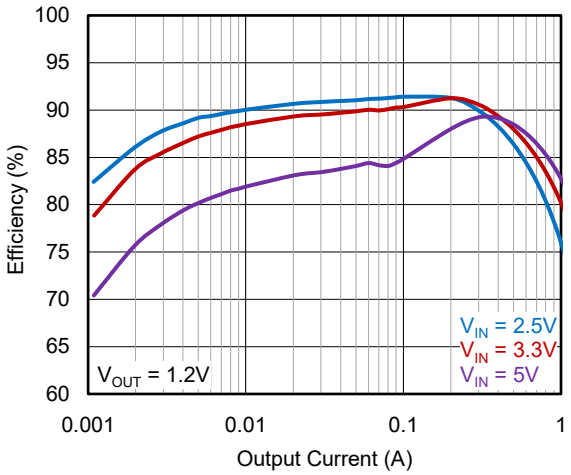
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Input Voltage Range	V_{IN}	Device is functional (Not in UVLO)		2.5		5.5	V
Quiescent Current	I_Q	No switching			53	90	μA
Shutdown Current	I_{SD}	EN = low	T_J = +25℃		0.05	0.5	μA
			T_J = -40℃ to +125℃			3.5	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.09	2.23	2.34	V
Under-Voltage Lockout Hysteresis	V_{HYS}				150		mV
Thermal Shutdown Temperature	T_{JSD}	Junction temperature rising			160		℃
		Junction temperature falling			140		
Logic Interface							
High-Level Threshold at EN Pin	V_{IH}			1.2			V
Low-Level Threshold at EN Pin	V_{IL}					0.4	V
Soft-Start							
Turn On Delay	t_{ON_DLY}	From EN high to SW start switching			110		μs
Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100%			700		μs
Minimum On Time (1)	t_{ON_MIN}	V_{IN} = 5.5V			72		ns
Maximum Duty Cycle	D_{MAX}				100		%
Output							
Feedback Regulation Voltage	V_{FB}	T_J = +25℃		588	600	612	mV
High-side FET On-Resistance	R_{DSON}	V_{IN} = 5V, I_{SW} = 0.5A			230	350	mΩ
Low-side FET On-Resistance					150	240	
High-side FET Current Limit	I_{LIM_HS}	V_{IN} = 5V		1.6	2	2.7	A
Switching Frequency	f_{SW}	V_{OUT} = 1.8V, I_{OUT} = 0.5A, CCM			1.5		MHz
SW Discharge Resistance	R_{DIS}	V_{OUT} = 1.8V, EN = low			48		Ω

NOTE: 1. Specified by design. Not production tested.

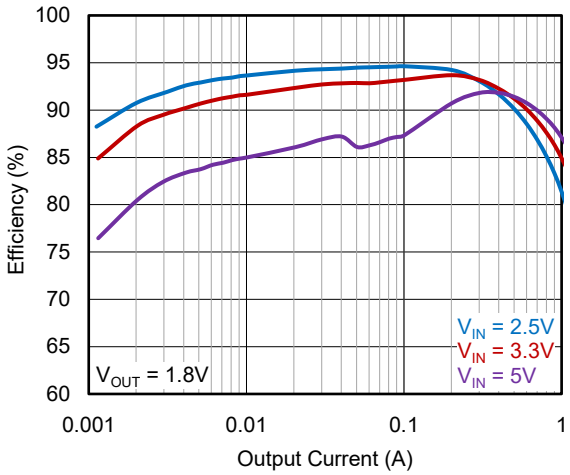
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 2.2μH (DCR = 11.8mΩ), and C_{OUT} = 10μF, unless otherwise noted.

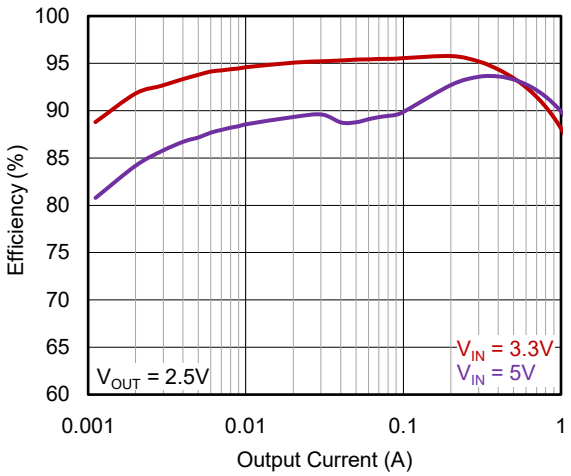
Efficiency vs. Output Current



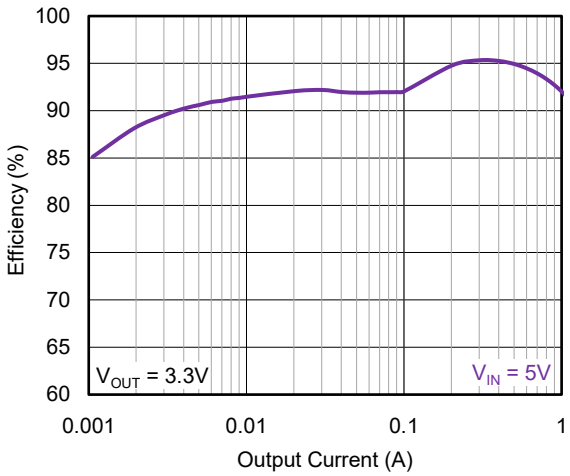
Efficiency vs. Output Current



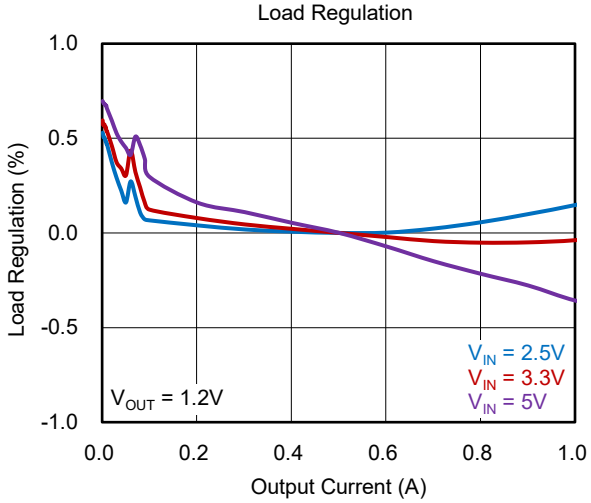
Efficiency vs. Output Current



Efficiency vs. Output Current



Load Regulation



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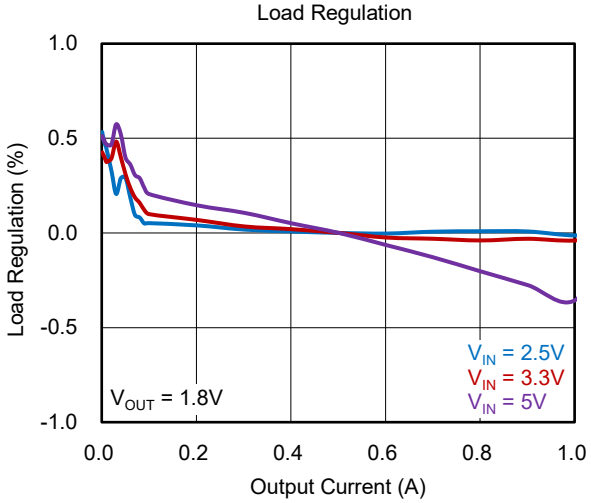
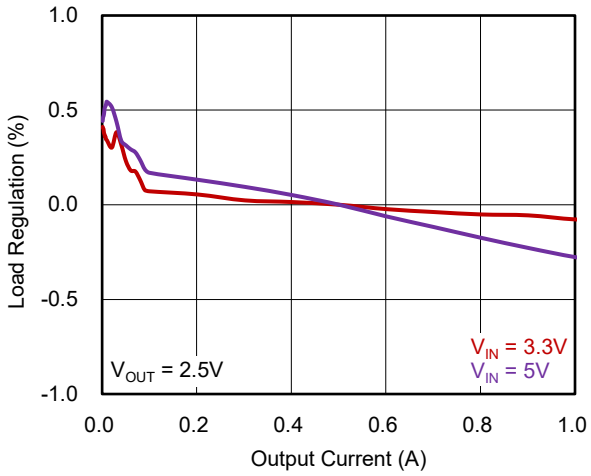


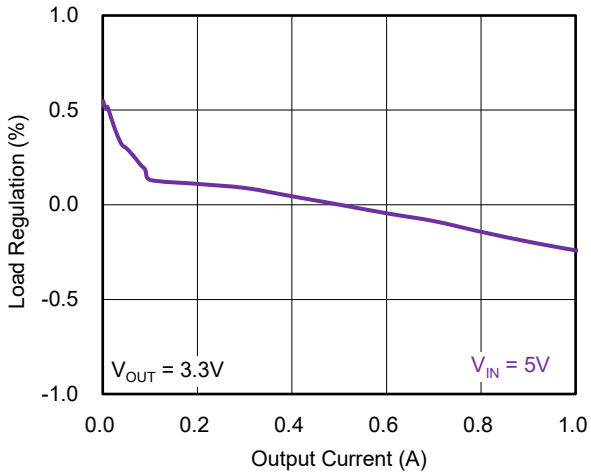
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 2.2μH (DCR = 11.8mΩ), and C_{OUT} = 10μF, unless otherwise noted.

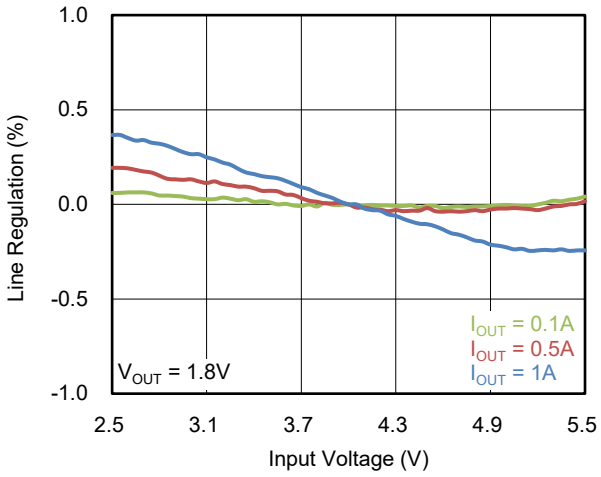
Load Regulation



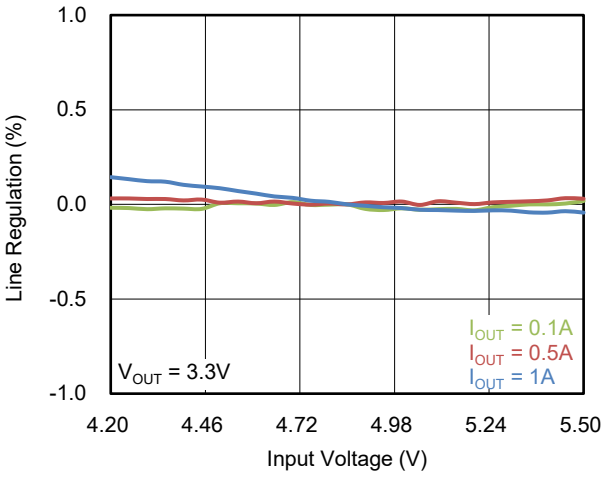
Load Regulation



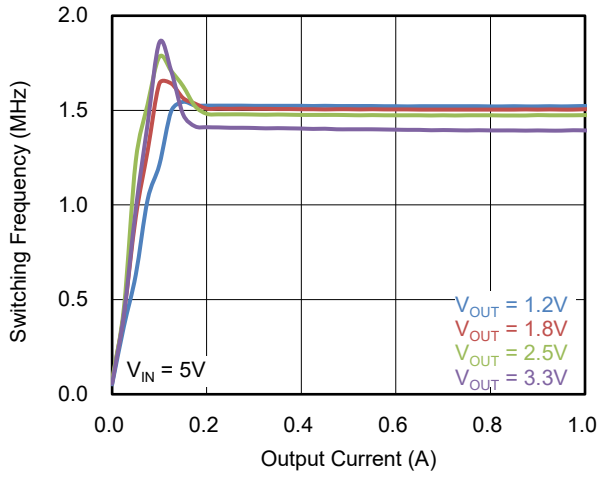
Line Regulation



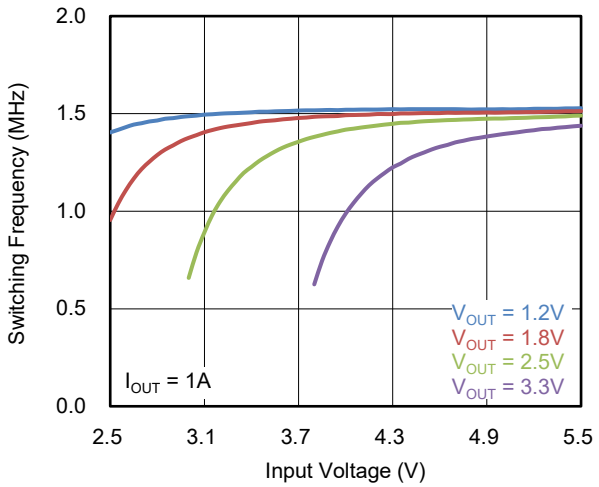
Line Regulation



Switching Frequency vs. Output Current



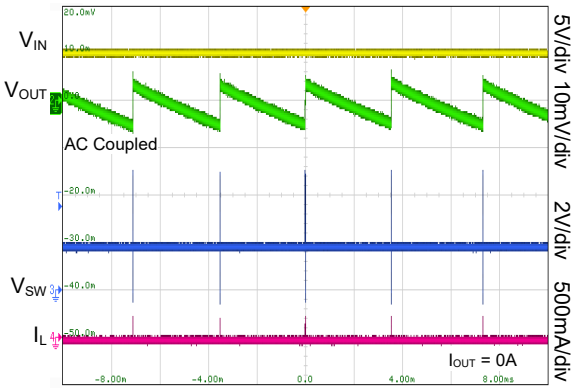
Switching Frequency vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

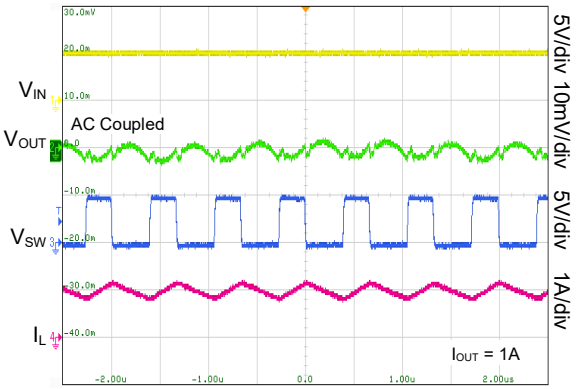
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 2.2μH (DCR = 11.8mΩ), and C_{OUT} = 10μF, unless otherwise noted.

Power Save Mode Operation



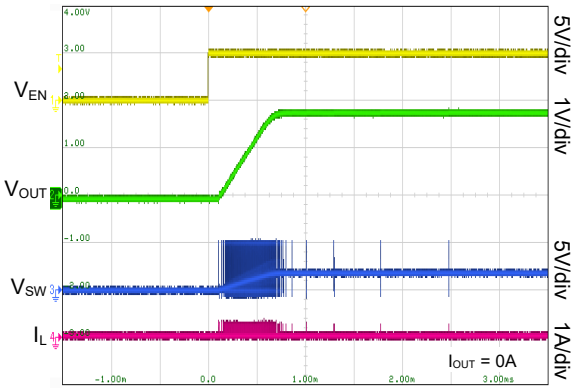
Time (2ms/div)

PWM Operation



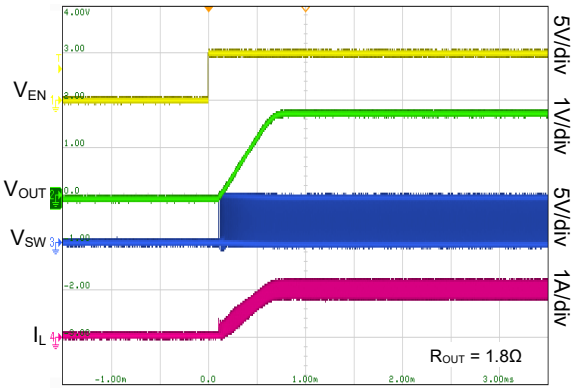
Time (500ns/div)

Startup through EN



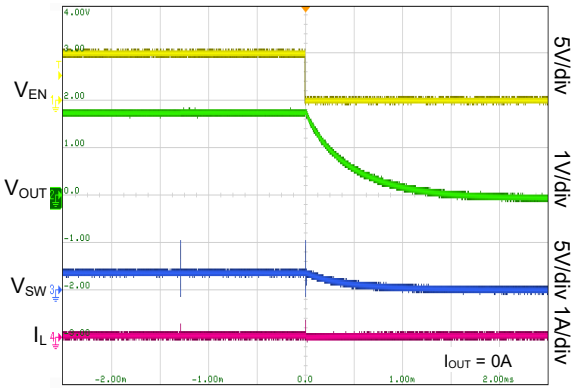
Time (500μs/div)

Startup through EN



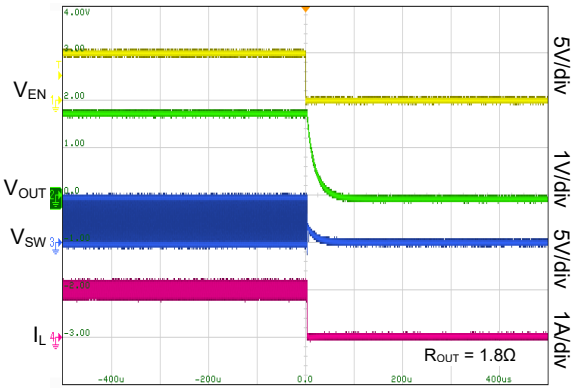
Time (500μs/div)

Shutdown through EN



Time (500μs/div)

Shutdown through EN

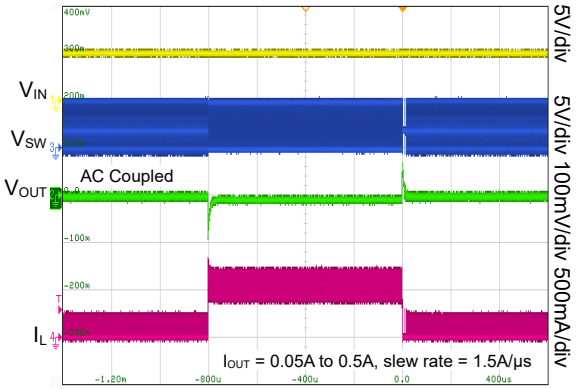


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

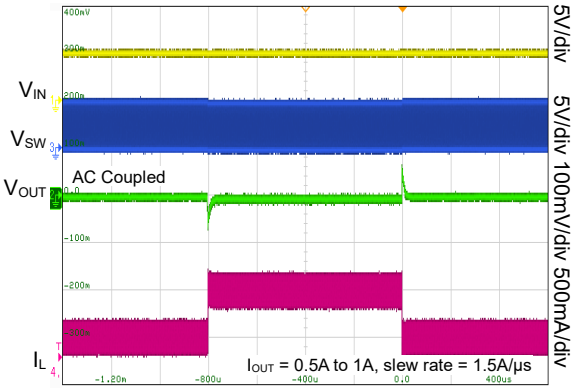
T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 2.2μH (DCR = 11.8mΩ), and C_{OUT} = 10μF, unless otherwise noted.

Load Transient



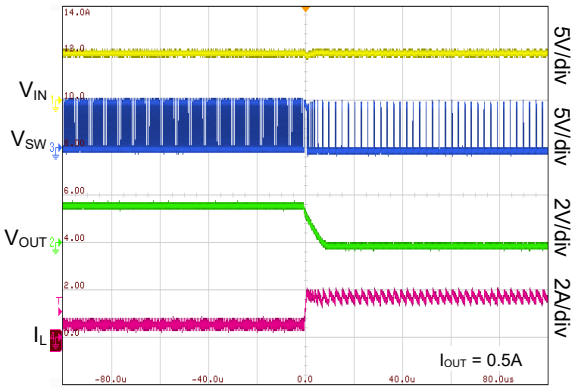
Time (200μs/div)

Load Transient



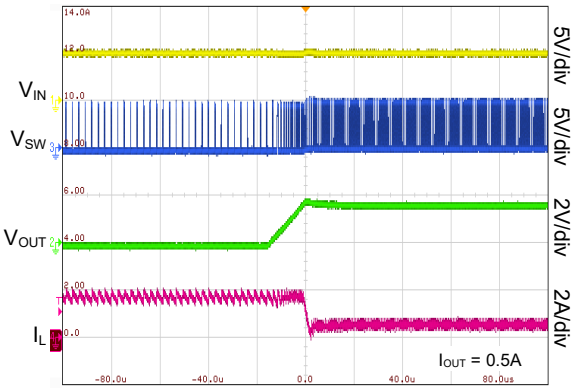
Time (200μs/div)

Short-Circuit Protection Entry



Time (20μs/div)

Short-Circuit Protection Recovery



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

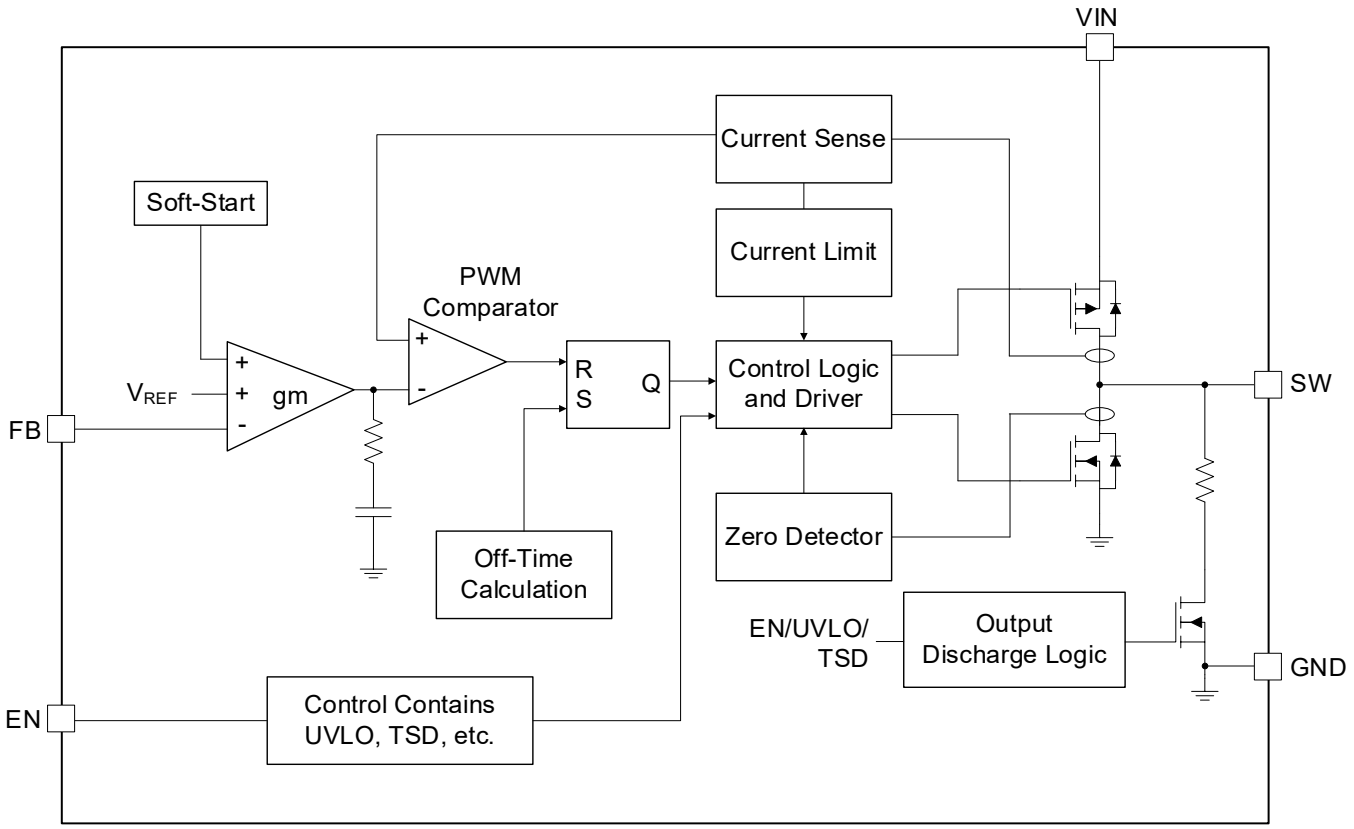


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61010A is a high efficiency Buck switching regulator specifically optimized for handheld battery-powered applications. Utilizing the adaptive off-time PWM control strategy, it operates at a quasi-fixed 1.5MHz switching frequency for moderate to heavy load conditions. This enables the use of compact inductors and capacitors for space-constrained designs.

At light load condition, SGM61010A enters power-save mode (PSM), reducing switching frequency and losses to extend battery life. The PSM quiescent current is typically 53μA while the shutdown current is as low as 0.05μA (TYP).

Under-Voltage Lockout (UVLO)

Operating with insufficient supply voltage can cause device malfunction or failure. The UVLO protection shuts down the device if the input voltage is below the V_{UVLO} threshold. The V_{UVLO} hysteresis is 150mV. When the input voltage exceeds the rising UVLO threshold, the device restarts with a fresh soft startup sequence.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.05μA (TYP). During shutdown, an internal FET is turned on and connects the SW pin to the GND through the internal discharge resistor which is typically 48Ω for smooth discharge of the output. This discharge function is also activated when the shutdown is caused by under-voltage lockout (UVLO) and thermal shutdown.

Soft-Start and Pre-biased Output

A 700μs internal soft-start circuit is included to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage when the device starts up. Soft-start limits inrush current during output capacitor charging and ensures smooth voltage rise. It also prevents input voltage droop when powering from high-impedance sources like primary and rechargeable batteries.

The SGM61010A is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off-period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to start up properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

Power-Save Mode (PSM)

At light load condition, the SGM61010A operates in power-save mode (PSM) to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in PSM. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Pulse Width Modulation (PWM)

In the condition of continuous conduction mode (CCM), which occurs at medium to heavy load the device works in pulse width modulation (PWM) operation. As the load increases, SGM61010A will automatically exit PSM and enter PWM.

Low Dropout Operation (100% Duty Cycle)

When the input voltage gradually drops to the regulation output voltage, the SGM61010A can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

V_{IN_MIN} is minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

DETAILED DESCRIPTION (continued)

Switch Current Limits and Short-Circuit Protection

The SGM61010A implements current limitation by sensing the current of the high-side switch. At the beginning of each cycle, the high-side switch is turned on. If the converter is overloaded or a short occurs on the output, the inductor current sensed by the high-side switch exceeds the maximum current limit threshold. Under this condition, the high-side switch is turned off to avoid damage. The shortened on-time will result in a reduced output voltage.

Note that the measured peak current limit in the closed-loop and open-loop (I_{LIM_HS}) test conditions is slightly different, mainly due to the current comparator propagation delay.

Thermal Shutdown Protection

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +160℃, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

APPLICATION INFORMATION

An application circuit schematic of the SGM61010A with adjustable output is provided in Figure 3.

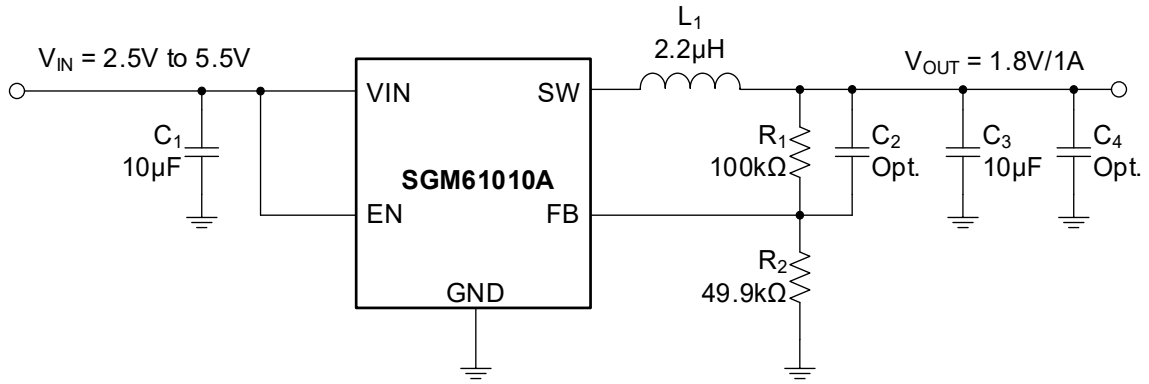


Figure 3. SGM61010A Application Example with 1.8V/1.0A Output

Output Voltage Setting

A resistor divider network (R_1 and R_2 in Figure 3) can be used to set the device output voltage based on the Equation 2. Use a 49.9kΩ resistor for R_2 to compromise between the quiescent current and the bias error/noise immunity of the FB pin.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2}) \quad (2)$$

When V_{IN} decreases to near V_{OUT} value, the switching frequency is decreased and the duty cycle is increased until it reaches 100%.

A feed-forward capacitor (C_2) can be placed in parallel with R_1 to improve the bandwidth and achieve faster transient response and reduce the V_{OUT} ripple in PSM.

Output Capacitor Design

For the device, the output capacitance is generally designed to limit the output voltage ripple below the required level. C_{OUT} also reduces the voltage transients when fast load changes occur. The inductor ripple current that is absorbed by C_{OUT} is determined by L, V_{OUT} and V_{IN}. The output voltage ripple is determined by the interaction of inductor current ripple with the capacitor impedance including its capacitance (C_{OUT}), ESR and ESL values.

During a load transient, the output capacitor provides or absorbs the extra load current alone that results in a droop or quick rise in its voltage, until the loop can respond, and the inductor average current reaches the new load level. The C_{OUT} capacitance determines the transient magnitude. Bias voltage may cause capacitance decreasing significantly if ceramic capacitors are used. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

Note that high ripple current in the capacitor ESR can cause high temperature due to power dissipation in the capacitor. High operating temperature shortens the capacitor lifetime. Therefore, the maximum allowed ripple current in the capacitor must not be exceeded.

Low ESL capacitors can be chosen if ringing in the low megahertz region is seen. Limiting the trace lengths on the PCB or replacing large capacitors with several smaller parallel ones can also help.

To have small output ripple and stable regulation loop, use low-ESR X5R or X7R ceramic capacitors with high ripple current ratings.

The output ripple caused by limited C_{OUT} capacitance and its parasitic ESR can be calculated from Equation 3:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (3)$$

In this example, a 10μF_10V_X7T_0603 ceramic capacitor is used.

APPLICATION INFORMATION (continued)

Inductor Design and Selection

In most cases, a 1μH to 2.2μH inductor works well for the device. Typically, a lower value inductor has a smaller physical size but may result in higher loss due to higher switching frequency required (the lower DCR may compensate for that at heavy loads). For a required ripple (ΔI_L), the inductor can be chosen based on Equation 4:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (4)$$

Typically, the ΔI_L is chosen around 10% to 30% of the maximum load current. For lower output voltage settings, it is recommended to use 1μH inductor to achieve good response and stability.

Inductor manufacturers usually provide thermal current rating (I_{RMS}) and saturation current rating (I_{SAT}). Choose the I_{SAT} above the (I_{LOAD_MAX} + ΔI_L/2) × 1.2 to avoid saturation.

The inductor DCR is also an important factor for efficiency and loss consideration. For better efficiency, SGMICRO suggests to choose the DCR of the inductor as small as possible. More generally, choosing the saturation current above high-side limit is enough.

Input Capacitor Design

The input capacitor provides the converter pulsating and high frequency input currents, and decouples them from the input line. The C_{IN} impedance at the switching frequency should be very low and less than the source impedance to filter the switching currents and prevent them from flowing in the input source. The input voltage ripple must be small for proper regulation and stability. The following Equation 5 can be used to calculate C_{IN} based on the required peak-to-peak input ripple (ΔV_{IN}).

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}{\frac{\Delta V_{IN}}{I_{LOAD}} \times f_{SW}} \quad (5)$$

The worst case, ripple occurs when the duty cycle is near to 50% (V_{OUT}/V_{IN} ≈ 0.5). Use Equation 6 to calculate C_{IN}:

$$C_{IN(MIN)} = \frac{1}{(\frac{\Delta V_{IN}}{I_{LOAD}}) \times 4 \times f_{SW}} \quad (6)$$

Use at least a 10μF low-ESR X5R or X7R ceramic capacitor for C_{IN}. A 10μF capacitor works well for most applications but for better filtering, a larger capacitor can be used. Consider the capacitor rated RMS current for the design. The C_{IN} RMS current is given by Equation 7:

$$I_{RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

In worst case, $I_{RMS(MAX)}$ is equal to 1/2 of the load DC current:

$$I_{RMS(MAX)} = \frac{1}{2} \times I_{LOAD} \quad (8)$$

Note that using long test leads for powering the converter on a lab bench can cause stability issues such as excessive ringing in the output during load transients. It is due to the large inductance of such wires that along with the low-ESR ceramic input capacitors create a high-Q network. Moreover, it can cause errors in loop phase and gain measurements. It is not the case in normal applications with short PCB traces feeding the input. However, if in an application the input inductance cannot be reduced, a high-ESR tantalum or aluminum electrolytic capacitor must be used in parallel with the low-ESR ceramic capacitors to stabilize the system by added the damping to the high-Q network.

LAYOUT CONSIDERATIONS

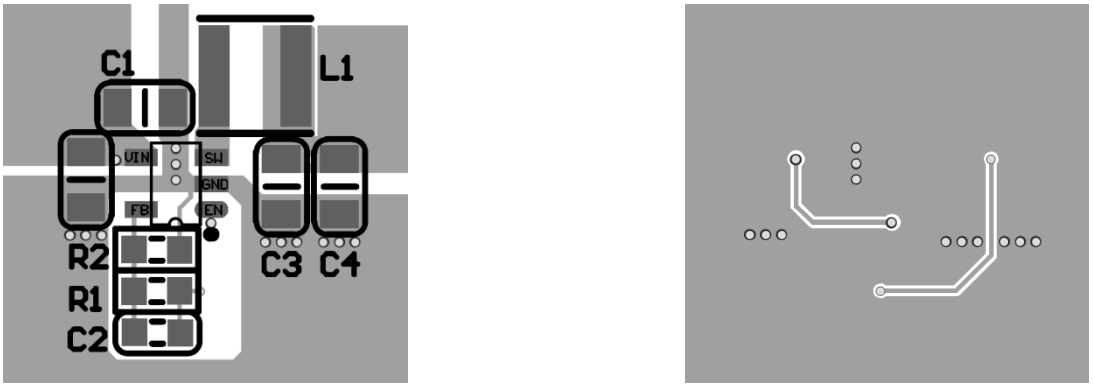
Some important PCB layout design considerations for the SGM61010A are listed below:

• Place the low-ESR input/output capacitors and the inductor as close as possible to the device with short, wide and direct traces on the same layer.

• Connect the GND terminal of the input and output capacitors together and to the device GND pin and the GND power plane in one point.

• Keep the FB feedback traces away from noisy elements or traces such as the SW node.

• Use GND layers under the device, switching traces and inductor for better shielding.



Top Layer　　Bottom Layer

Figure 4. SOT-23-5 PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

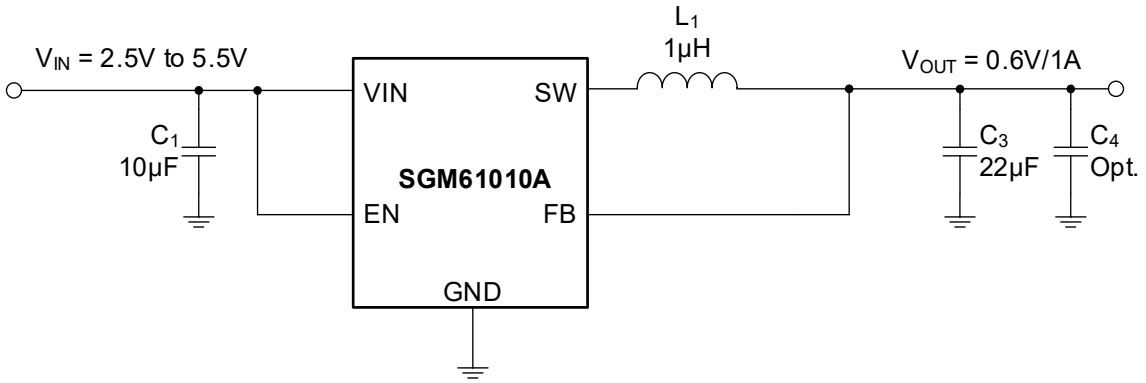


Figure 5. 0.6V Output Voltage Application

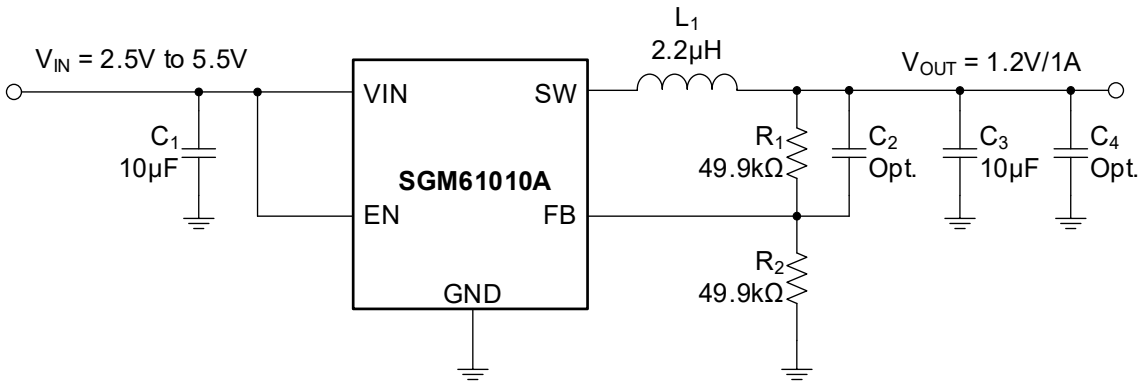


Figure 6. 1.2V Output Voltage Application

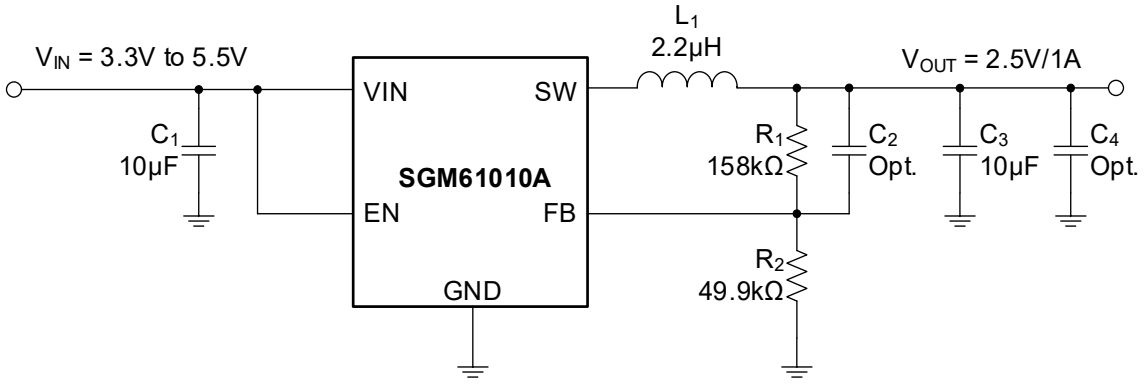


Figure 7. 2.5V Output Voltage Application

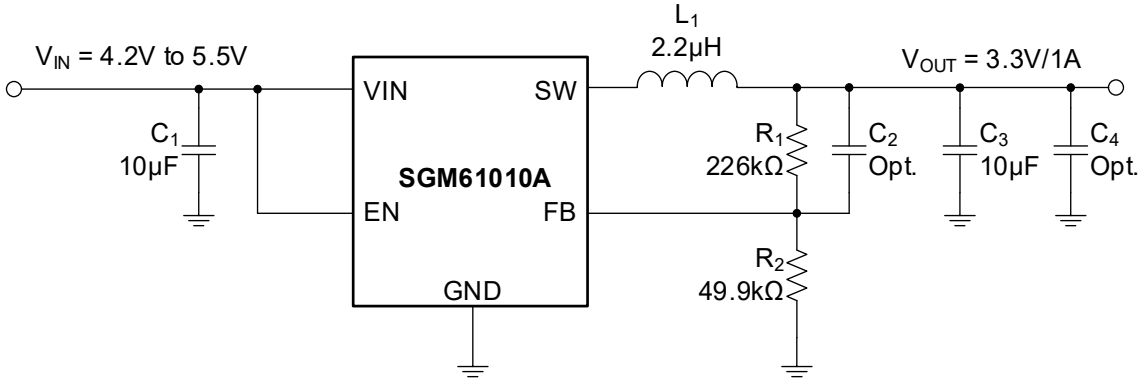


Figure 8. 3.3V Output Voltage Application

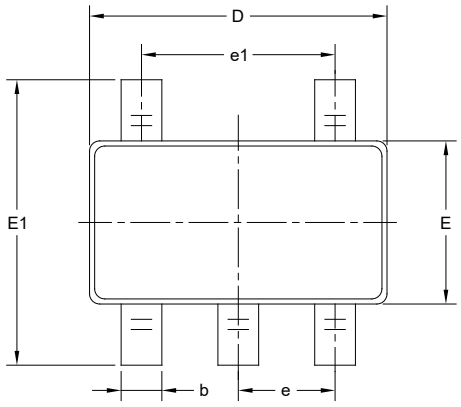
REVISION HISTORY

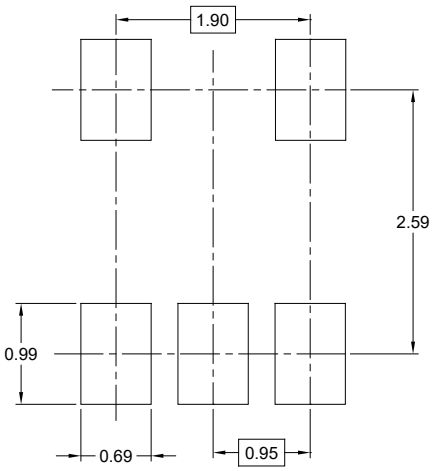
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JULY 2026)	Page
Changed from product preview to production data	All

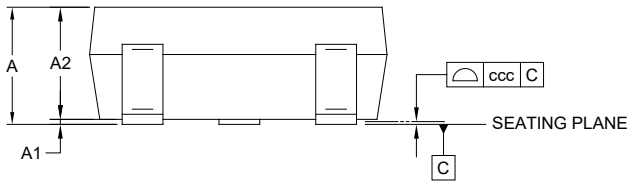
PACKAGE OUTLINE DIMENSIONS

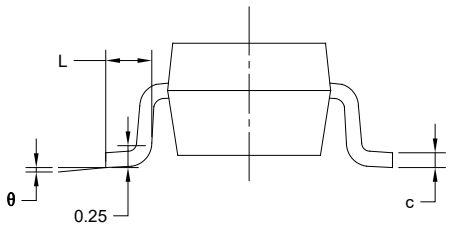
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



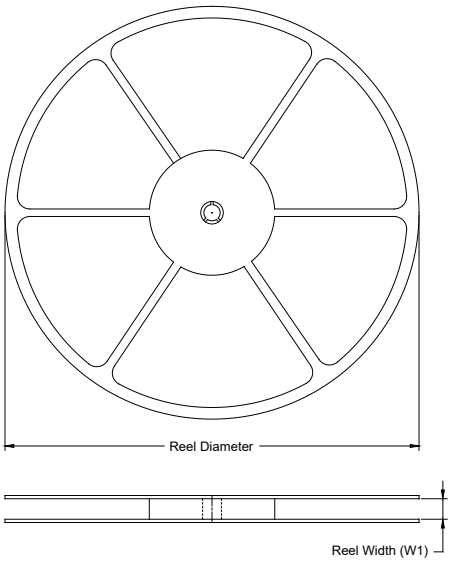


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

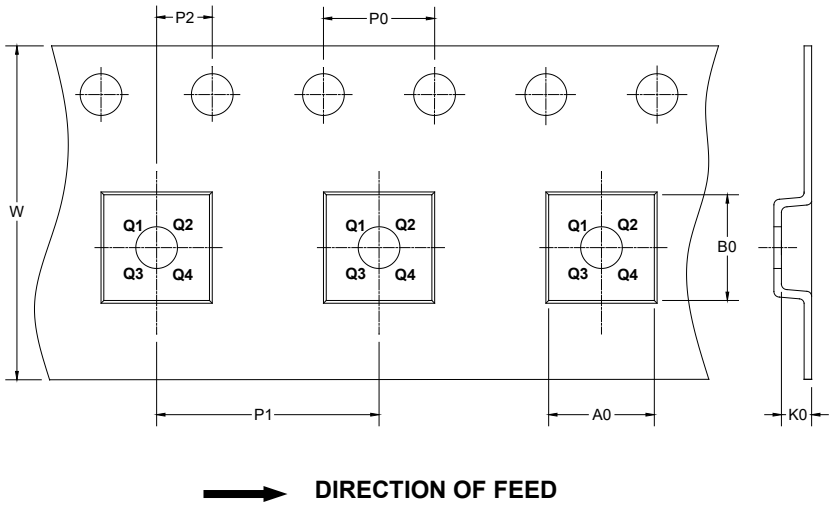
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



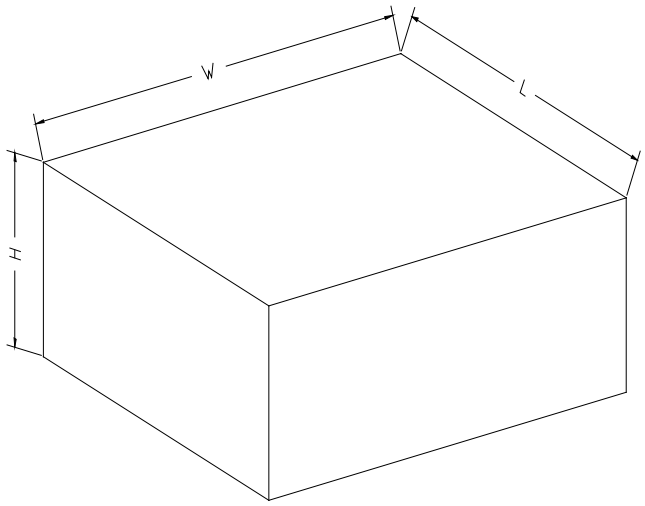
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002