SGM25712A
High-Side ORing FET Controller

GENERAL DESCRIPTION

The SGM25712A is a high-side ORing controller intended for use in the series path of a power supply. Together with an external MOSFET, it replicates the operation of an ideal diode.

By substituting traditional diode rectifiers in industrial electrical systems, this controller minimizes energy dissipation and voltage differentials across the circuit.

The SGM25712A device integrates a charge pump-driven gate driver for an external MOSFET along with a fast comparator to turn off the FET during reverse current events. It operates over a 5V to 75V supply range and accommodates transient voltages as high as 100V.

The SGM25712A also features a FET diagnostic test mode for the system controller to detect shorted MOSFETs.

The SGM25712A is available in a Green SOT-23-6 package.

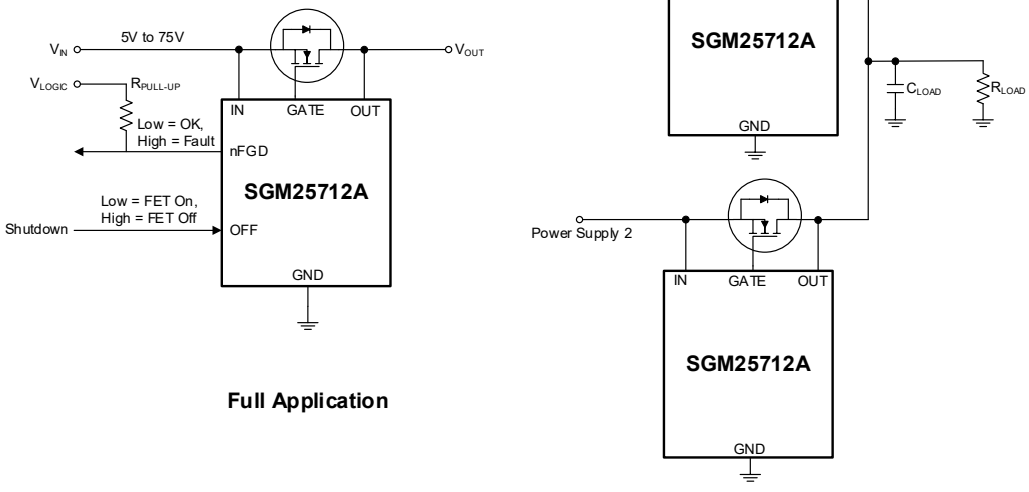
FEATURES

- **Wide Supply Input Voltage Range: 5V to 75V**
- **Transient Capability: 100V**
- **External N-Channel MOSFET Gate Driver with Charge Pump Circuitry**
- **MOSFET Diagnostic Test Mode**
- **Fast 56ns Transient Response to Current Reversal with C_{GATE} = 10nF**
- **2.2A Peak Gate Turn-Off Current for External MOSFET**
- **Minimum V_{DS} Clamping Circuit with Enhanced Turn-Off Speed**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Active ORing of Redundant (N+1)
Power Supplies

TYPICAL APPLICATION



Full Application

Typical Redundant Supply Configuration

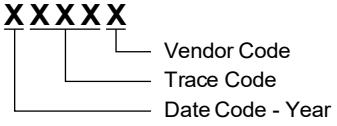
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25712A	SOT-23-6	-40℃ to +125℃	SGM25712AXN6G/TR	XXXXX 347	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, OUT Pins to Ground (1) ..... -0.3V to 100V
GATE Pin to Ground (1) ..... -0.3V to 100V
OFF Pin to Ground ..... -0.3V to 7V
nFGD Pin to Ground (Off) ..... -0.3V to 7V
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 136.1℃/W
SOT-23-6, θ_{JB} ..... 35.8℃/W
SOT-23-6, θ_{JC} ..... 77.9℃/W
Package Thermal Characterization Parameter
SOT-23-6, ψ_{JT} ..... 16.6℃/W
SOT-23-6, ψ_{JB} ..... 34.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. When the SGM25712A is active (OFF pin open/low and V_{IN} > V_{OUT}), the GATE pin typically maintains a 12V voltage differential above the IN pin.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

IN, OUT Pins ..... 5V to 75V
OFF Pin ..... 0V to 5.5V
nFGD Voltage (Off) ..... 0V to 5.5V
nFGD Sink Current (On) ..... 0A to 1mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

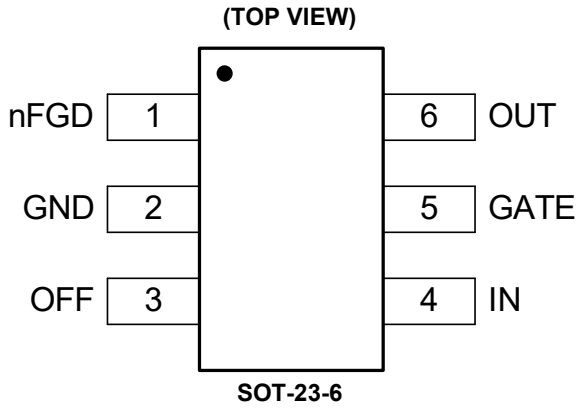
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	nFGD	O	Open Drain Fault Indicator. It should be pulled-up externally with a resistor to a supply voltage no higher than 5.5V. With the OFF pin at logic high, nFGD pulled low indicates that the forward source-to-drain voltage of the external MOSFET exceeds 347mV.
2	GND	G	Ground.
3	OFF	I	External MOSFET Test Mode Input. When the OFF pin is at logic high, the GATE pin is pulled low to turn off the external MOSFET. If the forward source-to-drain voltage of this MOSFET exceeds 347mV, the nFGD pin goes low to indicate that the MOSFET is not shorted. Test mode is disabled when the OFF pin is low or left floating.
4	IN	P	Charge Pump Supply Input and Voltage Sense Connection to the External MOSFET Source Pin.
5	GATE	O	Gate Drive Output. This pin is connected to the external MOSFET gate to control the MOSFET and emulate low forward voltage diode operation.
6	OUT	P	Internal Control Supply Input and Voltage Sense Connection to the External MOSFET Drain Pin.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{OUT} = 12V, V_{OFF} = 0V, C_{GATE} = 47nF, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Pin						
Operating Supply Range	V_{IN}		5		75	V
Operating Supply Current	I_{IN}	V_{IN} = 5V, GATE = open, V_{OUT} = V_{IN} - 100mV	100	163	230	μA
		V_{IN} = 12V, GATE = open, V_{OUT} = V_{IN} - 100mV	140	225	320	
		V_{IN} = 75V, GATE = open, V_{OUT} = V_{IN} - 100mV	150	242	340	
OUT Pin						
OUT Pin Current	I_{OUT}	V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV	45	75	110	μA
		V_{IN} = 12V, V_{OUT} = V_{IN} - 100mV	45	75	110	
		V_{IN} = 75V, V_{OUT} = V_{IN} - 100mV	50	79	115	
GATE Pin						
GATE Pin Source Current	I_{GATE_ON}	V_{IN} = 5V to 75V, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV	17	32	47	μA
V_{GATE} - V_{IN} in Forward Operation (1)	V_{GS}	V_{IN} = 5V, V_{OUT} = V_{IN} - 175mV	7	8.4	10	V
		V_{IN} = 12V, V_{OUT} = V_{IN} - 175mV	10	11.8	14	
		V_{IN} = 75V, V_{OUT} = V_{IN} - 175mV	10.5	12.2	14.5	
Gate Capacitance Discharge Time at Forward to Reverse Transition (See Figure 2)	t_{GATE_REV}	C_{GATE} = 0F (2)		23 (4)	100 (4)	ns
		C_{GATE} = 10nF (2)		56		
		C_{GATE} = 47nF (2)		154	338	
Gate Capacitance Discharge Time at OFF pin Low to High Transition (See Figure 3)	t_{GATE_OFF}	C_{GATE} = 47nF (3)		342		ns
GATE Pin Sink Current	I_{GATE_OFF}	V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t ≤ 10ms	1.3	2.2		A
Reverse V_{SD} Threshold	V_{SD_REV}	V_{IN} - V_{OUT}	-56	-33	-10	mV
Reverse V_{SD} Hysteresis	ΔV_{SD_REV}			9		mV
Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{SD_REG}	V_{IN} = 5V, V_{IN} - V_{OUT}	2	15	28	mV
		V_{IN} = 12V, V_{IN} - V_{OUT}	2	15	28	
OFF Pin						
OFF Input High Threshold Voltage	V_{OFF_IH}	V_{OUT} = V_{IN} - 500mV, V_{OFF} rising		1.56	1.73	V
OFF Input Low Threshold Voltage	V_{OFF_IL}	V_{OUT} = V_{IN} - 500mV, V_{OFF} falling	1.09	1.43		V
OFF Threshold Voltage Hysteresis	ΔV_{OFF}	V_{OFF_IH} - V_{OFF_IL}		130		mV
OFF Pin Internal Pull-Down	I_{OFF}	V_{OFF} = 5V	2	5.1	8	μA
nFGD Pin						
FET Test Threshold Voltage V_{OUT} < V_{IN}	V_{SD_TST}	V_{OFF} = 5V, V_{IN} = 12V, V_{OUT} falling from 12V	250	347	450	mV
FET Test Threshold Voltage Hysteresis	ΔV_{SD_TST}			95		mV
nFGD Output Low Voltage, nFGD Output = On	$nFGD_{VOL}$	V_{OFF} = 5V, I_{nFGD} = 1mA Sinking		617	850	mV
nFGD Output Leakage Current, nFGD Output = Off	$nFGD_{IOL}$	V_{OFF} = 0V, V_{nFGD} = 5.5V		0.004	0.7	μA

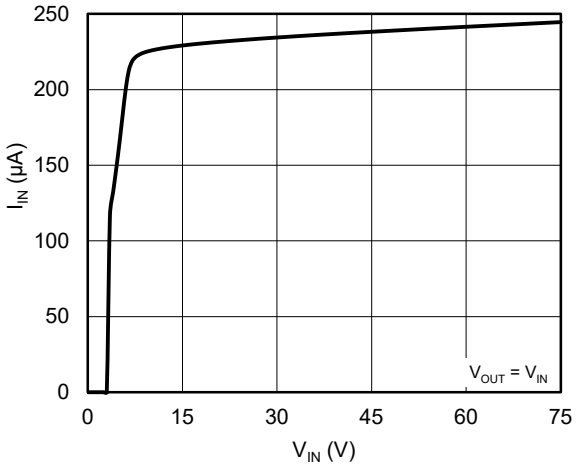
NOTES:

1. Measurement of V_{GS} voltage (V_{GATE} - V_{IN}) includes 1MΩ in parallel with C_{GATE}.
2. The time required for the GATE voltage to drop to V_{IN} + 1V after a (V_{IN} - V_{OUT}) transition from 200mV to -500mV. See Figure 2.
3. The time required for the GATE voltage to reach V_{IN} + 1V after a V_{OFF} transition from 0V to 5V. See Figure 3.
4. Guaranteed by design, not tested in production.

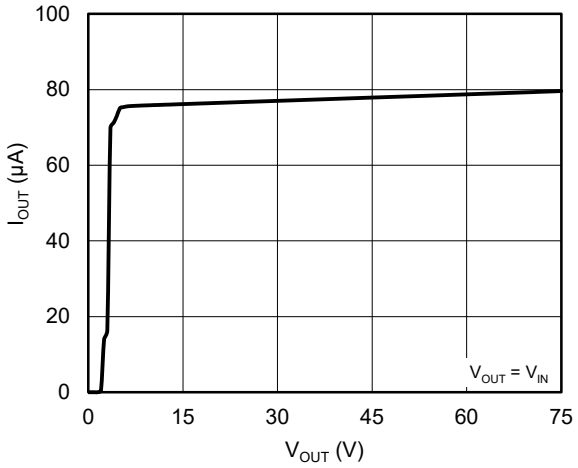
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OFF} = 0V, unless otherwise noted.

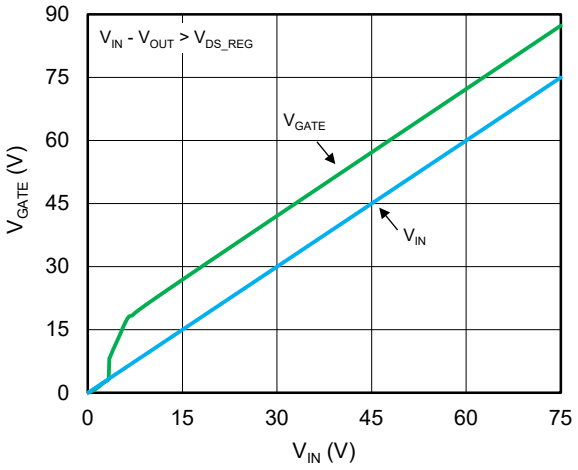
I_{IN} vs. V_{IN}



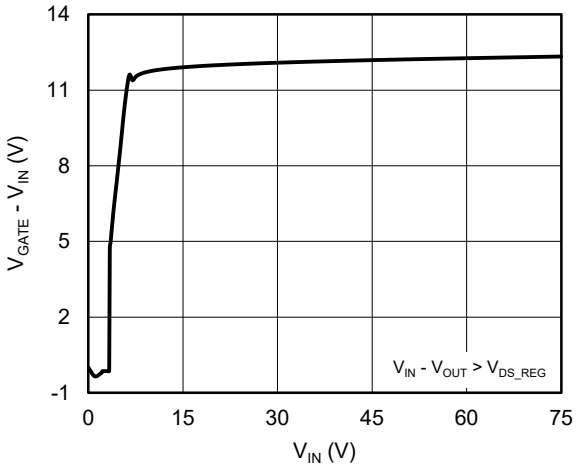
I_{OUT} vs. V_{OUT}



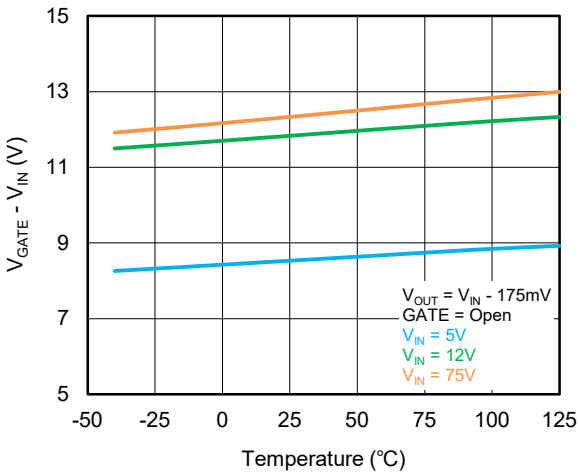
V_{GATE} vs. V_{IN}



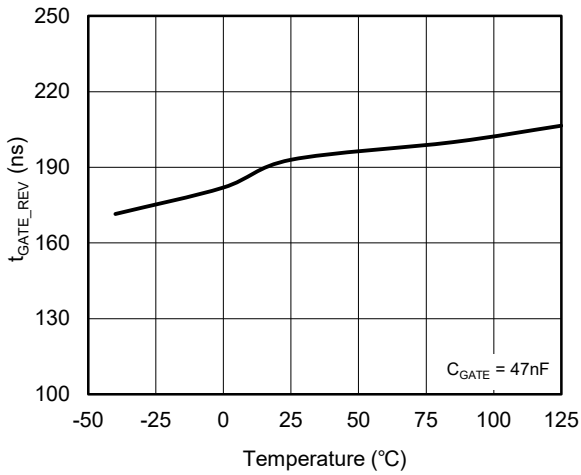
V_{GATE} - V_{IN} vs. V_{IN}



V_{GATE} - V_{IN} vs. Temperature



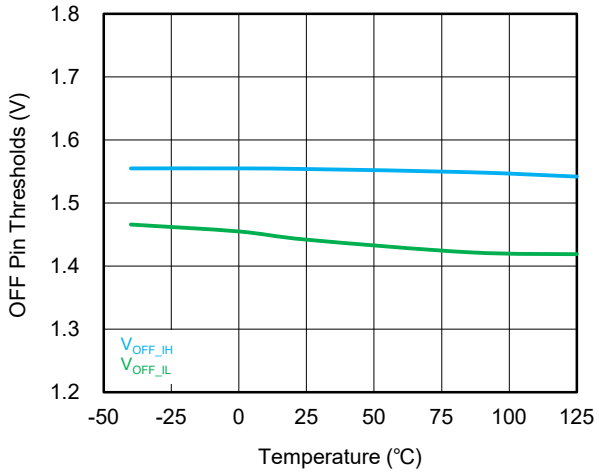
t_{GATE_REV} vs. Temperature



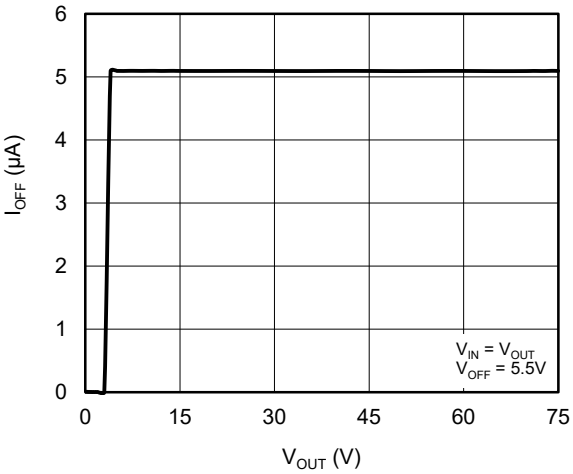
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OFF} = 0V, unless otherwise noted.

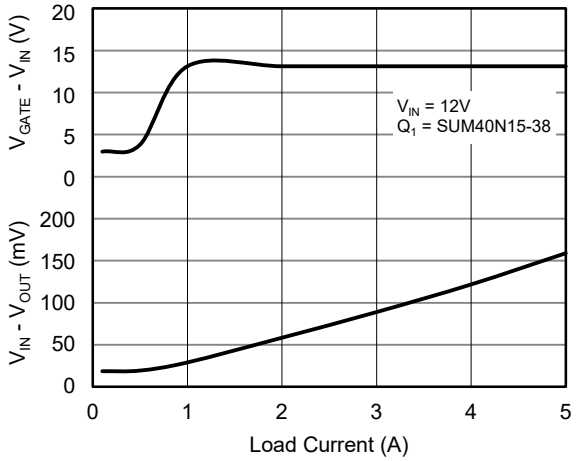
OFF Pin Thresholds vs. Temperature



OFF Pin Internal Pull-Down vs. V_{OUT}



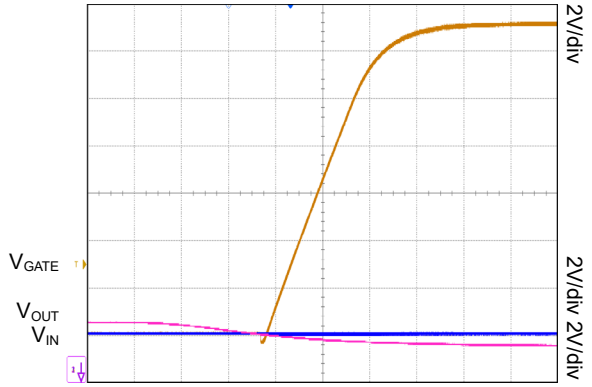
GATE Pin vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

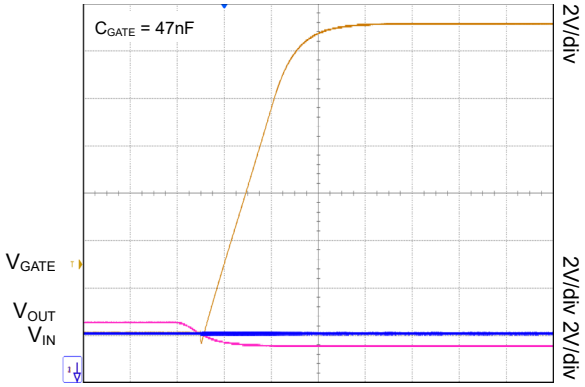
T_A = +25℃, C_{GATE} = 10nF, V_{IN} = 12V, I_{LOAD} = 5A, C_{OUT} = 0F, Q_1 = SUM40N15-38, unless otherwise noted.

Forward C_{GATE} Charge Time



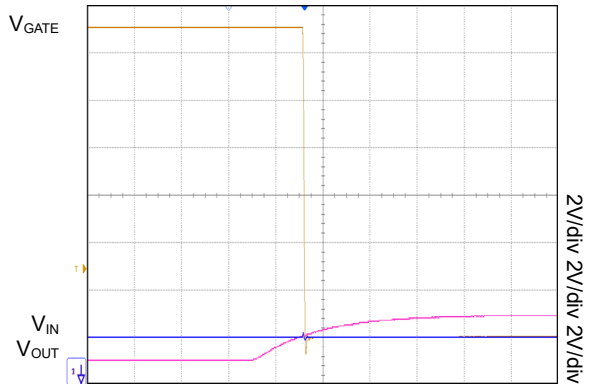
Time (2ms/div)

Forward C_{GATE} Charge Time



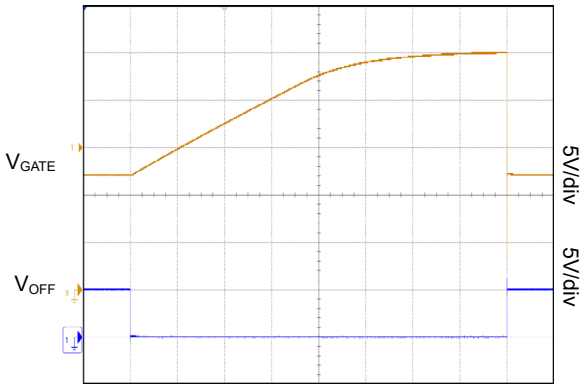
Time (10ms/div)

Reverse C_{GATE} Discharge



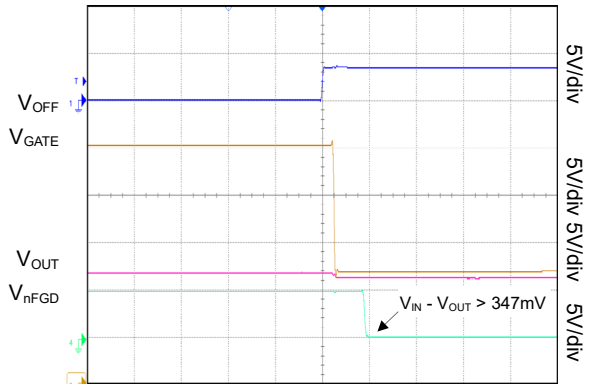
Time (1μs/div)

C_{GATE} Charge and Discharge vs. OFF Pin



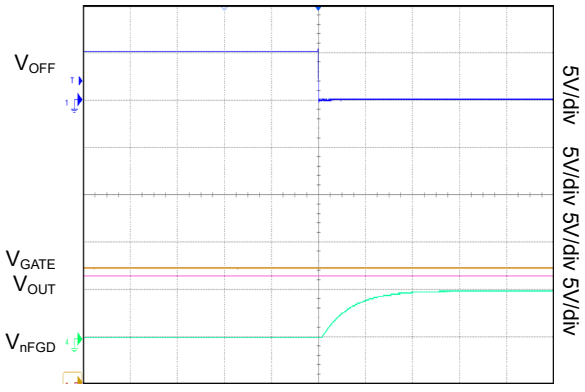
Time (1ms/div)

OFF Pin, On to Off Transition



Time (1μs/div)

OFF Pin, Off to On Transition



Time (5μs/div)

TIMING DIAGRAMS

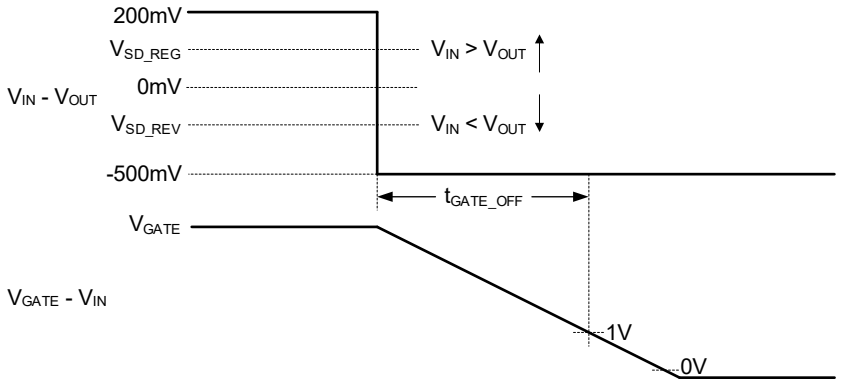


Figure 2. Forward to Reverse Transition Gate Off Timing Diagram

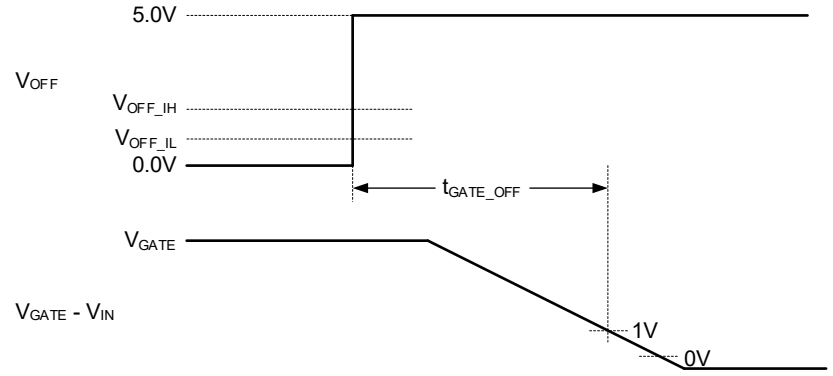


Figure 3. OFF Pin Low to High Transition Gate Off Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

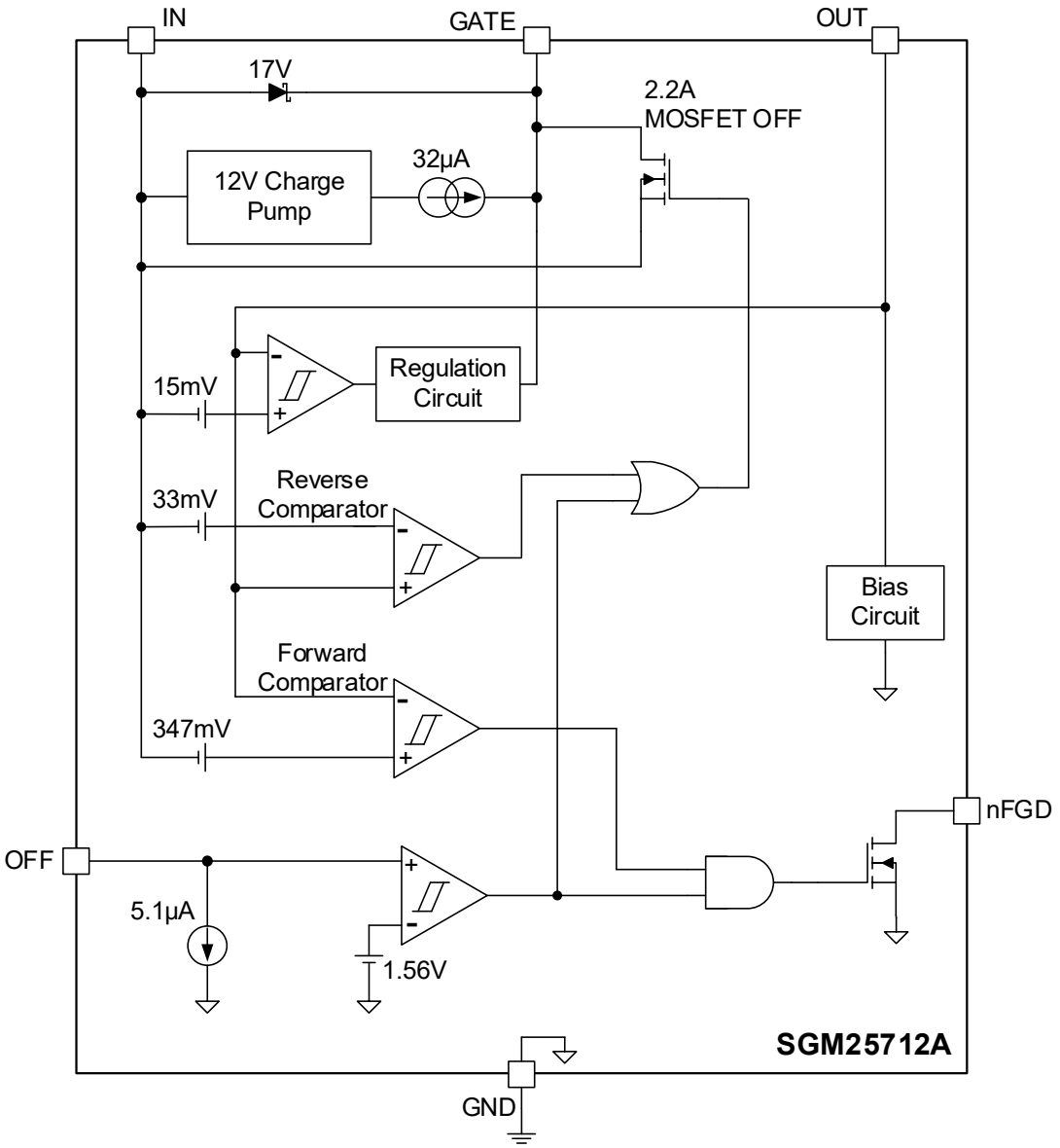


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

To achieve greater reliability, systems requiring high availability typically incorporate multiple redundant power supplies wired in parallel. Connecting these supplies to a common load point is usually accomplished through Schottky ORing diodes. Compared with an ORing diode, an N-channel MOSFET adds only a small amount of complexity, yet it avoids the diode's forward voltage drop and the power losses that grow with load current. It also reduces, or eliminates, the need for diode heat sinks or large thermal copper areas in circuit board layouts for high-power applications.

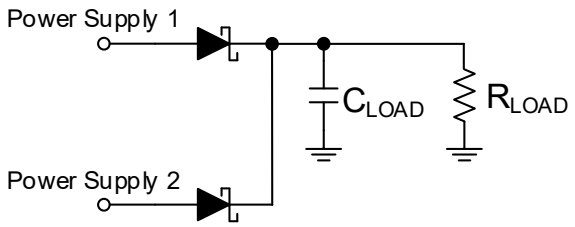


Figure 5. ORing with Diodes

The SGM25712A is a high-side ORing controller designed to drive an external N-channel MOSFET, thereby supplanting conventional ORing diodes. It monitors the source-drain voltage via the IN and OUT pins, and modulates the MOSFET's gate signal (via the GATE pin) to regulate its operation dynamically. This configuration enables diode-like rectification behavior, where the MOSFET's source and drain terminals function analogously to a diode's anode and cathode respectively, but with idealized low-forward-voltage characteristics.

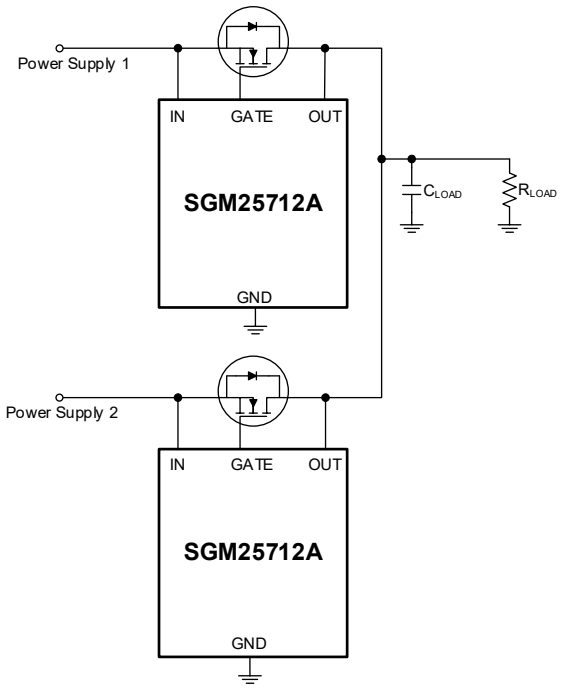


Figure 6. ORing with MOSFETs

Feature Description

IN, GATE, and OUT Pins

Upon initial power application, the load current passes via the MOSFET's body diode from source to drain. As soon as the voltage over the body diode (V_{SD}) exceeds the V_{SD_REG} threshold, the SGM25712A activates a 32μA charge pump current source to initiate MOSFET gate charging.

The SGM25712A is intended to control the gate-to-source voltage (V_{GS}) of the MOSFET. If the current through the MOSFET drops, such that the source-to-drain voltage drops below the 15mV (TYP) V_{SD_REG} threshold, the voltage at the GATE pin will decrease until V_{SD} stabilizes at 15mV. Conversely, if V_{SD} exceeds the V_{SD_REG} regulation point, V_{GS} increases until it reaches the 11.8V (TYP). In addition, the internal Zener diode between the GATE and IN pins of the SGM25712A can clamp V_{GS} to 17V or less.

When the MOSFET current reverses (e.g., due to input supply failure), causing the voltage between SGM25712A's IN and OUT pins to drop below the V_{SD_REV} threshold (-33mV TYP), the SGM25712A activates a strong internal GATE-to-IN discharge transistor to rapidly discharge the MOSFET gate.

DETAILED DESCRIPTION (continued)

In cases of abrupt input supply failure (e.g., shorted to ground), a temporary reverse current flows via the MOSFET until the gate discharges completely. This current originates from parallel power supplies as well as load capacitance.

The SGM25712A detects voltage reversal conditions within 23ns (TYP) and initiates gate discharge. Turn-off time depends on the MOSFET's gate capacitance (C_{GS}); for example, a 47nF C_{GS} allows full turn-off within 154ns (TYP). This rapid response suppresses transient voltage and current effects at the output, reducing disturbances from redundant power supplies.

OFF Pin and nFGD Pin

The OFF pin is a logic-level input that controls the gate drive to the external MOSFET in FET Test Mode. This mode is intended to detect whether the MOSFET is shorted, (i.e. IN-to-OUT short). When the OFF pin is high, the MOSFET is turned off regardless of the sensed IN and OUT voltages, and FET Test Mode is activated. In this mode, the MOSFET is turned off, and load current flows through its body diode from input to output. If the MOSFET is operating normally, the voltage drop is approximately 700mV. The FET test comparator of the SGM25712A monitors the IN to OUT voltage difference, with a V_{SD_TST} threshold of 347mV (TYP). If the IN-to-OUT voltage difference is greater than the V_{SD_TST} threshold, nFGD is at logic low. Conversely, if the IN-to-OUT voltage difference is less than the V_{SD_TST} threshold, nFGD is pulled high to logic high through an external pull-up resistor.

The OFF pin has an internal pull-down of 5.1μA (TYP). If FET Test Mode is not used, this pin should be grounded or left floating. When the OFF pin is low, the nFGD pin is not activated and remains in a high-impedance state.

Some application conditions may prevent nFGD pin from indicating that the external MOSFET is operating normally. For example, when the SGM25712A is used in parallel redundant power supplies, the OUT pin voltage of one supply may be forced close enough to the IN pin voltage, and consequently, the sensed IN-to-OUT voltage difference does not exceed the V_{SD_TST} threshold. In addition, with a large output capacitance and a low load current, the output capacitor may require a considerable amount of time to discharge. nFGD does not switch low until the IN-to-OUT voltage difference exceeds the V_{SD_TST} threshold.

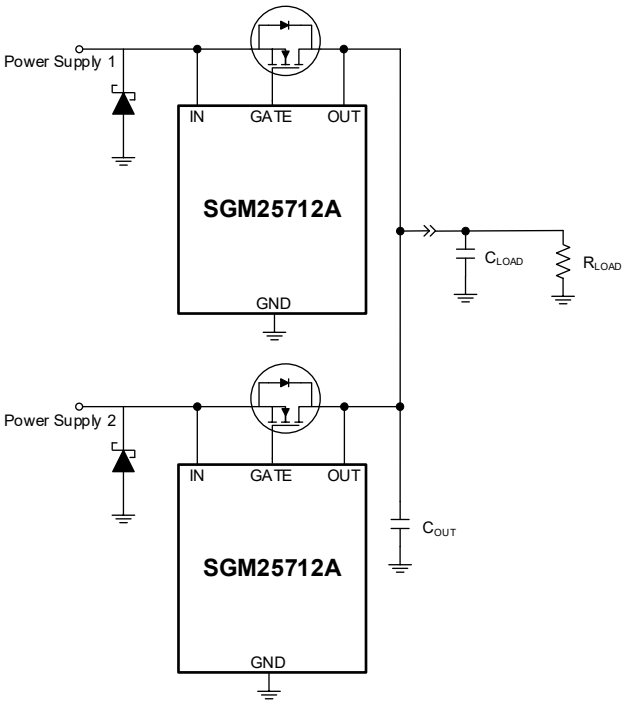


Figure 7. Typical Connection

APPLICATION INFORMATION

Short-Circuit Failure of an Input Supply

An abrupt short-circuit (0Ω) across the input voltage source induces the maximum possible backflow current during the discharge phase of the MOSFET gate by the SGM25712A's internal controller. This reverse current magnitude is constrained solely by the MOSFET's on-state resistance (R_{DSON}), combined with resistive losses and inductive effects from parasitic wiring elements. See Figure 8 for details. The peak instantaneous reverse current under worst-case conditions would thus be determined by:

$$I_{D_REV} = \left(V_{OUT} - V_{IN}\right) / R_{DSON} \quad (1)$$

The internal reverse comparator will activate and begin discharging the gate terminal as soon as reverse current reaches:

$$I_{D_REV} = V_{SD_REV} / R_{DSON} \quad (2)$$

Upon complete MOSFET deactivation, the energy accumulated in parasitic wiring inductances is dissipated into the remaining circuitry. Consequently, the IN pin of the SGM25712A experiences a negative voltage surge, whereas the OUT pin undergoes a positive voltage surge. To protect the IN pin, a diode clamp to ground can be applied to suppress negative voltage. The output pin can be protected using a local bypass capacitor or a TVS diode. In low-voltage applications, the MOSFET's drain-source breakdown voltage (V_{BR_DSS}) might suffice for OUT pin protection, provided V_{IN} + $V_{BR_DSS_MAX}$ remains below 75V. However, since datasheets typically do not guarantee the maximum breakdown thresholds, reliance on this approach is advisable only under careful evaluation.

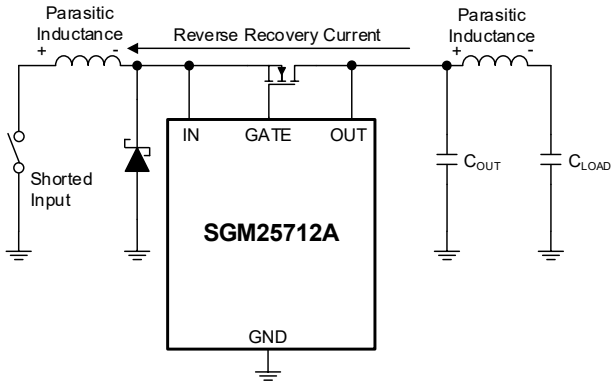


Figure 8. Input Supply Fault Transients

Table 1. FET Test Status Table

OFF Pin	Mode	FET Gate Drive	V_{IN} - V_{OUT}	FET Status	nFGD Pin Status	nFGD Pin Voltage
Low or Open	Normal Operation	Active	-	-	Hi-Z	High
High	FET Test	Off	> V_{SD_TST}	OK	Low-Z	Low
			< V_{SD_TST}	Not OK	Hi-Z	High

MOSFET Selection

The critical electrical parameters of the MOSFET include the maximum continuous drain current (I_D), maximum source current (I_S, body diode rating), maximum drain-source voltage (V_{DS_MAX}), threshold voltage (V_{GS_TH}), drain-source reverse breakdown voltage (V_{BR_DSS}) and on-state resistance (R_{DSON}).

Drain current (I_D): the rated I_D must exceed system load current to prevent thermal overstress.

Body diode current (I_S): I_S is normally equal to, or a little above, the drain current rating, although that current only flows while the gate is being charged towards V_{GS_TH}.

Gate Charge Time (t_Q): defined by the equation $t_Q = Q_G/I_{GATE_ON}$, where Q_G represents total gate charge and I_{GATE_ON} is the drive current during MOSFET turn-on.

1. Drain-source voltage (V_{DS_MAX}): must exceed the peak application voltage (including fault conditions) to prevent breakdown.
2. Reverse breakdown voltage (V_{BR_DSS}): in low-voltage applications, this parameter provides transient protection for the OUT pin by enabling a conduction path from OUT to IN during positive voltage spikes on the OUT pin.
3. The threshold voltage (V_{GS_TH}) between gate and source has to be compatible with what the SGM25712A driver can deliver. Logic-level MOSFETs, with R_{DSON} quoted at a 4V gate-source threshold, are the usual choice. Sub-logic-level devices quoted at 2.5V V_{GS_TH} are also usable, provided their other ratings are checked against the output capability of the driver.

APPLICATION INFORMATION (continued)

4. The dominant loss in the MOSFET of an SGM25712A active ORing arrangement is conduction loss, set by the source-to-drain current flowing into the load and by the R_{DSON} of the device. Lowering R_{DSON} is the obvious way to cut that loss, but choosing the lowest available R_{DSON} does not always give a good result, which is the opposite of the usual expectation. Several factors are behind this.

   (1) Reverse transition detection is crucial for system reliability. Increased on-state resistance (R_{DSON}) enhances voltage signal amplification to the SGM25712A's reverse comparator even under reduced reverse current conditions. This enables faster MOSFET shutdown triggering if the input voltage path is grounded, thereby minimizing potential disruptions to the redundant power bus.

   (2) Reverse conduction leakage. When multiple input power sources exhibit voltage levels closely aligned, a minor current might persistently traverse the MOSFET's drain-source path (reverse conduction) without triggering the SGM25712A's reverse detection circuitry. However, elevated on-resistance (R_{DSON}) reduces this reverse conduction current magnitude by increasing impedance in the leakage pathway.

   (3) There is an inverse relationship between MOSFET cost and on-state resistance (R_{DSON}): lower R_{DSON} values generally correlate with higher component costs. This arises because reducing R_{DSON} typically requires larger die sizes, thicker metal layers, or advanced process technologies to maintain low resistance, all of which increase fabrication expenses.

5. The primary loss mechanism in the SGM25712A's MOSFET-based active ORing configuration is conduction loss, which scales with the square of the source-to-drain current (I_{DS}^2) multiplied by the MOSFET's on-resistance (R_{DSON}). Reducing R_{DSON} directly minimizes this loss but introduces critical trade-offs that must be evaluated holistically:

   (1) A MOSFET with an excessively high R_{DSON} value may cause substantial power losses. Additionally, during regulation toward the V_{SD_REG} threshold of 15mV, the SGM25712A driver will fully charge the MOSFET gate to its maximum capacity while attempting to drive the drain-source voltage to this target. Higher gate charge lengthens the turn-off discharge time because the gate discharge current remains constant.

   (2) R_{DSON} selection is advised to maintain a voltage drop between 15mV and 100mV under nominal load conditions to adhere to the recommended operational guidelines. Formula: $(15mV / I_D) \leq R_{DSON} \leq (100mV / I_D)$.

   (3) When designing MOSFET packages, thermal resistance must be assessed alongside expected power loss to keep the junction temperature (T_J) within acceptable operational boundaries, as elevated T_J values directly elevate the on-state resistance (R_{DSON}), thereby compromising device efficiency under thermal loading.

6. $P_D = I_D^2 \times (R_{DSON})$

7. With T_A = +35℃, I_{LOAD} = 10A and R_{DSON} = 10mΩ, the required maximum rated junction-to-ambient thermal resistance (θ_{JA}) to maintain junction temperature (T_J) below +100 ℃ is calculated through the following derivation. First, compute power dissipation (P_D): $P_D = I_D^2 \times R_{DSON} = (10A)^2 \times 10m\Omega = 1W$. The thermal resistance θ_{JA} is then determined via the equation $T_J = T_A + P_D \times \theta_{JA}$. Rearranging for θ_{JA} gives $\theta_{JA} \leq (T_J - T_{A_MAX}) / P_D = (100℃ - 35℃) / 1W = 65℃/W$.

TYPICAL APPLICATIONS

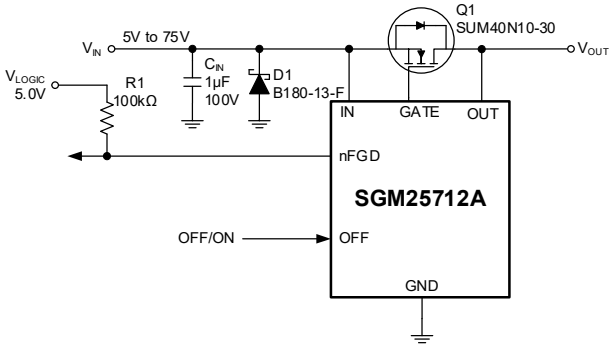


Figure 9. Basic Application with Input Transient Protection

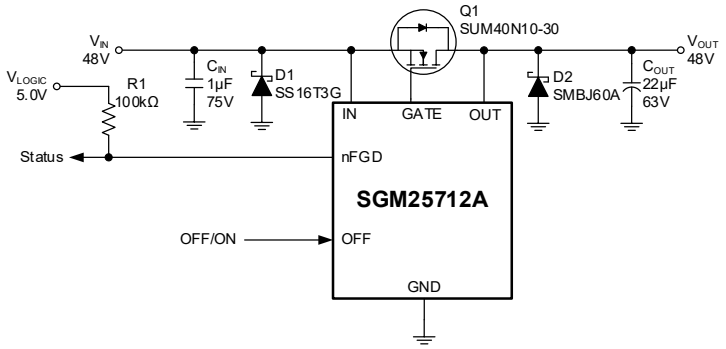


Figure 10. Typical +48V Application with Transient Protection

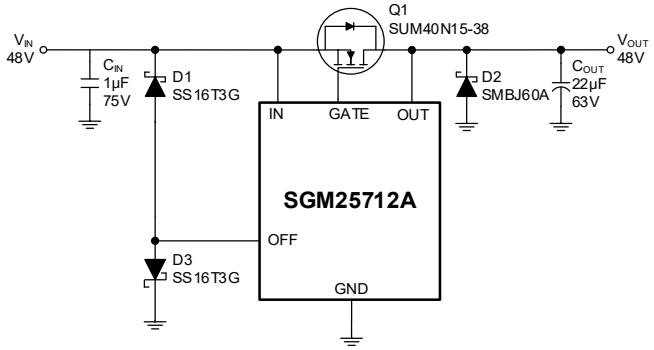


Figure 11. +48V Application with Reversed Input Voltage (V_{IN} = -48V) Protection

Layout Guidelines

- To ensure stable operation in all designs, SGMICRO advises placing a ceramic decoupling capacitor with a capacitance of 1μF between the input (IN) and ground (GND) terminals.
- The decoupling capacitor should be positioned as near as possible to the IN and GND pins of the device. Critical attention is required to reduce the loop area generated by the bypass capacitor's trace connections, the input (IN) terminal, and the ground (GND) node of the device.
- High-current power paths require the shortest possible trace lengths with cross-sectional areas rated for double the full-load current.
- The IN and OUT pads are designed for heat dissipation. To maximize thermal performance, connect them to large-area copper regions on both the top and bottom PCB layers via thermal vias. Strategically placing vias beneath the device minimizes voltage gradients across the IN and OUT pads and ensures uniform current distribution through the component. These measures are critical to achieving optimal on-resistance and precise current-sense accuracy.
- To ensure optimal performance, it is recommended that the IN, GATE, and OUT terminals be placed adjacent to the source and drain terminals of the MOSFET.

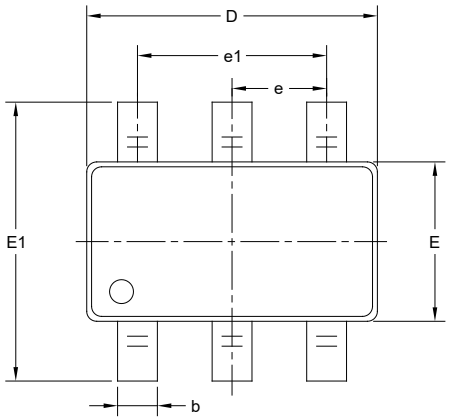
REVISION HISTORY

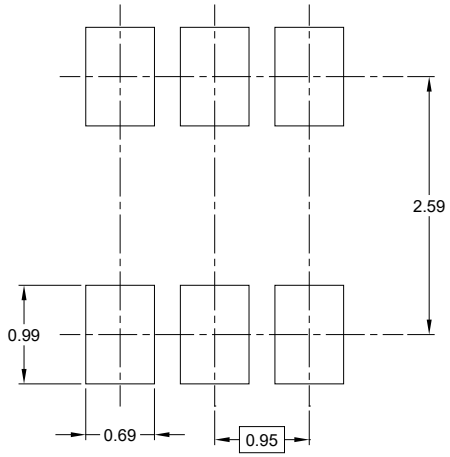
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2026)	Page
Changed from product preview to production data	All

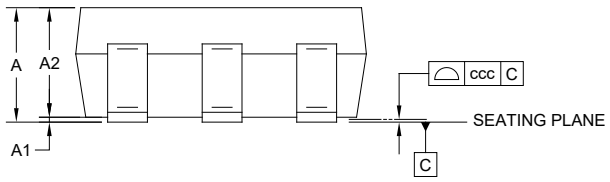
PACKAGE OUTLINE DIMENSIONS

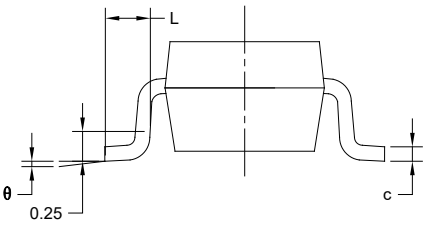
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



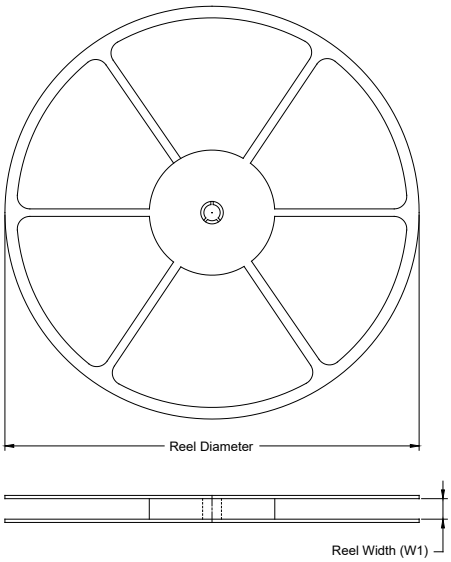


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

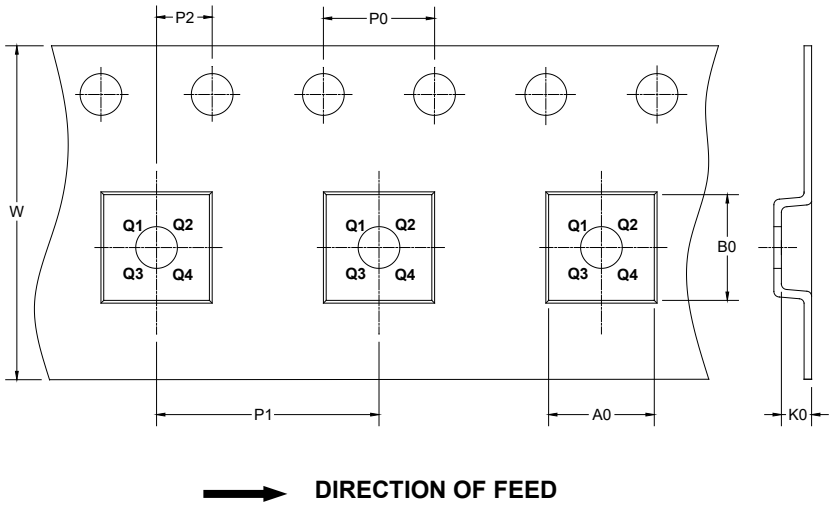
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



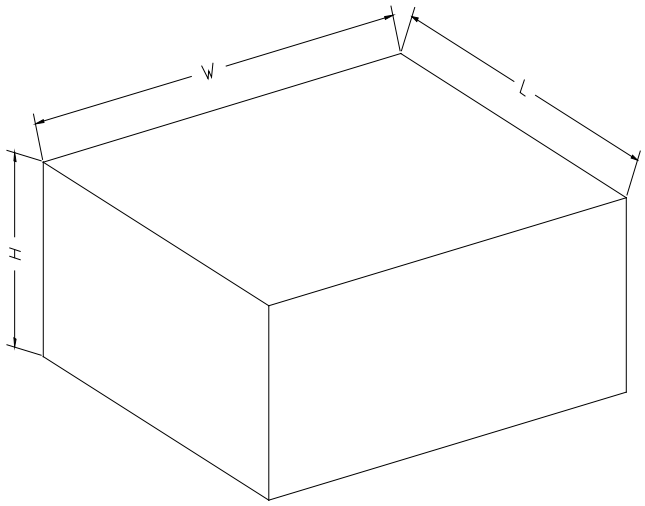
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002